



**Flash-ROM Module 8MByte (2Mx32Bit), 80Pin-SMM, 3.3V Design**  
**Part No. HMF2M32F4VSB**

## GENERAL DESCRIPTION

The HMF2M32F4VSB is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of four 1M x 16 FROM mounted on a 80-pin stackable type, double - sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits. When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3.0V DC power supply and all inputs and outputs are LVTTTL-compatible.

## FEATURES

- w Part Identification
  - HMF2M32F4VSB : Socket 5mm
- w Access time: 90, 100, 120ns
- w High-density 8MByte design
- w High-reliability, low-power design
- w Single + 3.0V  $\pm$  0.5V power supply
- w All in/outputs are LVTTTL-compatible
- w FR4-PCB design
- w 80-pin Designed by
  - 40-pin Fine Pitch Connector (x 2EA)
- w Minimum 1,000,000 write/erase cycle
- w Sector erases architecture

## OPTIONS

## MARKING

- w Timing
 

90ns access	-90
100ns access	-100
120ns access	-120
- w Packages
 

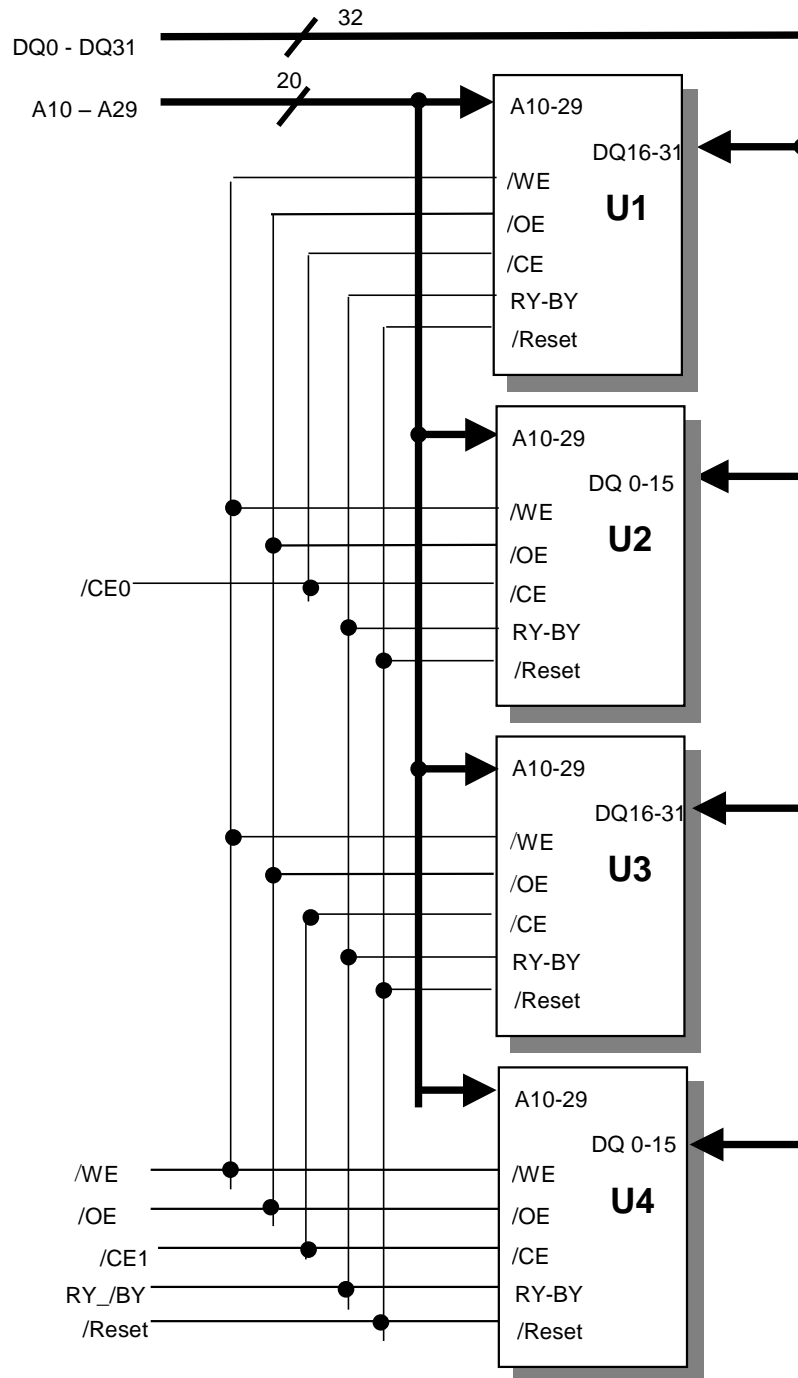
80-pin SMM	F
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## PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	VCC	21	VCC	1	VCC	21	VCC
2	CE0*	22	DQ16	2	DQ15	22	NC
3	NC	23	DQ24	3	DQ7	23	NC
4	NC	24	DQ17	4	DQ14	24	BYTE*
5	NC	25	DQ25	5	DQ6	25	OE*
6	RY_BY*	26	DQ18	6	DQ13	26	CE1*
7	VSS	27	VSS	7	VSS	27	VSS
8	RESET*	28	DQ26	8	DQ5	28	A13
9	WE*	29	DQ19	9	DQ12	29	A29
10	A10	30	DQ27	10	DQ4	30	A11
11	A21	31	DQ20	11	DQ11	31	A12
12	A20	32	DQ28	12	DQ3	32	A22
13	A19	33	DQ21	13	DQ10	33	A23
14	VSS	34	VSS	14	VSS	34	VSS
15	A18	35	DQ29	15	DQ2	35	A24
16	A17	36	DQ22	16	DQ9	36	A25
17	A16	37	DQ30	17	DQ1	37	A26
18	A15	38	DQ23	18	DQ8	38	A27
19	A14	39	DQ31	19	DQ0	39	A28
20	VCC	40	VCC	20	VCC	40	VCC

<sup>4</sup> cf : Address & Data Bus is organized for LG Specification.  
 ( A10 & DQ0 are MSB, A29 & DQ31 are LSB)

FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	$V_{CC} \pm 0.3V$	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	$D_{OUT}$	ACTIVE
WRITE or ERASE	X	L	L	H	$D_{IN}$	ACTIVE

NOTE: X means don't care

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to $V_{CC} + 0.5V$
Voltage with respect to ground $V_{CC}$	$V_{CC}$	-0.5V to +4.0V
Storage Temperature	$T_{STG}$	-65°C to +150°C
Operating Temperature	$T_A$	-40°C to +85°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
$V_{CC}$ for $\pm 10\%$ device Supply Voltages	$V_{CC}$	2.7V	3.0	3.6V
Ground	$V_{SS}$	0	0	0

DC AND OPERATING CHARACTERISTICS (  $0^{\circ}C \leq T_A \leq 70^{\circ}C$  )

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	$V_{CC} = V_{CC \text{ max}}, V_{IN} = \text{GND to } V_{CC}$	$I_{L1}$	-10	1.0	$\mu A$
Output Leakage Current	$V_{CC} = V_{CC \text{ max}}, V_{OUT} = \text{GND to } V_{CC}$	$I_{L0}$	-10	1.0	$\mu A$
Output High Voltage	$I_{OH} = -2.0mA, V_{CC} = V_{CC \text{ min}}$	$V_{OH}$	$0.85 \times V_{CC}$	-	V
Output Low Voltage	$I_{OL} = 4.0mA, V_{CC} = V_{CC \text{ min}}$	$V_{OL}$	-	0.4	V
Vcc Active Read Current (1)	/CE = $V_{IL}$ , /OE = $V_{IH}$	5MHZ	-	64	mA
		1MHZ	-	32	
Vcc Active Write Current (2)	/CE = $V_{IL}$ , /OE = $V_{IH}$	$I_{CC2}$	-	120	mA
Vcc Standby Current	/CE, /RESET = $V_{CC} \pm 0.3V$	$I_{CC3}$	-	120	mA
Low Vcc Lock-Out Voltage		$V_{LKO}$	1.5	-	V

Notes: 1. The  $I_{CC}$  current listed includes both the DC operating current and the frequent component (at 5MHz).

2.  $I_{CC}$  active while embedded algorithm (program or erase) is in progress

3. Not 100% tested

## ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Block Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		27		sec	
Word Programming Time	-	11	330	μs	Excludes system-level overhead
Chip Programming Time	-	12	36	sec	

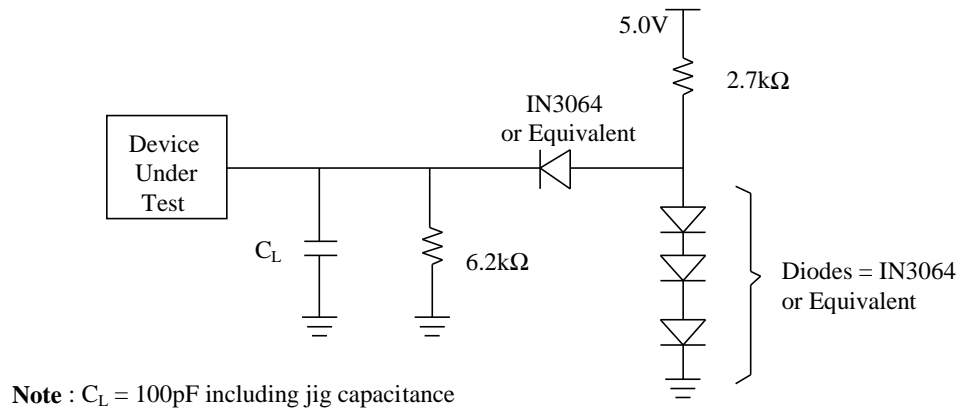
**TSOP CAPACITANCE**

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	-	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	-	10	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	-	10	pF

**Notes :** Capacitance is periodically sampled and not 100% tested.

**TEST SPECIFICATIONS**

TEST CONDITION	VALUE	UNIT
Output load	1TTL gate	
Input rise and full times	5	ns
Input pulse levels	0 to 3	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V



## AC CHARACTERISTICS

## └ Read Only Operations Characteristics

PARAMETER	DESCRIPTION	SPEED						UNIT
		- 90		-100		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	90		100		120		ns
t <sub>ACC</sub>	Address Access time		90		100		120	ns
t <sub>CE</sub>	Chip Enable to Access time		90		100		120	ns
t <sub>OE</sub>	Output Enable time		35		40		50	ns
t <sub>DF</sub>	Chip Enable to Output High-Z		30		30		30	ns
t <sub>OEH</sub>	Output Enable Hold Time	0		0		0		ns
t <sub>QH</sub>	Output Hold Time From Addresses, /CE or /OE	0		0		0		ns

└ Erase/Program Operations  
Alternate /WE Controlled Writes

PARAMETER	DESCRIPTION	- 90		-100		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time (1)	90	-	100	-	120	-	ns
t <sub>AS</sub>	Address Setup Time	0	-	0	-	0	-	ns
t <sub>AH</sub>	Address Hold Time	45	-	45	-	50	-	ns
t <sub>DS</sub>	Data Setup Time	45	-	45	-	50	-	ns
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-	ns
t <sub>OES</sub>	Output Enable Setup Time	0	-	0	-	0	-	ns
t <sub>GHWL</sub>	Read Recover Time Before Write	0	-	0	-	0	-	ns
t <sub>CS</sub>	/CE Setup Time	0	-	0	-	0	-	ns
t <sub>CH</sub>	/CE Hold Time	0	-	0	-	0	-	ns
t <sub>WP</sub>	Write Pulse Width	45	-	45	-	50	-	ns
t <sub>WPH</sub>	Write Pulse Width High	30	-	30	-	30	-	ns
t <sub>PGM</sub>	Programming Operation	11		11		11		ns
t <sub>BERS</sub>	Block Erase Operation (2)	0.7	-	0.7	-	0.7	-	ns
t <sub>VCS</sub>	Vcc set up time	50	-	50	-	50	-	ns
t <sub>RB</sub>	Write Recover Time Before RY_/BY	0	-	0	-	0	-	ns
t <sub>RH</sub>	/RESRT High Before Read	50	-	50	-	50	-	ns
t <sub>RPD</sub>	/RESRT to Power Down Time	20	-	20	-	20	-	ns
t <sub>RP</sub>	/RESRT Pulse Width	500	-	500	-	500	-	ns
t <sub>RSTS</sub>	/RESRT Setup Time	500	-	500	-	500	-	ns

Notes :: 1. Not 100% tested

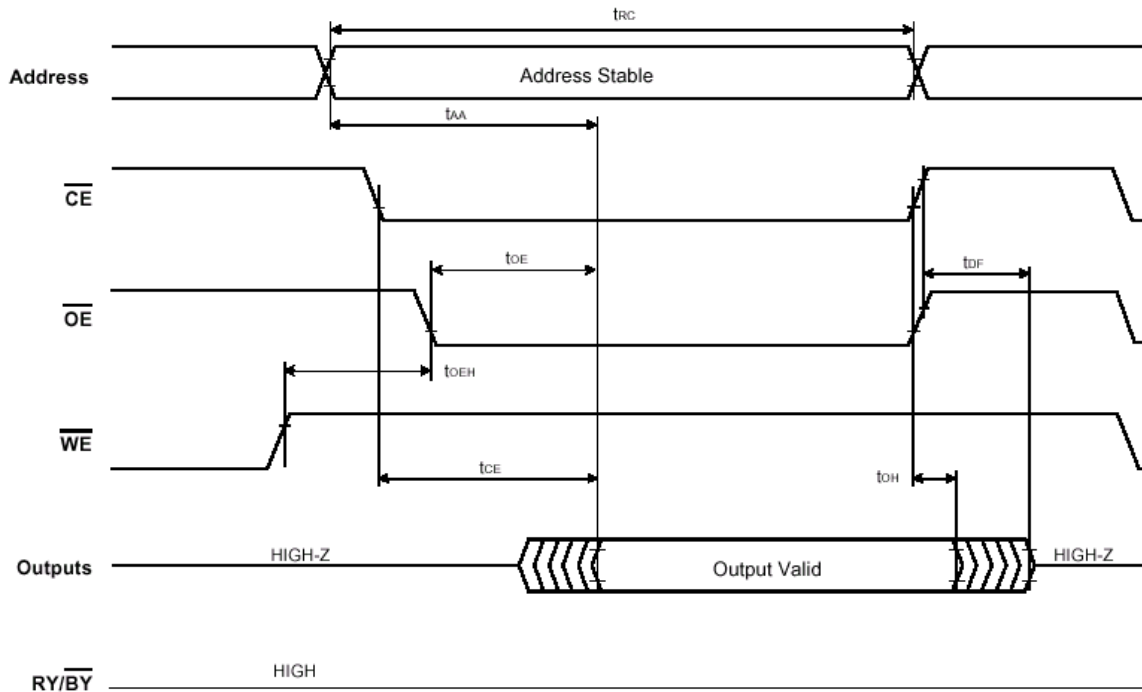
2 . The duration of the program or erase operation varies and is calculated in the internal algorithms.

**U Erase/Program Operations  
Alternate /CE Controlled Writes**

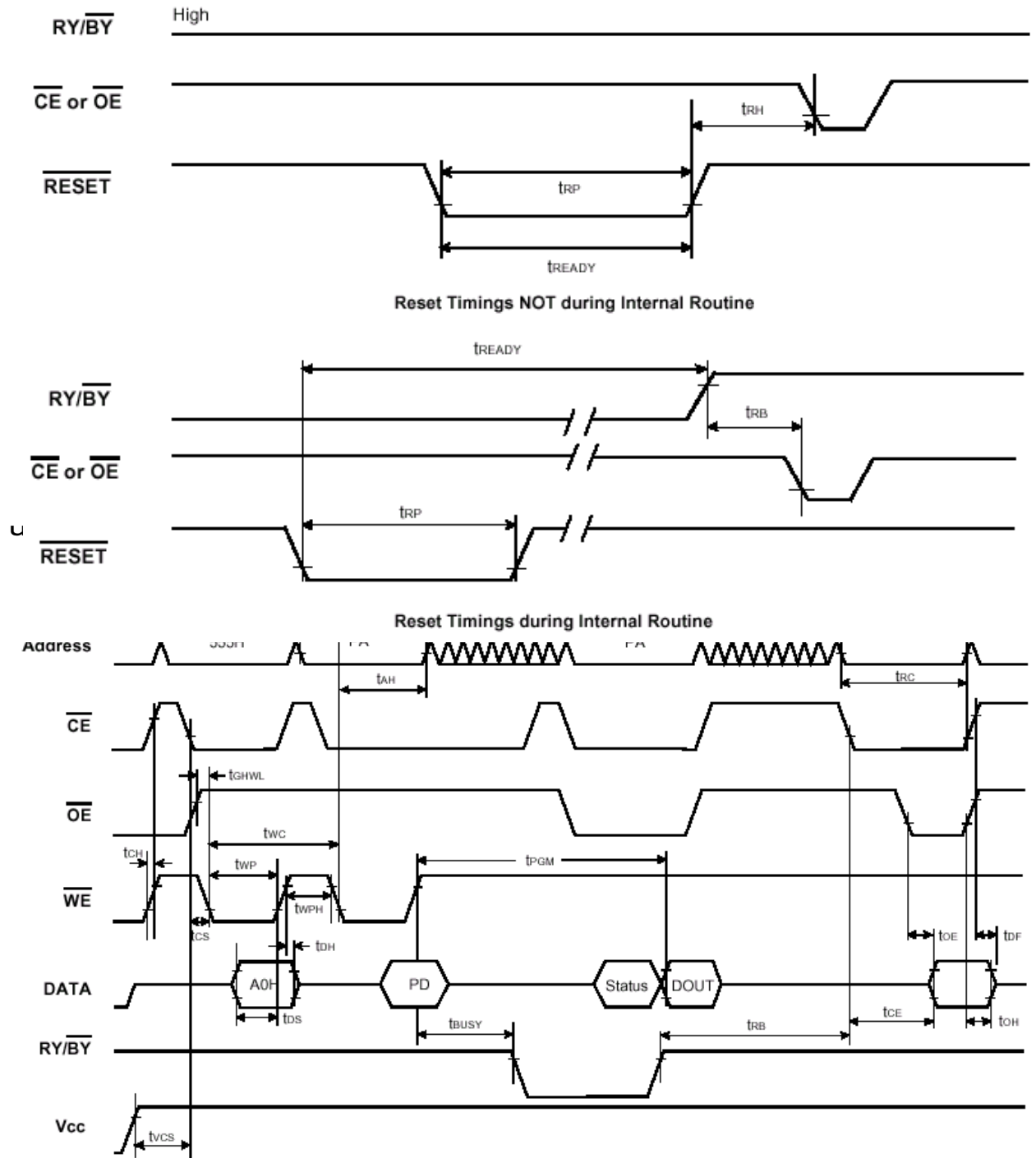
PARAMETER	DESCRIPTION	- 90		-100		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{WC}$	Write Cycle Time(1)	90	-	100	-	120	-	ns
$t_{AS}$	Address Setup Time	0	-	0	-	0	-	ns
$t_{AH}$	Address Hold Time	45	-	45	-	50	-	ns
$t_{DS}$	Data Setup Time	45	-	45	-	50	-	ns
$t_{DH}$	Data Hold Time	0	-	0	-	0	-	ns
$t_{OES}$	Output Enable Setup Time	0	-	0	-	0	-	ns
$t_{GHWL}$	Read Recover Time Before Write	0	-	0	-	0	-	ns
$t_{CS}$	/CE Setup Time	0	-	0	-	0	-	ns
$t_{CH}$	/CE Hold Time	0	-	0	-	0	-	ns
$t_{WP}$	Write Pulse Width	45	-	45	-	50	-	ns
$t_{WPH}$	Write Pulse Width High	30	-	30	-	30	-	ns
$t_{PGM}$	Programming Operation	11		11		11		ns
$t_{BERS}$	Block Erase Operation (2)	0.7	-	0.7	-	0.7	-	ns

- Notes :** 1. Not 100% tested  
 2. This does not include the preprogramming time

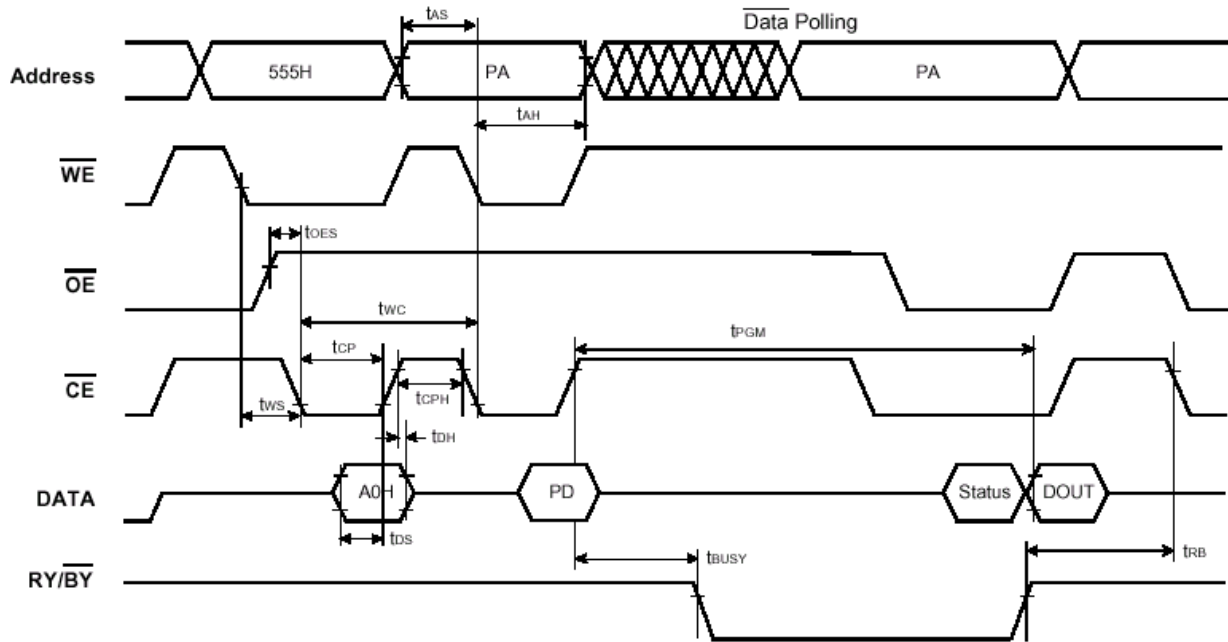
**U READ OPERATIONS TIMING**



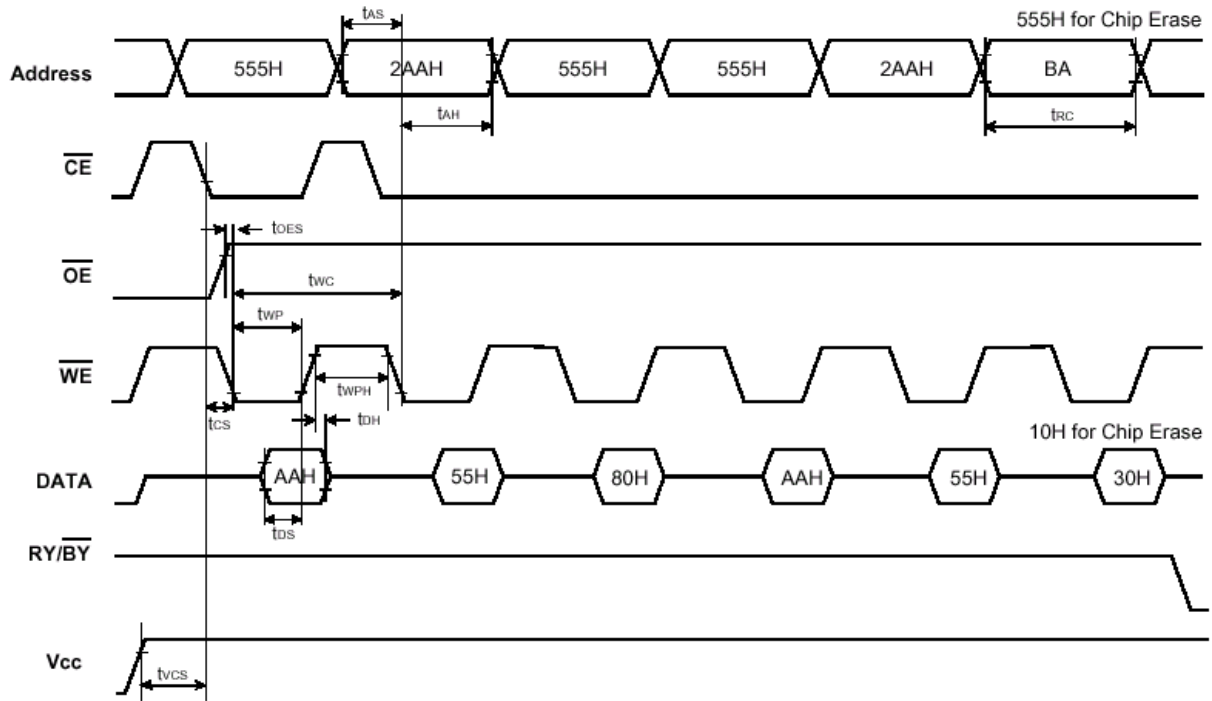
RESET TIMING



Alternate /CE Controlled Writes

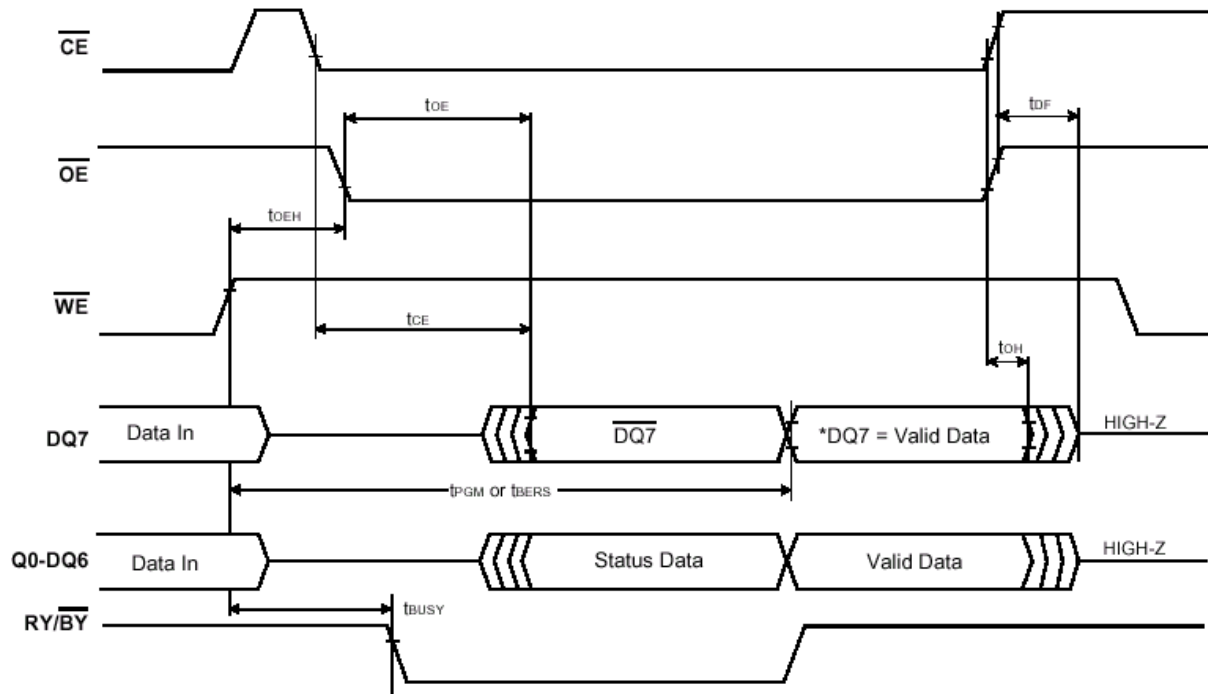


CHIP/BLOCK ERASE OPERATION TIMINGS

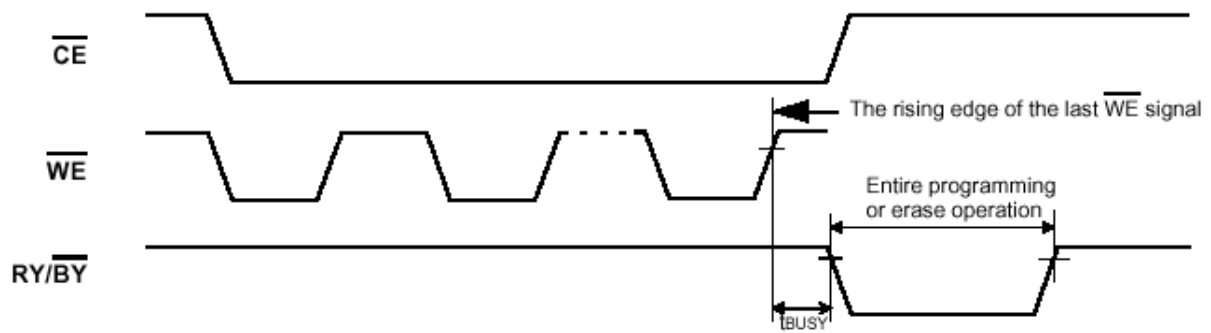




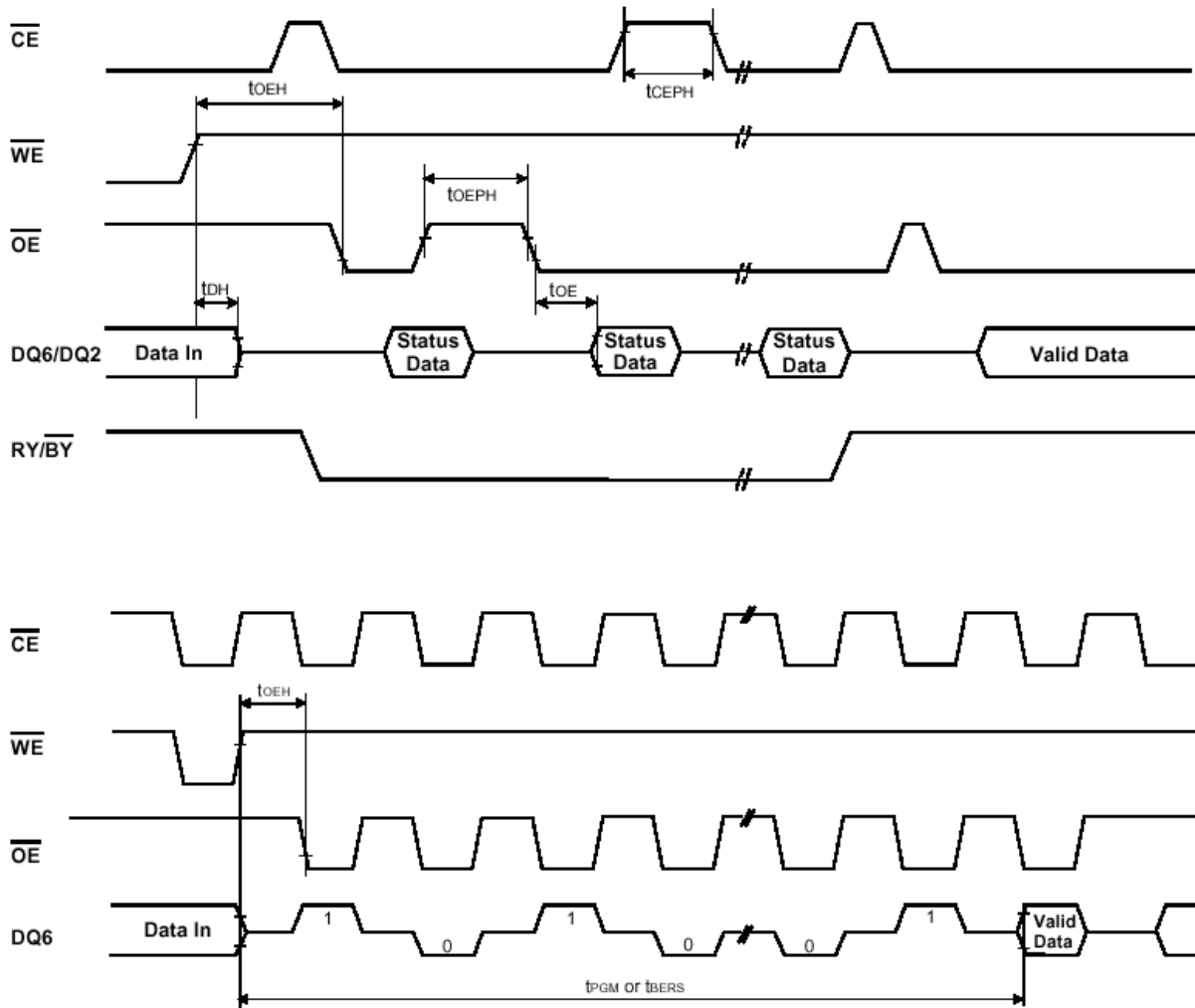
DATA# POLLING TIMES DURING INTERNAL ROUTINE OPERATION



RY\_ /BY TIMING DURING ERASE / PROGRAM OPERATION

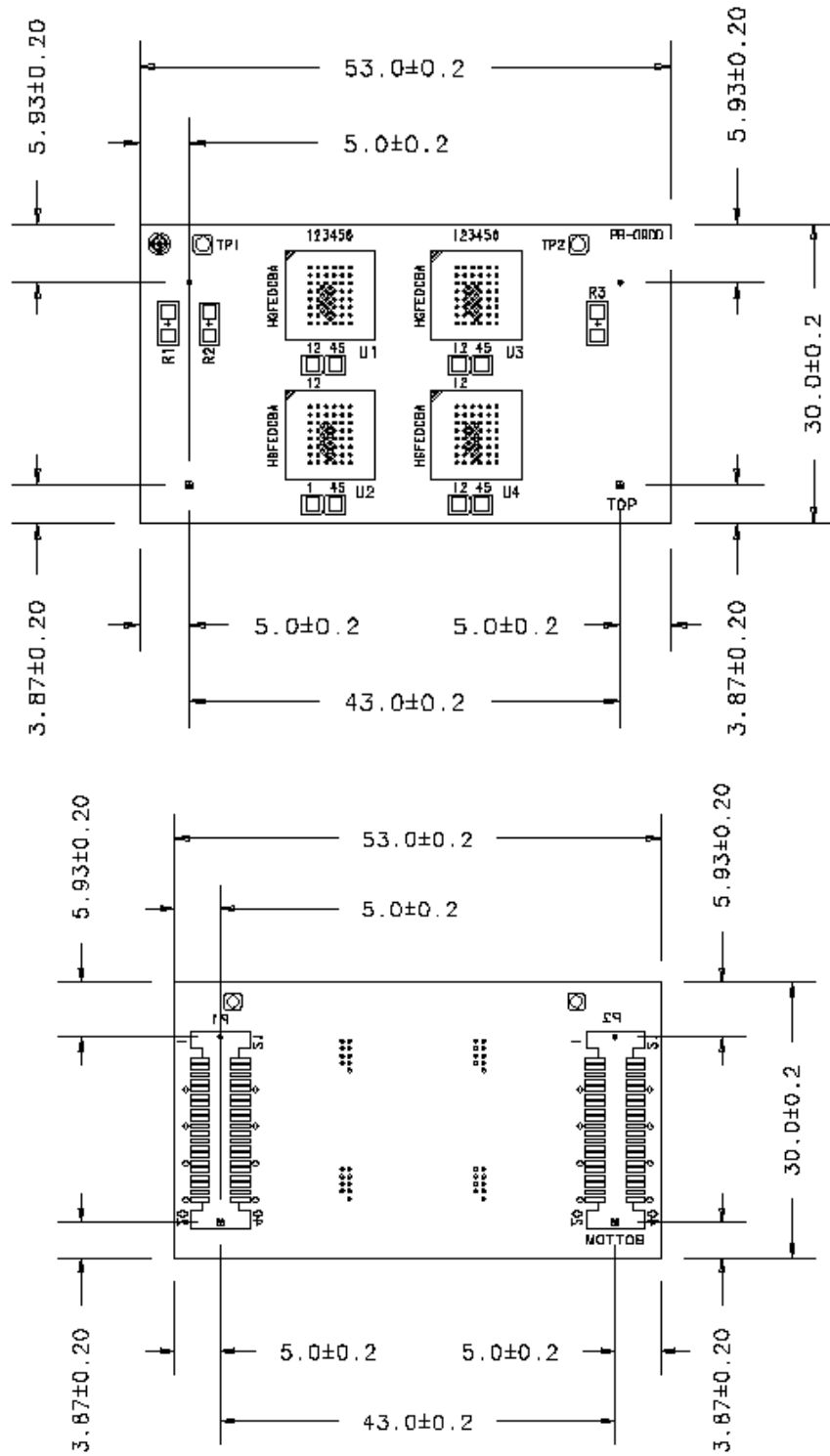


□ TOGGLE# BIT DURING INTERNAL ROUTINE OPERATION



PACKAGE DIMMENSIONS

Unit : mm



PCB Thickness : 1.3 ± 0.1mm

**ORDERING INFORMATION**

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
<b>HMF2M32F4VSB-90</b>	8MByte	x 32	80Pin –SMM	4EA	3.3V	90ns
<b>HMF2M32F4VSB-100</b>	8Mbyte	x 32	80Pin –SMM	4EA	3.3V	100ns
<b>HMF2M32F4VSB-120</b>	8Mbyte	x 32	80Pin –SMM	4EA	3.3V	120ns