PCA9306

Dual bidirectional I²C-bus and SMBus voltage-level translator

Rev. 04 — 26 October 2009 Product data sheet

1. General description

The PCA9306 is a dual bidirectional I²C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.6 V ($V_{ref(1)}$) and 1.8 V to 5.5 V ($V_{bias(ref)(2)}$).

The PCA9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PCA9306 is not a bus buffer like the PCA9509 or PCA9517A that provide both level translation and physically isolates the capacitance to either side of the bus when both sides are connected. The PCA9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PCA9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I²C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I²C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2 MHz.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

2. Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I²C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I²C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Allows voltage level translation between:
  - 1.0 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.2 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.8 V $V_{ref(1)}$ and 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 2.5 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
  - 3.3 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 Ω ON-state connection between input and output ports provides less signal distortion
- Open-drain I²C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I²C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Packages offered: SO8, TSSOP8, VSSOP8, XQFN8

3. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C.

Type number	Topside mark	Package		
		Name	Description	Version
PCA9306D	PCA9306	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9306DP	306P	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9306DC	306C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
PCA9306DP1[2]	306T	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
PCA9306DC1[3]	P06	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
PCA9306GM	P6X[4]	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-1

[1] Also known as MSOP8.

[2] Same footprint and pinout as the Texas Instruments PCA9306DCT.

[3] Same footprint and pinout as the Texas Instruments PCA9306DCU.

[4] 'X' will change based on date code.

4. Functional diagram

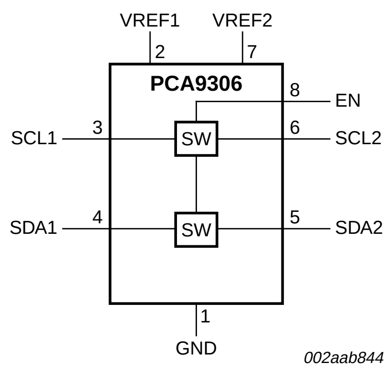


Fig 1. Logic diagram of PCA9306 (positive logic)

5. Pinning information

5.1 Pinning

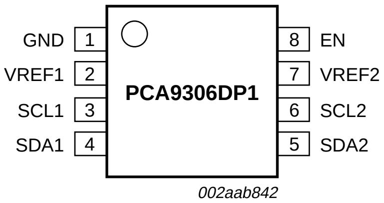


Fig 2. Pin configuration for TSSOP8 (DP1)

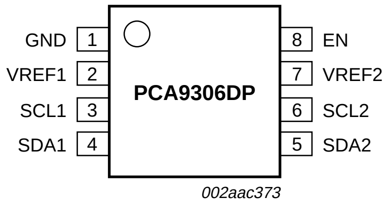


Fig 3. Pin configuration for TSSOP8 (DP) (MSOP8)

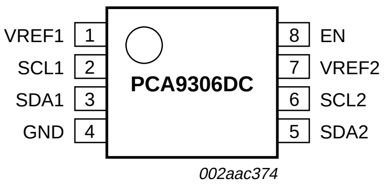


Fig 4. Pin configuration for VSSOP8 (DC)

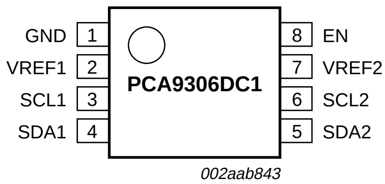


Fig 5. Pin configuration for VSSOP8 (DC1)

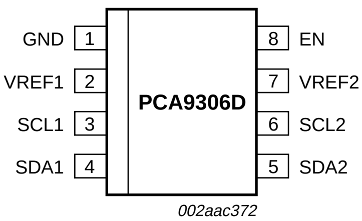


Fig 6. Pin configuration for SO8

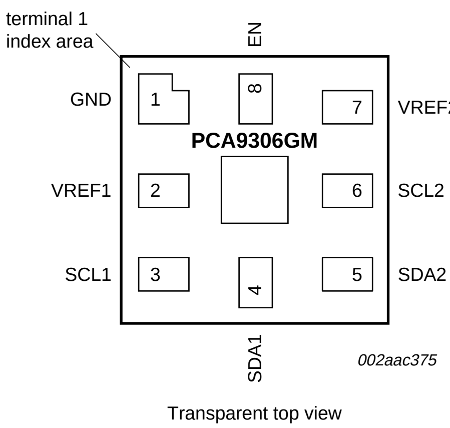


Fig 7. Pin configuration for XQFN8

5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SO8, TSSOP8 (MSOP8), TSSOP8, VSSOP8 (DC1), XQFN8	VSSOP8 (DC)	
GND	1	4	ground (0 V)
VREF1	2	1	low-voltage side reference supply voltage for SCL1 and SDA1
SCL1	3	2	serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
SDA1	4	3	serial data, low-voltage side; connect to VREF1 through a pull-up resistor
SDA2	5	5	serial data, high-voltage side; connect to VREF2 through a pull-up resistor
SCL2	6	6	serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
VREF2	7	7	high-voltage side reference supply voltage for SCL2 and SDA2
EN	8	8	switch enable input; connect to VREF2 and pull-up through a high resistor

6. Functional description

Refer to Figure 1 "Logic diagram of PCA9306 (positive logic)".

6.1 Function table

Table 3. Function selection (example)
H = HIGH level; L = LOW level.

Input EN[1]	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disconnect

[1] EN is controlled by the $V_{bias(ref)(2)}$ logic levels and should be at least 1 V higher than $V_{ref(1)}$ for best translator operation.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).
Over operating free-air temperature range.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ref(1)}$	reference voltage (1)		–0.5	+6	V
$V_{bias(ref)(2)}$	reference bias voltage (2)		–0.5	+6	V
V_I	input voltage		–0.5[1]	+6	V
$V_{I/O}$	voltage on an input/output pin		–0.5[1]	+6	V
I_{ch}	channel current (DC)		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-	–50	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	voltage on an input/output pin	SCL1, SDA1, SCL2, SDA2	0	5	V
$V_{ref(1)}$[1]	reference voltage (1)	VREF1	0	5	V
$V_{bias(ref)(2)}$[1]	reference bias voltage (2)	VREF2	0	5	V
$V_{I(EN)}$	input voltage on pin EN		0	5	V
$I_{sw(pass)}$	pass switch current		-	64	mA
T_{amb}	ambient temperature	operating in free-air	–40	+85	°C

[1] $V_{ref(1)} \leq V_{bias(ref)(2)} - 1$ V for best results in level shifting applications.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = −18 mA; $V_{I(EN)}$ = 0 V		-	-	−1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	μA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	7.1	-	pF
$C_{io(off)}$	off-state input/output capacitance	SCLn, SDAn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	4	6	pF
$C_{io(on)}$	on-state input/output capacitance	SCLn, SDAn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	9.3	12.5	pF
R_{on}	ON-state resistance[2]	SCLn, SDAn; V_I = 0 V; I_O = 64 mA	[3]				
		$V_{I(EN)}$ = 4.5 V		-	2.4	5.0	Ω
		$V_{I(EN)}$ = 3 V		-	3.0	6.0	Ω
		$V_{I(EN)}$ = 2.3 V		-	3.8	8.0	Ω
		$V_{I(EN)}$ = 1.5 V		-	9.0	20	Ω
		$V_{I(EN)}$ = 1.5 V	[4]	-	32	80	Ω
		V_I = 2.4 V; I_O = 15 mA					
		$V_{I(EN)}$ = 4.5 V		-	4.8	7.5	Ω
		$V_{I(EN)}$ = 3 V		-	46	80	Ω
		V_I = 1.7 V; I_O = 15 mA					
		$V_{I(EN)}$ = 2.3 V		-	40	80	Ω

[1] All typical values are at T_{amb} = 25 °C.

[2] Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

[3] Guaranteed by design.

[4] For DC and DC1 (VSSOP8) package only.

10. Dynamic characteristics

Table 7. Dynamic characteristics (translating down)

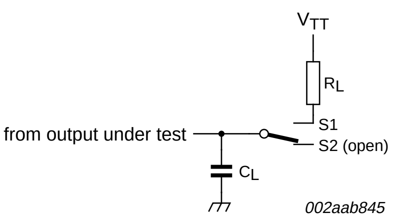
T_{amb} = −40 °C to +85 °C, unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.2	0	0.6	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.5	0	0.75	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.2	0	0.6	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.5	0	1.5	0	0.75	ns

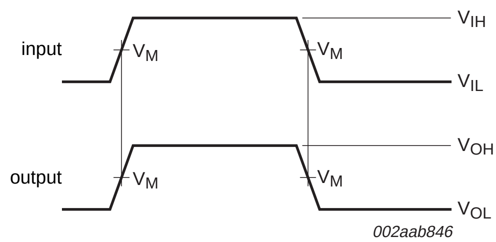
Table 8. Dynamic characteristics (translating up)

T_{amb} = −40 °C to +85 °C, unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_{TT} = 3.3 V; V_M = 1.15 V; R_L = 300 Ω (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.75	0	1.0	0	0.5	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	2.75	0	1.65	0	0.8	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_{TT} = 2.5 V; V_M = 0.75 V; R_L = 300 Ω (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.75	0	1.0	0	0.5	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	3.3	0	2.0	0	1.0	ns



a. Load circuit



b. Timing diagram

S1 = translating up; S2 = translating down.

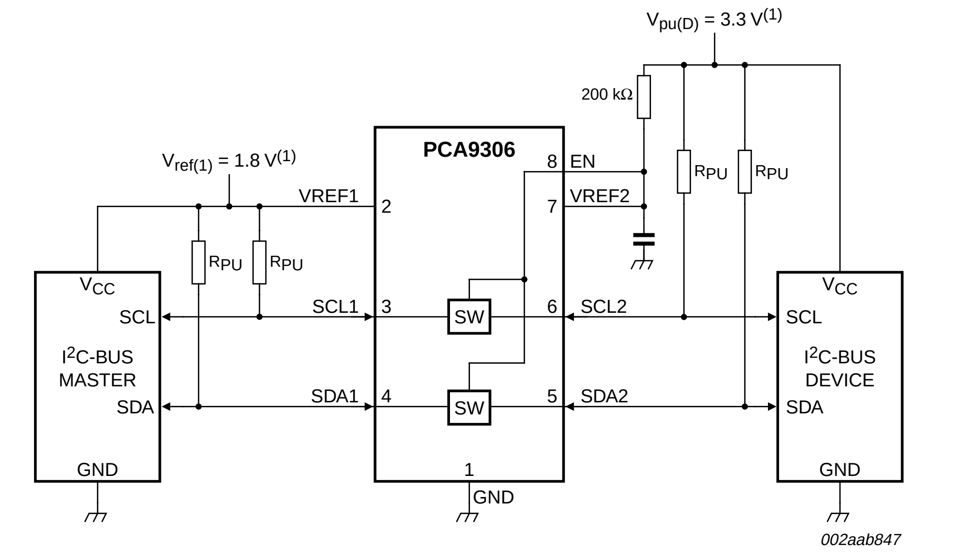
C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2 ns; t_f ≤ 2 ns.

The outputs are measured one at a time, with one transition per measurement.

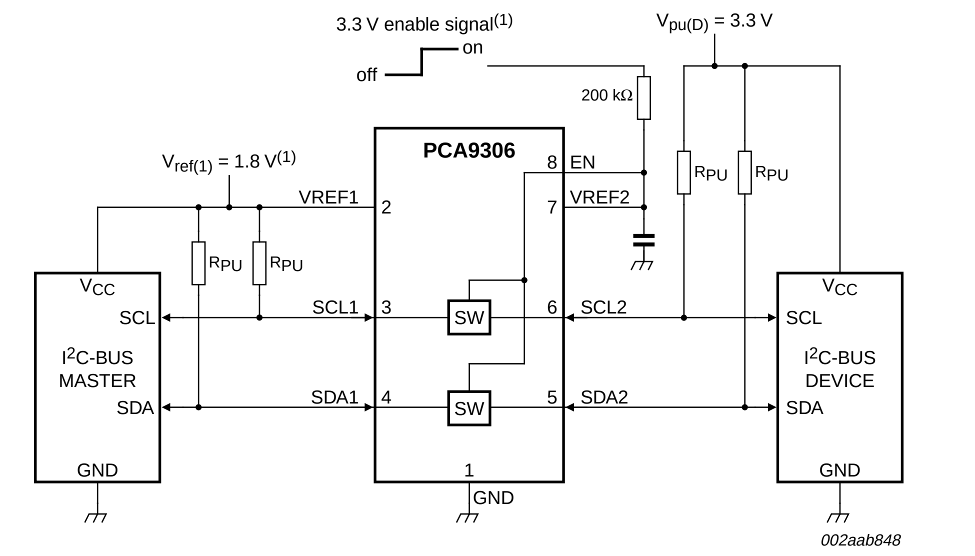
Fig 8. Load circuit for outputs

11. Application information



(1) The applied voltages at $V_{ref(1)}$ and $V_{pu(D)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Fig 9. Typical application circuit (switch always enabled)



(1) In the Enabled mode, the applied enable voltage and the applied voltage at $V_{ref(1)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Fig 10. Typical application circuit (switch enable control)

11.1 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I^2C-bus master output can be totem-pole or open-drain (pull-up resistors may be required) and the I^2C-bus device output can be totem-pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to $V_{pu(D)}$). However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{ref(1)}$) is connected to the processor core power supply voltage. When VREF2 is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V $V_{pu(D)}$ power supply, and $V_{ref(1)}$ is set between 1.0 V and ($V_{pu(D)}$ – 1 V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to $V_{pu(D)}$.

Table 9. Application operating conditions

Refer to Figure 9.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{bias(ref)(2)}$	reference bias voltage (2)		$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{I(EN)}$	input voltage on pin EN		$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{ref(1)}$	reference voltage (1)		0	1.5	4.4	V
$I_{sw(pass)}$	pass switch current		-	14	-	mA
I_{ref}	reference current	transistor	-	5	-	µA
T_{amb}	ambient temperature	operating in free-air	–40	-	+85	°C

[1] All typical values are at T_{amb} = 25 °C.

11.2 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{pu(D)} - 0.35\ V}{0.015\ A}$$

Table 10 summarizes resistor reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor values shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306 device at 0.175 V, although the 15 mA only applies to current flowing through the PCA9306 device.

Table 10. Pull-up resistor values

Calculated for V_{OL} = 0.35 V; assumes output driver V_{OL} = 0.175 V at stated current.

$V_{pu(D)}$	Pull-up resistor value (Ω)					
	15 mA		10 mA		3 mA	
	Nominal	+10 %[1]	Nominal	+10 %[1]	Nominal	+10 %[1]
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

[1] +10 % to compensate for V_{CC} range and resistor tolerance.

11.2.1 Maximum frequency calculation

The maximum frequency is totally dependent upon the specifics of the application and the device can operate > 33 MHz. Basically, the PCA9306 behaves like a wire with the additional characteristics of transistor device physics and should be capable of performing at higher frequencies if used correctly.

Here are some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306 close to the processor.
- The trace length should be less than half the time of flight to reduce ringing and reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher the drive strength (up to 15 mA), the higher the frequency the device can use.

In a 3.3 V to 1.8 V direction level shift, if the 3.3 V side is being driven by a totem pole type driver no pull-up resistor is needed on the 3.3 V side. The capacitance and line length of concern is on the 1.8 V side since it is driven through the ON resistance of the PCA9306. If the line length on the 1.8 V side is long enough there can be a reflection at the chip/terminating end of the wire when the transition time is shorter than the time of flight of the wire because the PCA9306 looks like a high-impedance compared to the wire. If the wire is not too long and the lumped capacitance is not excessive the signal will only be slightly degraded by the series resistance added by passing through the PCA9306. If the lumped capacitance is large the rise time will deteriorate, the fall time is much less affected and if the rise time is slowed down too much the duty cycle of the clock will be degraded and at some point the clock will no longer be useful. So the principle design consideration is to minimize the wire length and the capacitance on the 1.8 V side for the clock path. A pull-up resistor on the 1.8 V side can also be used to trade a slower fall time for a faster rise time and can also reduce the overshoot in some cases.

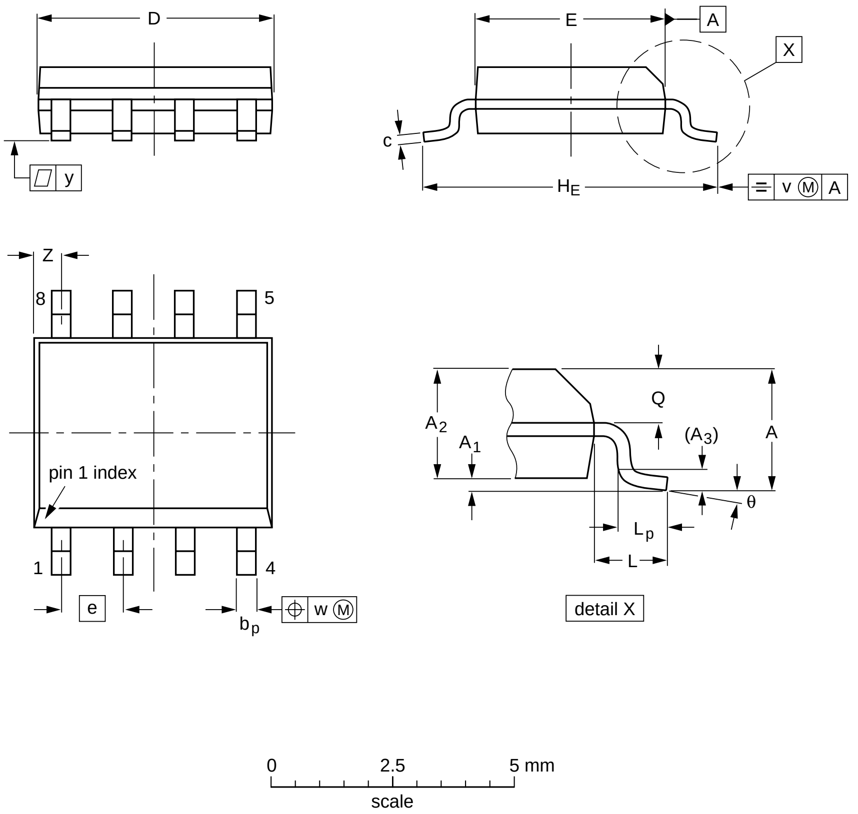
11.2.1.1 Example maximum frequency

Question — We need to make the PLL area of a new line card backwards compatible and need to need to convert one GTL signal to LVTTL, invert it, and convert it back to GTL. The signal we want to convert is random in nature but will mostly be around 19 MHz with very long periods of inactivity where either a HIGH or LOW state will be maintained. The traces are 1 or 2 inches long with trace capacitance of about 2 pF per inch.

Answer — The frequency of the PCA9306 is limited by the capacitance of the part, the capacitance of the traces and the pull-up resistors used. The limiting case is probably the LOW-to-HIGH transition in the GTL to LVTTL direction, and there the use of the lowest acceptable resistor values will minimize the rise time delay. Assuming 50 pF capacitance and 220 Ω resistance, the RC time constant is 11 ns (50 pF × 220 Ω). With 19 MHz corresponding to 50 ns period the PCA9306 will support this application.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

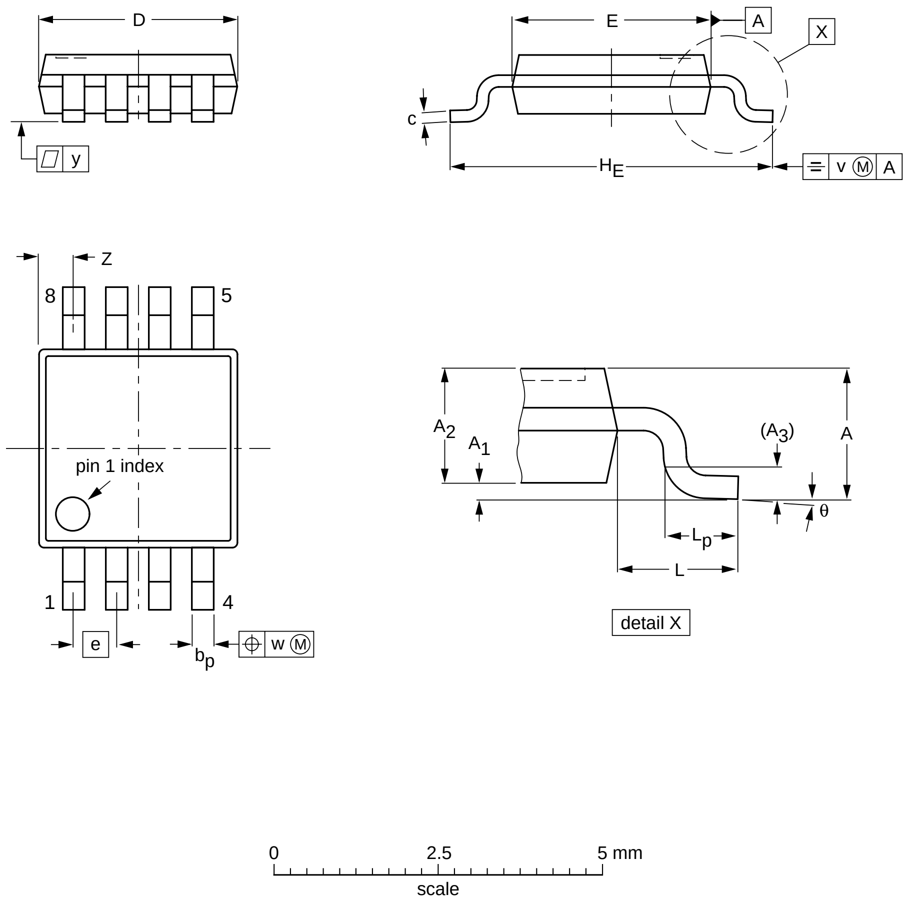
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

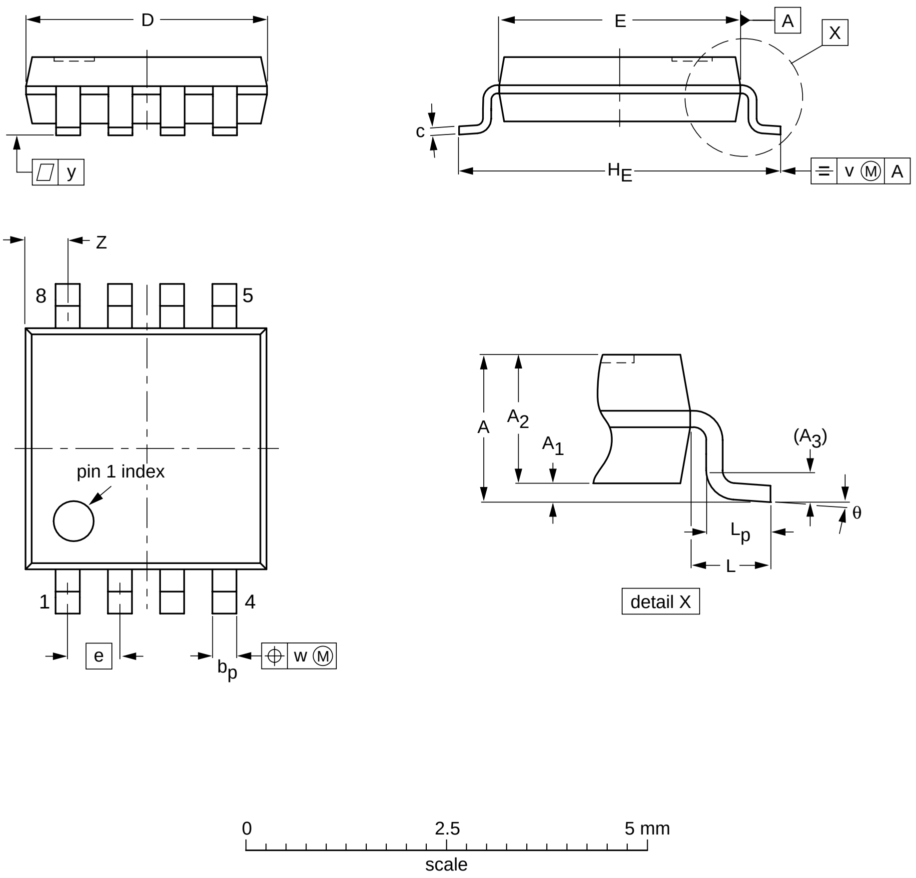
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 12. Package outline SOT505-1 (TSSOP8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

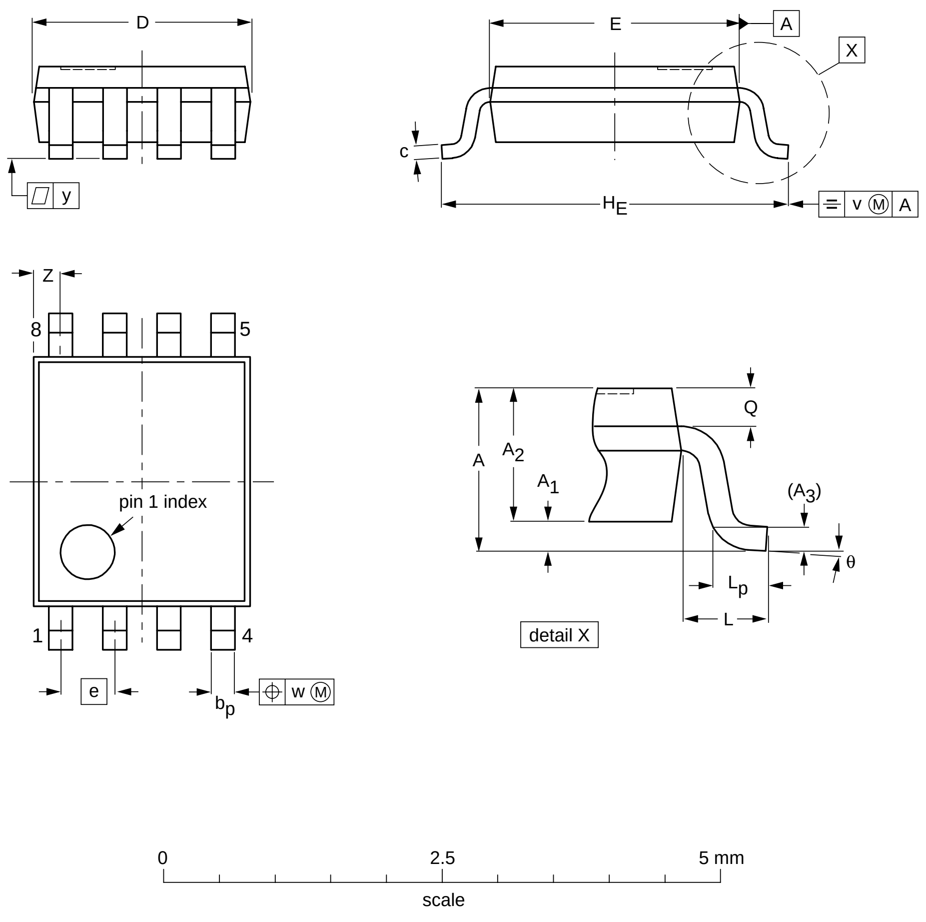
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 13. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

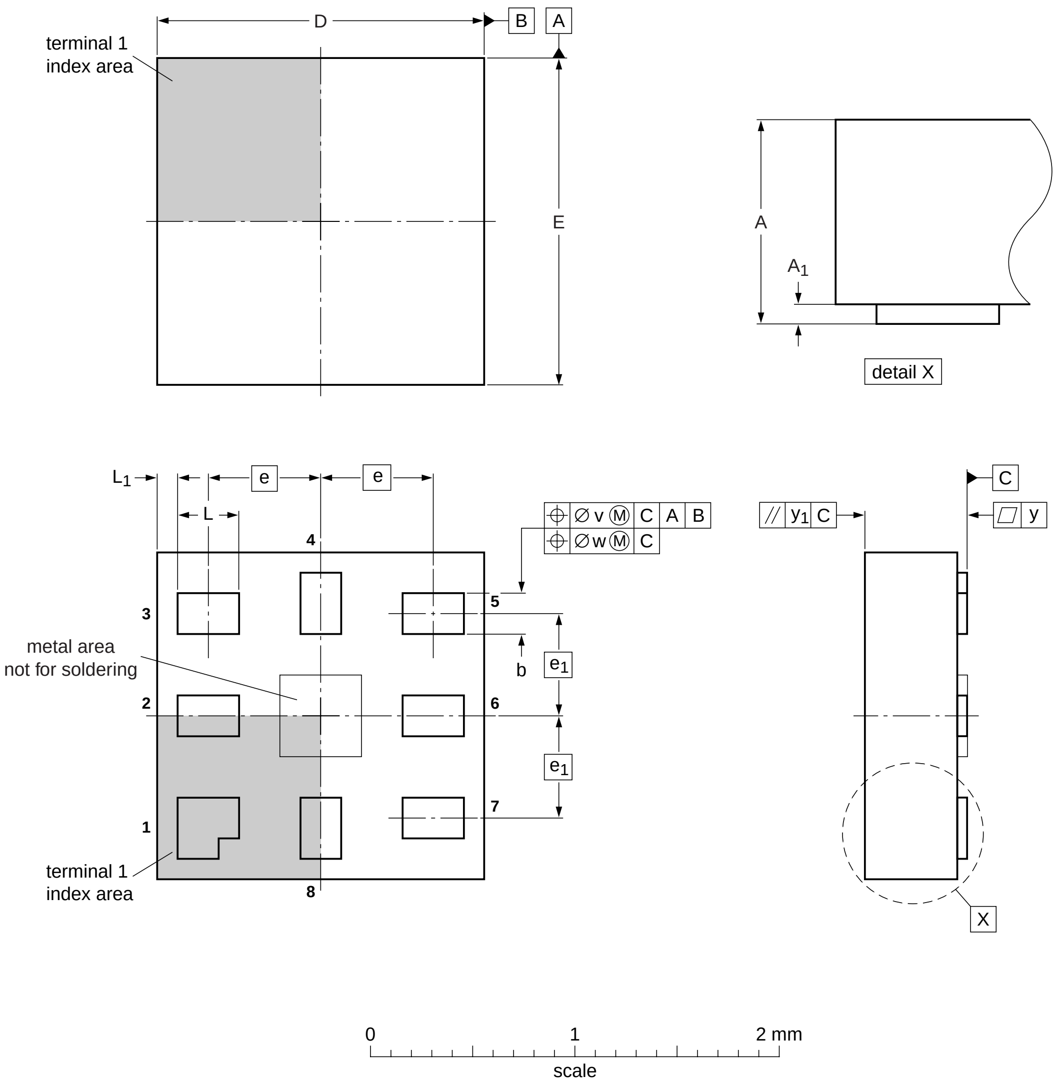
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 14. Package outline SOT765-1 (VSSOP8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT902-1	- - -	MO-255	- - -			~~05-11-25~~ 07-11-14

Fig 15. Package outline SOT902-1 (XQFN8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

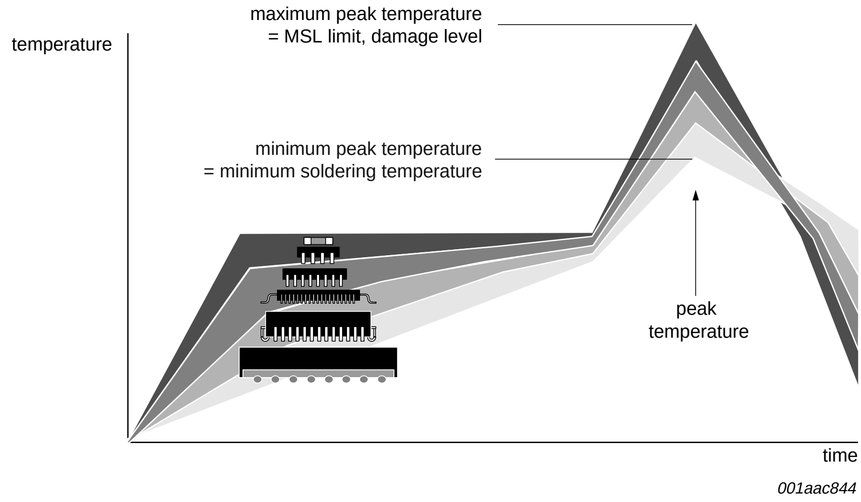
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
MM	Machine Model
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network
SMBus	System Management Bus

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9306_4	20091026	Product data sheet	-	PCA9306_3
Modifications:	• Section 1 "General description": – 1st paragraph: changed from "... operational from 1.1 V to 3.6 V ($V_{ref(1)}$) and 1.8 V to 5.5 V ($V_{bias(ref)(2)}$)" to "... operational from 1.0 V to 3.6 V ($V_{ref(1)}$) and 1.8 V to 5.5 V ($V_{bias(ref)(2)}$)". – 2nd paragraph, 1st sentence: changed from "... between 1.2 V and 5 V" to "... between 1.0 V and 5 V" – 3rd paragraph: deleted first 2 sentences; added (new) last sentence. – 5th paragraph: added (new) last sentence. • Section 2 "Features": – 4th bullet item, 2nd sub-bullet: added 1.8 V $V_{bias(ref)(2)}$ – 10th bullet item re-written • Table 1 "Ordering information": – Topside mark for PCA9306DC1 changed from "306U" to "P06" • updated soldering information			
PCA9306_3	20080804	Product data sheet	-	PCA9306_2
PCA9306_2	20070221	Product data sheet	-	PCA9306_1
PCA9306_1	20061020	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 October 2009

Document identifier: PCA9306_4