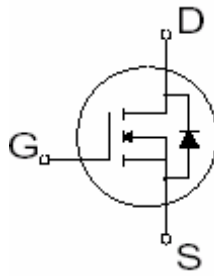


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



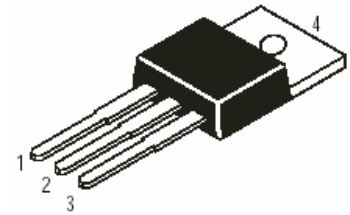
$$V_{DSS} = 600V$$

$$I_{D25} = 7.5A$$

$$R_{DS(ON)} = 1.2 \Omega$$

### Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate  
Pin2-Drain  
Pin3-Source

### Application

- Switching application

### Absolute Maximum Ratings

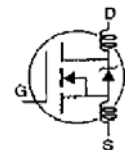
	Parameter	Max.	Units
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}@10V$	7.5	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}@10V$	4.6	
$I_{DM}$	Pulsed Drain Current ①	30	
$P_D@T_C=25^\circ C$	Power Dissipation	150	W
	Linear Derating Factor	1.18	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	230	mJ
$I_{AR}$	Avalanche Current ①	7.5	A
$E_{AR}$	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.8	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +175	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	0.9	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

**Electrical Characteristics @T<sub>J</sub>=25 °C(unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	600	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp.Coefficient	—	0.06	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-resistance	—	1.0	1.2	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =3.8A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	7.5	8.8	—	S	V <sub>DS</sub> =40V, I <sub>D</sub> =3.8A
I <sub>DSS</sub>	Drain-to-Source Leakage current	—	—	25	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V
		—	—	250		V <sub>DS</sub> =480V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse leakage	—	—	-100		V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	36	nC	I <sub>D</sub> =7.5A V <sub>DS</sub> =480V V <sub>GS</sub> =10V See Fig.6 and 13④
Q <sub>gs</sub>	Gate-to-Source charge	—	—	5.5		
Q <sub>gd</sub>	Gate-to-Drain("Miller") charge	—	—	20		
t <sub>d(on)</sub>	Turn-on Delay Time	—	45	—	nS	V <sub>DD</sub> =300V I <sub>D</sub> =3.8A R <sub>G</sub> =25Ω
t <sub>r</sub>	Rise Time	—	130	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	170	—		
t <sub>f</sub>	Fall Time	—	71	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1250	—	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz See Figure 5
C <sub>oss</sub>	Output Capacitance	—	138	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	18	—		


**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	7.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	30		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.4	V	T <sub>J</sub> =25°C, I <sub>S</sub> =7.5A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	250	nS	T <sub>J</sub> =25°C, I <sub>F</sub> =7.5A
Q <sub>rr</sub>	Reverse Recovery Charge	—	3.5	—	nC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> + L <sub>D</sub> )				

## Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature(see figure 11)
- ② L = 7.3mH, I<sub>AS</sub> = 7.5 A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
- ③ I<sub>SD</sub> ≤ 7.5A, di/dt ≤ 200A/μS, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 25°C
- ④ Pulse width ≤ 300 μS; duty cycle ≤ 2%