VIV0102THJ

VTM™
DC to DC
Voltage Transformation

FEATURES

- 38.4 Vdc – 1.2 Vdc 50 A Voltage Transformation Module
  - Operating from standard 48 V or 24 V PRMs
- High efficiency (>89%) reduces system power consumption
- High density (334 A/in³)
- "Half Chip" V•I Chip package enables surface mount, low impedance interconnect to system board
- Contains built-in Protection features:
  - Overvoltage lockout
  - Overcurrent
  - Short circuit
  - Over temperature protection
- Provides enable/disable control, internal temperature monitoring, current monitoring
- ZVS/ZCS resonant Sine Amplitude Converter topology

TYPICAL APPLICATION

- High End Computing Systems
- Automated Test Equipment
- Telecom Base Stations
- High Density Power Supplies
- Communication Systems

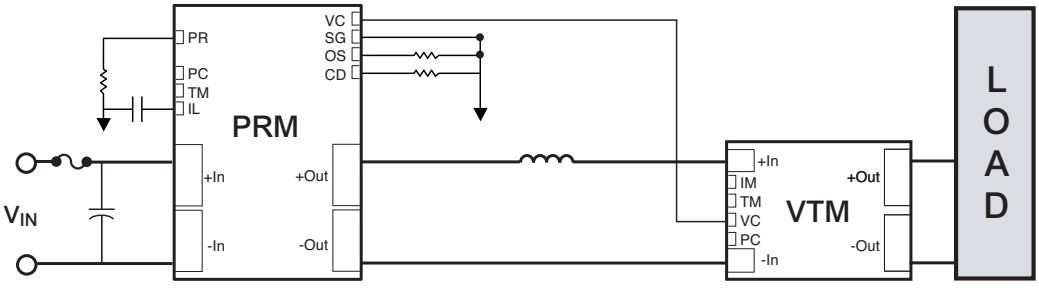
DESCRIPTION

The V•I Chip Voltage Transformation Module is a high efficiency (>89%) Sine Amplitude Converter (SAC)™ operating from a 26 to 55 Vdc primary bus to deliver an isolated 1.2 V secondary. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators, which means that capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the K factor of the VIV0102THJ is 1/32, that capacitance value can be reduced by a factor of 1,024x, resulting in savings of board area, materials and total system cost.

The VIV0102THJ is provided in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip package provides flexible thermal management through its low junction-to-case and junction-to-board thermal resistance. With high conversion efficiency the VIV0102THJ increases overall system efficiency and lowers operating costs compared to conventional approaches.
The VIV0102THJ enables the utilization of Factorized Power Architecture providing efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

V_{IN} = 26 – 55 V	I_{OUT} = 50 A(NOM)
V_{OUT} = 0.81 – 1.72 V (NO LOAD)	K = 1/32

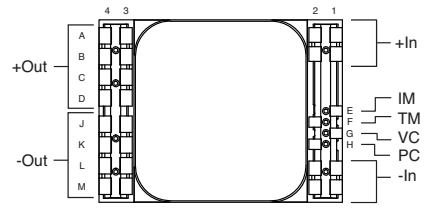
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

+IN to –IN . . . . . -1.0 Vdc – +60 Vdc
PC to –IN . . . . . -0.3 Vdc – +20 Vdc
TM to –IN . . . . . -0.3 Vdc – +7.0 Vdc
+IN/-IN to +OUT/-OUT . . . . . 2250 V (Hi Pot)
+IN/-IN to +OUT/-OUT . . . . . 60 V (working)
+OUT to –OUT . . . . . -1.0 Vdc – +4 Vdc
Temperature during reflow . . . . . 225°C (MSL5)

PACKAGE ORDERING INFORMATION



Bottom View

Signal Name	Designation
+In	A1-B1, A2-B2
–In	L1-M1, L2-M2
IM	E1
TM	F2
VC	G1
PC	H2
+Out	A3-D3, A4-D4
–Out	J3-M3, J4-M4

PART NUMBER	DESCRIPTION
VIV0102THJ	-40°C – 125°C T_J, J lead
VIV0102MHJ	-55°C – 125°C T_J, J lead

CONTROL PIN SPECIFICATIONS

See section 5.0 for further application details and guidelines.

PC (V•I Chip VTM Primary Control)

The PC pin can enable and disable the VTM. When held below 2.0 V the VTM will be disabled. When allowed to float with an impedance to –IN of greater than 60 kΩ the module will start. The PC pin is capable of being driven high either by an external logic signal or internal pull up to 5 V (operating).

TM (V•I Chip VTM Temperature Monitor)

The TM pin monitors the internal temperature of the VTM within an accuracy of ±5 °C. It has a room temperature setpoint of ~3.0 V and an approximate gain of 10 mV/°C. It can source up to 100 µA and may also be used as a "Power Good" flag to verify that the VTM is operating.

IM (V•I Chip Current Monitor)

The IM pin provides a DC analog voltage proportional to the output current of the VTM. This voltage varies between 0.4 and 2.4 V and represents VTM output current within 25% of the actual value under all operating line temperature conditions between 50% and 100% load.

VC (VTM Control)

In typical applications the VC pin of the VTM is tied to the VC pin of the PRM™ Regulator. In these applications the PRM provides a temporary VC voltage during startup synchronizing the output rise of the two devices. In addition, the VC port provides feedback to the PRM on its output resistance through an internal resistor.

For applications which do not use a PRM, a voltage between 12 V and 17 V must be applied to VC in order to enable the VTM.

1.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Voltage range	V_{IN}	No external VC applied	**26**		**55**	Vdc
dV/dt	dV_{IN}/dt				**1**	V/µs
No load power dissipation	P_{NL}	V_{IN} = 42 V		2.6	**4.6**	W
		V_{IN} = 26 V to 55 V			**5.4**	W
Inrush Current Peak	I_{INR-P}	VC enable, V_{IN} = 42 V C_{OUT} = 2,500 µF, I_{OUT} = 50 A		2.5	**10**	A
DC Input Current	I_{IN-DC}				**1.8**	A
K Factor $\left(\frac{V_{OUT}}{V_{IN}}\right)$	K			1/32		V/V
Output Current(average)	$I_{OUT-AVG}$				**50**	A
Output Current(Peak)	I_{OUT-PK}	T_{PEAK} <10 ms, I_{OUT_AVG} ≤ 50 A			**75**	A
Output Power (average)	$P_{OUT-AVG}$	I_{OUT_AVG} ≤ 50 A			**80**	W
Output Voltage	V_{OUT}	Section 3.0	**0.60**		**1.75**	V
Efficiency (Ambient)	η_{AMB}	V_{IN} = 42 V, T_J =25°C, I_{OUT} = 50 A	83.5	86.1		%
		V_{IN} = 26 V to 55 V, T_J = 25°C I_{OUT} = 50 A	77.5			
Efficiency (Hot)	η_{HOT}	V_{IN} = 42 V, TJ = 100° C, I_{OUT} = 50 A	84	85.5		%
Efficiency (Over load range)	$\eta_{20\%}$	10 A < I_{OUT} < 50 A	**77**			%
Output Resistance (Ambient)	$R_{OUT-AMB}$	T_J = 25°C	1.9	2.7	3.5	mΩ
Output Resistance (Hot)	$R_{OUT-HOT}$	T_J = 125°C	2.2	3.2	4.1	mΩ
Output Resistance (Cold)	$R_{OUT-COLD}$	T_J = -40°C	1.6	2.3	3	mΩ
Load Capacitance	C_{OUT}	VTM Standalone Operation. V_{IN} pre-applied, VC enable			**2,500**	µF
Switching Frequency	F_{SW}		**1.35**	1.48	**1.60**	MHz
Ripple Frequency	F_{SW-RP}		**2.70**	2.96	**3.20**	MHz
Output Voltage Ripple	V_{OUT-PP}	C_{OUT} = 0 µf, I_{OUT} = 50 A V_{IN} = 42 V, 20 MHz BW, Section 8.0		155	**350**	mV
PC						
PC Voltage (Operating)	V_{PC}		**4.7**	5	**5.3**	V
PC Voltage (Enable)	V_{PC-EN}		**2**	2.5	**3**	V
PC Voltage (Disable)	V_{PC-DIS}				**2**	V
PC Source Current (Startup)	I_{PC-EN}		**50**	100	**300**	µA
PC Source Current (Operating)	I_{PC-OP}				**2**	mA
PC Resistance (Internal)	R_{PC-INT}	Internal pull down resistor	**50**	150	**400**	kΩ
PC Resistance (External)	R_{PC-EXT}	Connected to –IN. Unit will not start if below minimum value	**60**			kΩ
PC Capacitance (Internal)	C_{PC-INT}	Section 5.0			**560**	pF
PC Disable Time	T_{PC-DIS}			4		µs
PC Fault Response Time	T_{FR-PC}	From fault to PC = 2.0 V		100		µs
TM						
TM Voltage (Ambient)	V_{TM-AMB}	T_J = 27°C	**2.95**	3	**3.05**	V
TM Gain	A_{TM}			10		mV/°C
TM Source Current	I_{TM}				**100**	µA
TM Resistance (Internal)	R_{TM-INT}	Internal pull down resistor	**25**	40	**50**	kΩ
TM Capacitance (External)	C_{TM-EXT}				**50**	pF

1.0 ELECTRICAL CHARACTERISTICS (CONT.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
TM (CONT.)						
TM Voltage Ripple	V_{TM-PP}	C_{TM} = 0 µF, V_{IN} = 42 V, I_{OUT} = 50 A, 20 MHz BW		120	**200**	mV
TM Fault Response Time	T_{FR-TM}	From fault to TM = 1.5 V		10		µs
IM						
IM Voltage (No Load)	V_{IM-NL}	T_J = 25°C, V_{IN} = 42 V, I_{OUT} = 0	0.4	0.57	0.72	V
IM Voltage (50%)	$V_{IM-50\%}$	T_J = 25°C, V_{IN} = 42 V, I_{OUT} = 25 A		1.2		V
IM Voltage (Full Load)	V_{IM-FL}	T_J = 25°C, V_{IN} = 42 V, I_{OUT} = 50 A		2.0		V
IM Gain	A_{IM}	T_J = 25°C, V_{IN} = 42 V, I_{OUT} > 25 A		16		mV/A
IM Resistance (External)	R_{IM-EXT}		**2.5**			MΩ
VC						
External VC Voltage	V_{VC-EXT}	Required for startup, and operation below 26 V. See Section 5.0	**12**		**17**	V
VC Slew Rate	dVC/dt	Required for proper startup	**0.0025**		**0.25**	V/µs
VC Current Draw (steady-state)	I_{VC}	VC = 14 V, V_{IN} = 0		75	**150**	mA
VC Inrush Current	I_{INR-VC}	VC = 17 V, dVC/dt = 0.25 V/µs			**750**	mA
Internal VC Capacitance	C_{VC-INT}	VC = 0 V		2.2		µF
Output Turn-On Delay (VC)	T_{ON}	V_{IN} pre-applied, PC floating, VC enable, C_{PC} = 0 µF, C_{OUT} = 2,500 µF			**500**	µs
VC to PC Delay	T_{VC-PC}	VC = 10.5 V to PC high, V_{IN} = 0 V, dVC/dt = 0.25 V/µs		10	**25**	µs
VC Application Time	T_{VC-AP}	Maximum application time of VC			20	ms
VC Internal Resistor	R_{VC-INT}			14.3		kΩ
PROTECTION						
Positive Going OVLO	V_{IN_OVLO+}		**55.5**	57.7	**59.8**	V
UV Turn-Off	V_{IN_UVTO}	No external VC applied, I_{OUT} = 50 A		16.2	**26**	V
Output Overcurrent Trip	I_{OCP}		**60**		**100**	A
Short Circuit Protection Trip Current	I_{SCP}		**60**		**120**	A
Thermal Shutdown Setpoint	T_{J-OTP}		125	130	135	°C
Output Overcurrent Response Time Constant	T_{OCP}	Effective internal RC filter		3.8		ms
Short Circuit Protection Response Time	T_{SCP}	From detecton to cessation of switching		1		µs
Overvoltage Lockout Response Time Constant	T_{OVLO}	Effective internal RC filter		2.4		µs
GENERAL SPECIFICATION						
Isolation Voltage (Hi-Pot)	V_{HIPOT}		**2,250**			VDC
Working Voltage (IN – OUT)	V_{IN-OUT}				**250**	V
Isolation Capacitance	C_{IN-OUT}	Unpowered Unit	**270**	**340**	**410**	pF
Isolation Resistance	R_{IN-OUT}		**10**			MΩ
MTBF		**MIL HDBK 217F, 25°C, Ground Benign**		4.5		MHrs
Agency Approvals / Standards		cTUVus				
		CE Mark				
		ROHS 6 of 6				

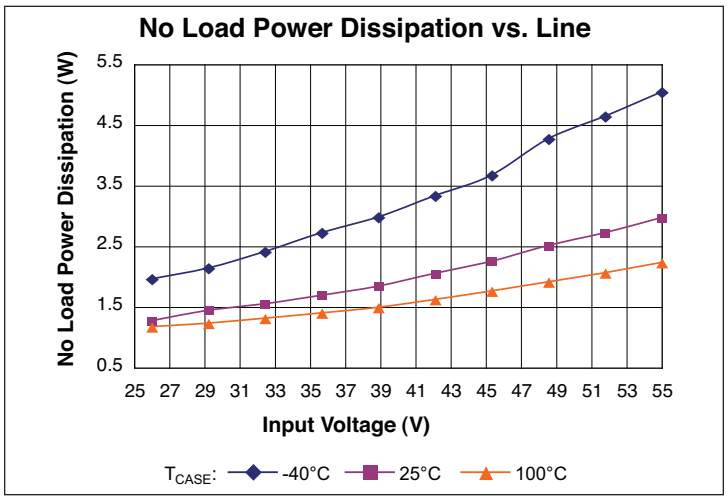


Figure 1 – *No load power dissipation vs. V_{IN}; T_{CASE}*

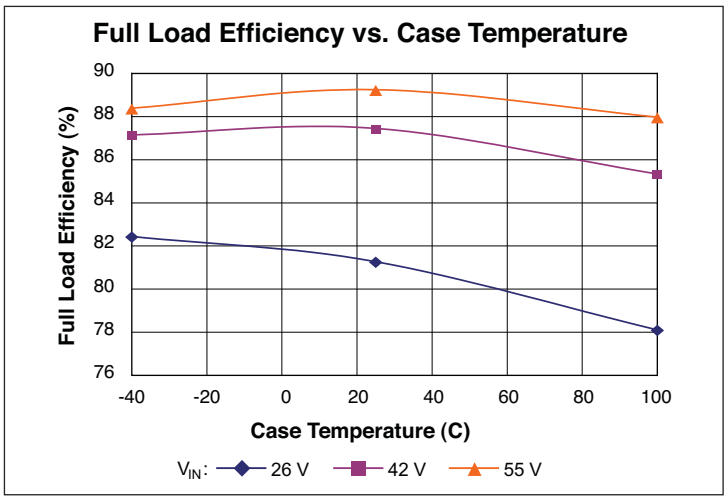


Figure 2 – *Full load efficiency vs. temperature; V_{IN}*

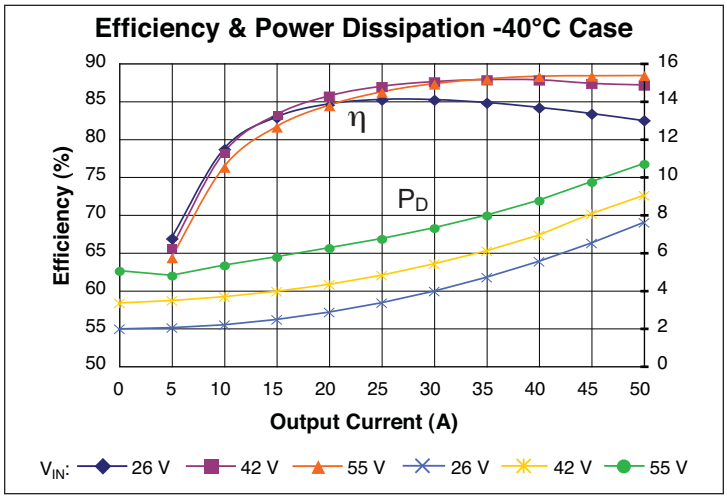


Figure 3a – *Efficiency and power dissipation at -40°C (case); V_{IN}*

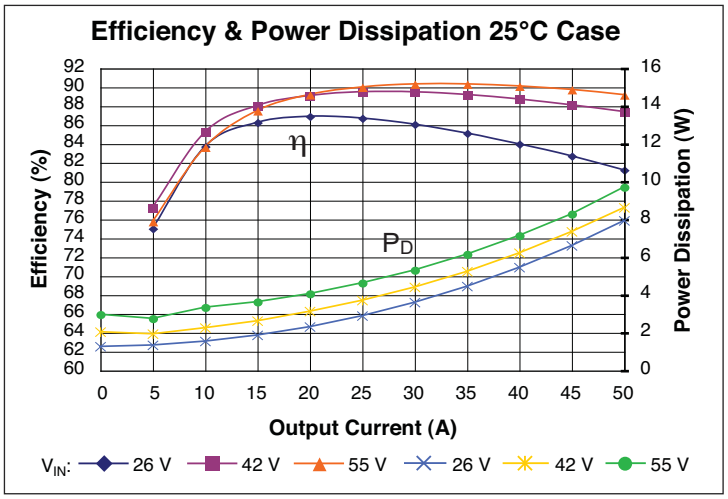


Figure 3b – *Efficiency and power dissipation at 25°C (case); V_{IN}*

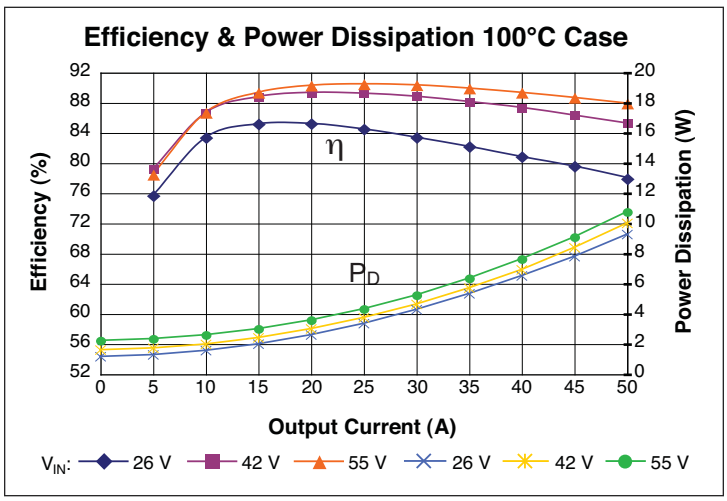


Figure 3c – *Efficiency and power dissipation at 100°C (case); V_{IN}*

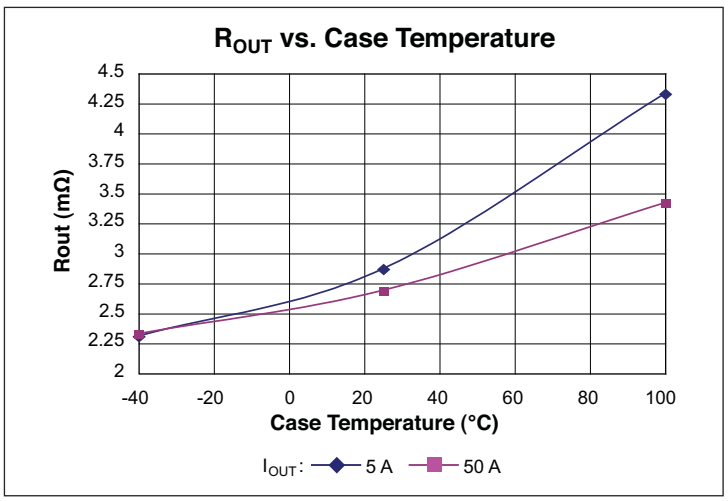


Figure 4 – *R_{OUT} vs. temperature vs. I_{OUT}*

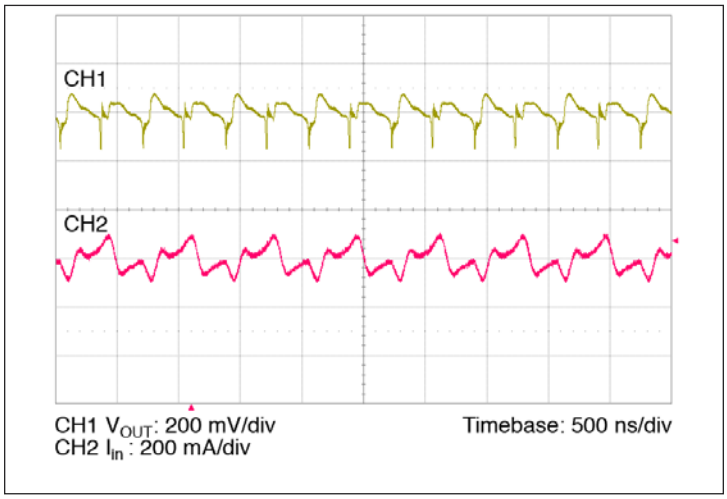


Figure 5 – *Full load ripple, 100 µF C_{IN}; No external C_{OUT}*

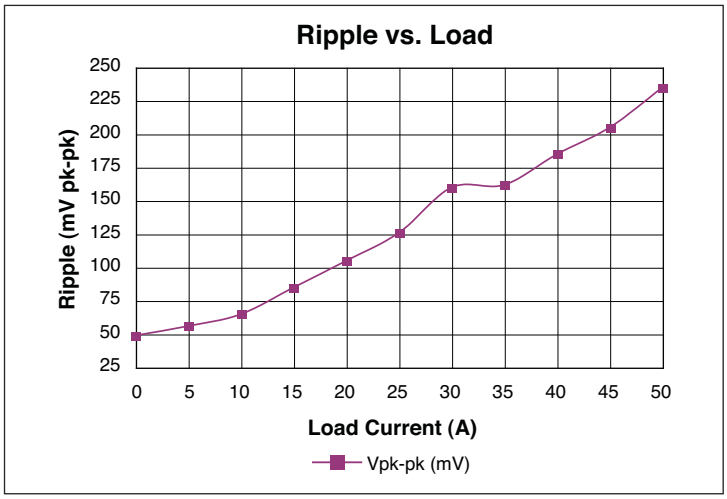


Figure 6 – *Vripple vs. I_{OUT} ; 42 V_{IN}, no external output capacitance*

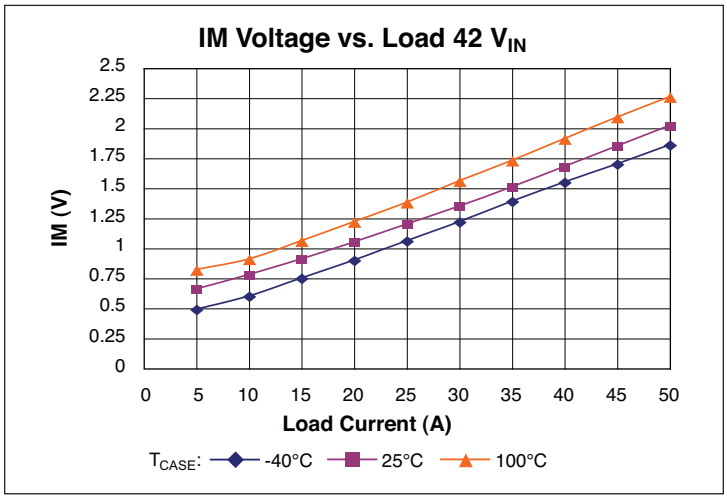


Figure 7 – *IM voltage vs. load; 42 V_{IN}*

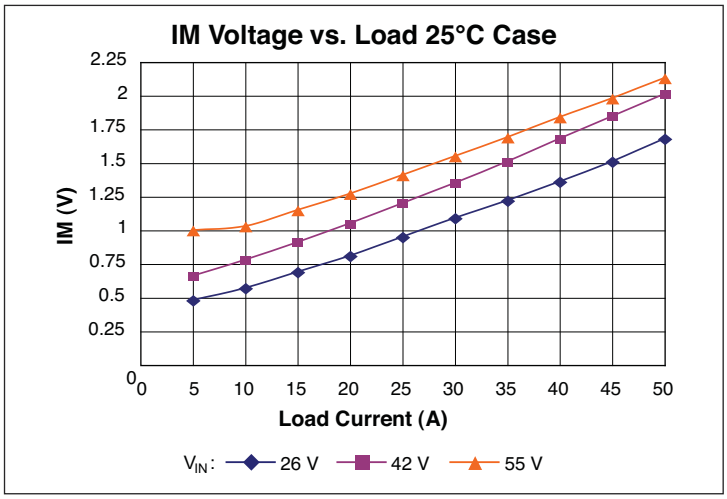


Figure 8 – *IM voltage vs. load; 25°C Case*

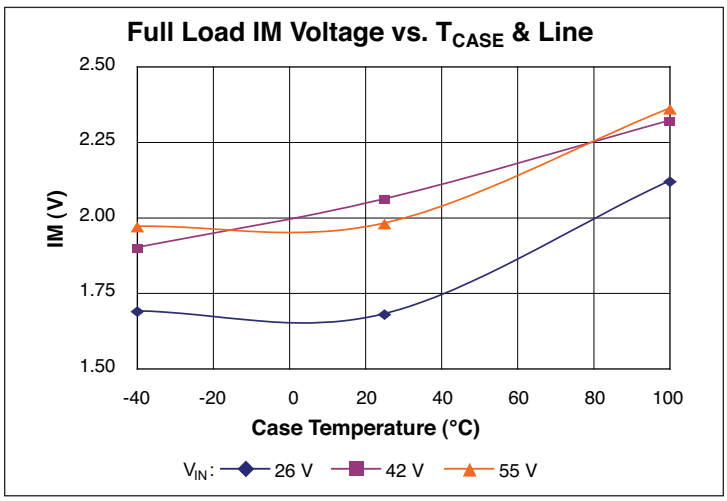


Figure 9 – *Full load IM voltage vs. T_{CASE} & line*

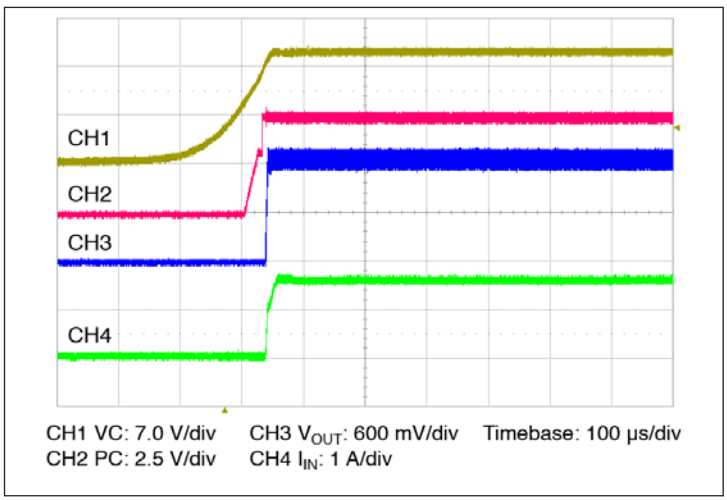


Figure 10 – *Start up from application of VC; V_{IN} pre-applied*
No external C_{OUT}

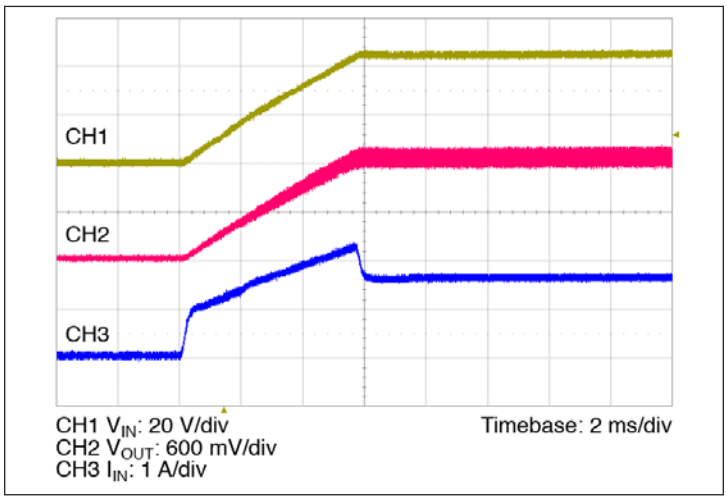


Figure 11 – *Start up from application of V_{IN}; VC pre-applied No external C_{OUT}*

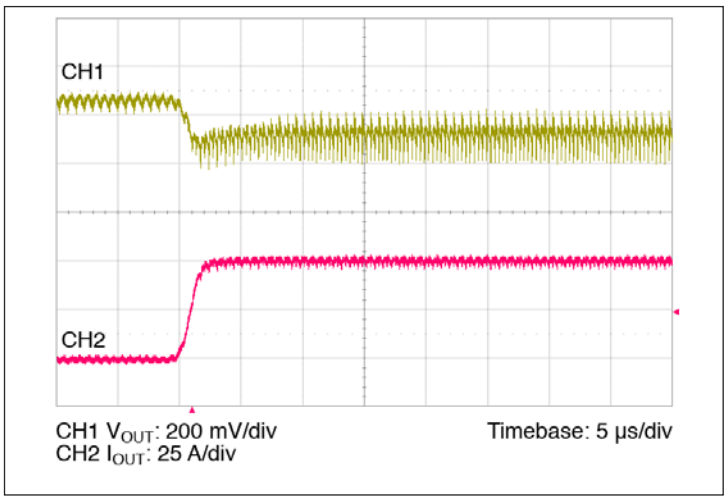


Figure 12 – *0 – 50 A transient response; C_{IN} = 100 µF, no external C_{OUT}*

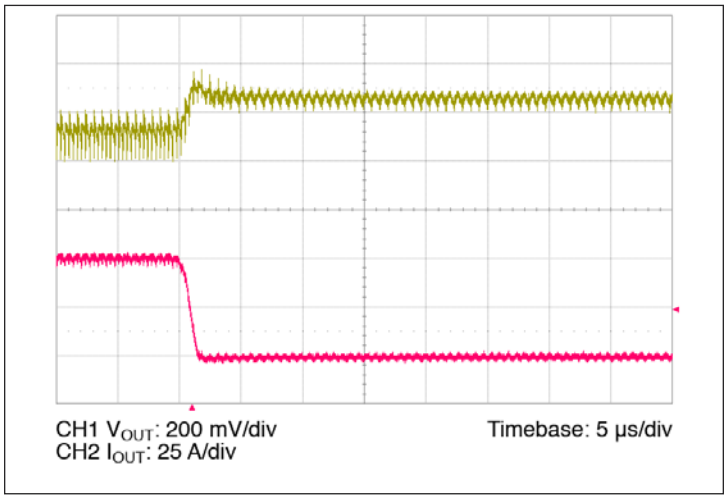


Figure 13 – *50 A – 0 A transient response; C_{IN} = 100 µF, no external C_{OUT}*

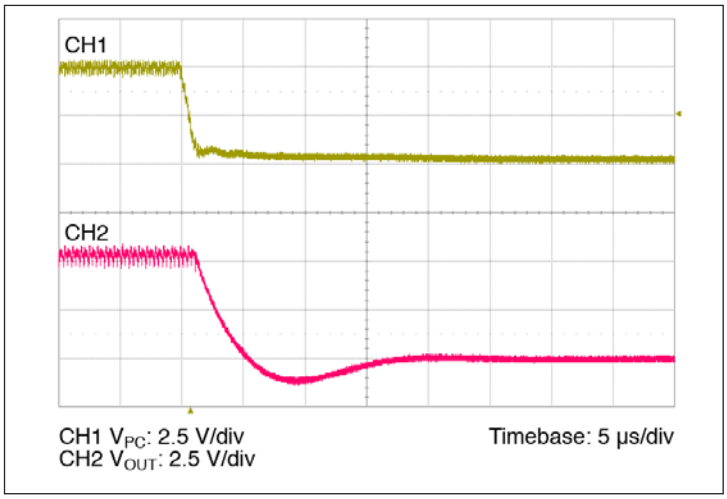


Figure 14 – *PC disable waveform; R_{LOAD} = 0.025 Ω, No external C_{OUT}*

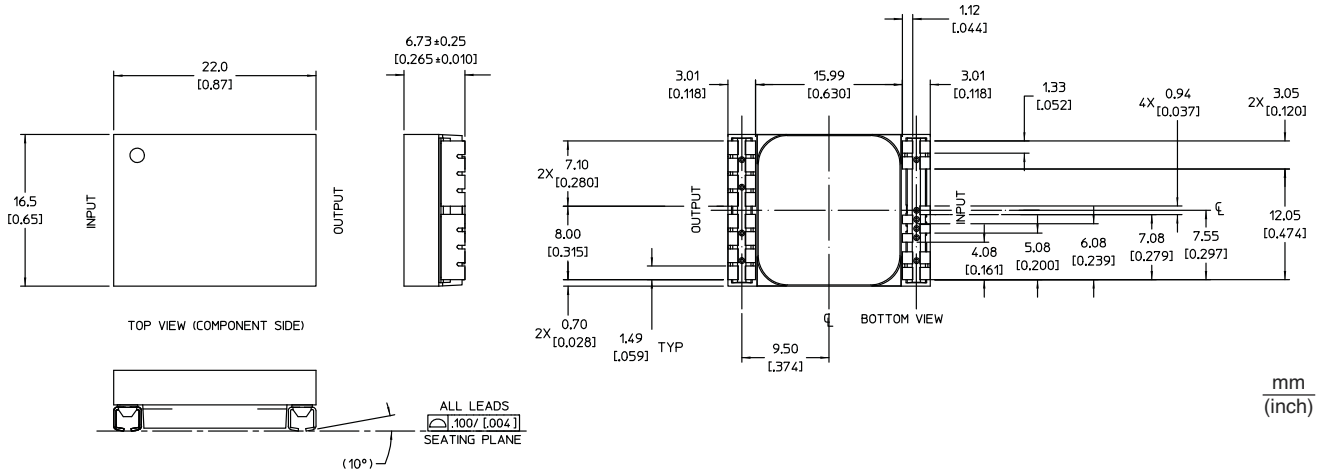
2.0 PACKAGE/MECHANICAL SPECIFICATIONS

All specifications are at **T_J=25°C** unless otherwise noted. See associated figures for general trend data.

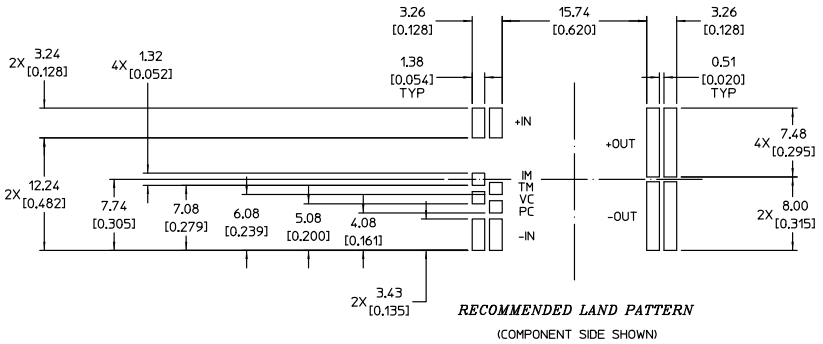
ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Length	L		21.7 / 0.85	22.0 / 0.87	22.3 / 0.88	mm/in
Width	W		16.4 / 0.64	16.5 / 0.65	16.6 / 0.66	mm/in
Height	H		6.48 / 0.255	6.73 / 0.265	6.98 / 0.275	mm/in
Volume	Vol	No Heatsink		2.44 / 0.150		cm^3/in^3
Footprint	F	No Heatsink		3.6 / 0.56		cm^2/in^2
Current Density	CD	No Heatsink		334		A/in^3
Weight	W			0.28/8		oz/g
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	µm
		Gold	0.003		0.05	µm
Operating Temperature (Junction)	T_J	VIV0102THJ (T-Grade)	-40		125	°C
		VIV0102MHJ (M-Grade)	-55		125	°C
Storage Temperature	T_{ST}	VIV0102THJ (T-Grade)	-40		125	°C
		VIV0102MHJ (M-Grade)	-65		125	°C
Thermal Impedance	$Ø_{JC}$	JUNCTION TO CASE			2.7	°C/W
Thermal Capacity				5		Ws/°C
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-leads only		2.5	3.0	lbs
Moisture Sensitivity Level		MSL Level 5	5			
ESD Rating	ESD_{HBM}	Human Body Model[a]	1500			V_{DC}
	ESD_{MM}	Machine Model[b]	400			V_{DC}
Peak Temperature During Reflow					225	°C
Peak Time Above 183°C					150	s
Peak Heating Rate During Reflow				1.5	3	°C/s
Peak Cooling Rate Post Reflow				1.5	6	°C/s

[a] JEDEC JESD 22-A114C.01
[b] JEDED JESD 22-A115-A

2.1 MECHANICAL DRAWING

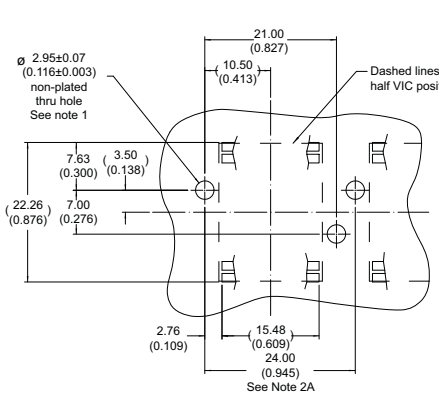


2.2 RECOMMENDED LAND PATTERN

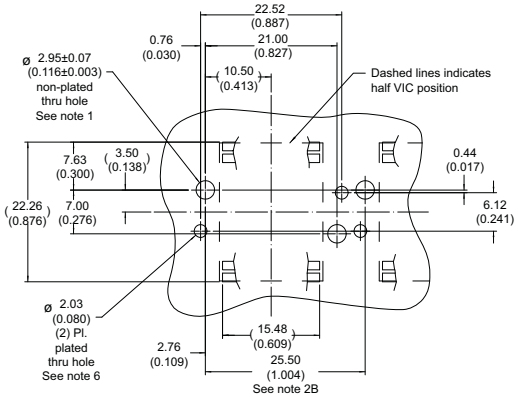


2.3 RECOMMENDED LAND PATTERN FOR PUSH PIN HEATSINK

Notes:
1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.
2. (A) minimum recommended pitch is 24.00 (0.945) this provides 7.50 (0.295) component edge–to–edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
(B) Minimum recommended pith is 25.50 (1.004). This provides 9.00 (0.354) component edge–to–edge spacing, and 2.00 (0.079) clearence between Vicor heat sinks.
3. V•I Chip land pattern shown for reference only, actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all half size V•I Chips.
4. RoHS complient per CST–0001 latest revision.
5. Unless otherwise specified:
Dimensions are mm (inches)
tolerances are:
x.x (x.xx) = ±0.13 (0.01)
x.xx (x.xxx) = ±0.13 (0.005)
6. Plated through holes for grounding clips (33855) shown for reference, Heatsink orientation and device pitch will dictate final grounding solution.



(NO GROUNDING CLIPS)



(WITH GROUNDING CLIPS)

3.0 POWER, VOLTAGE, EFFICIENCY RELATIONSHIPS

Because of the high frequency, fully resonant SAC topology, power dissipation and overall conversion efficiency of VTM converters can be estimated as shown below.

Key relationships to be considered are the following:

1. Transfer Function

   a. No load condition

   $V_{OUT} = V_{IN} \bullet K$ Eq. 1

   Where K (transformer turns ratio) is constant for each part number

   b. Loaded condition

   $V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT}$ Eq. 2

2. Dissipated Power
   The two main terms of power losses in the VTM module are:

   - No load power dissipation (P_{NL}) defined as the power used to power up the module with an enabled power train at no load.
   - Resistive loss (R_{OUT}) refers to the power loss across the VTM modeled as pure resistive impedance.

   $P_{DISSIPATED} \approx P_{NL} + P_{R_{OUT}}$ Eq. 3

Therefore, with reference to the diagram shown in Figure 15

$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}}$ Eq. 4

Notice that R_{OUT} is temperature and input voltage dependent and P_{NL} is temperature dependent (See Figure 15).

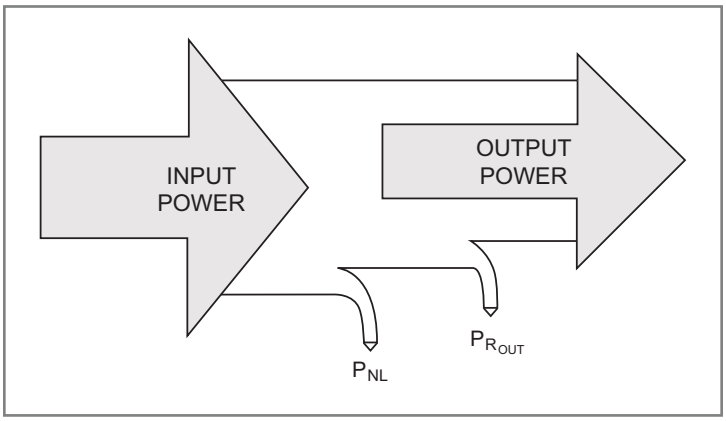


Figure 15 – *Power transfer diagram*

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} = \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} = 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} \right) \quad \text{Eq. 5}$$

4.0 OPERATING

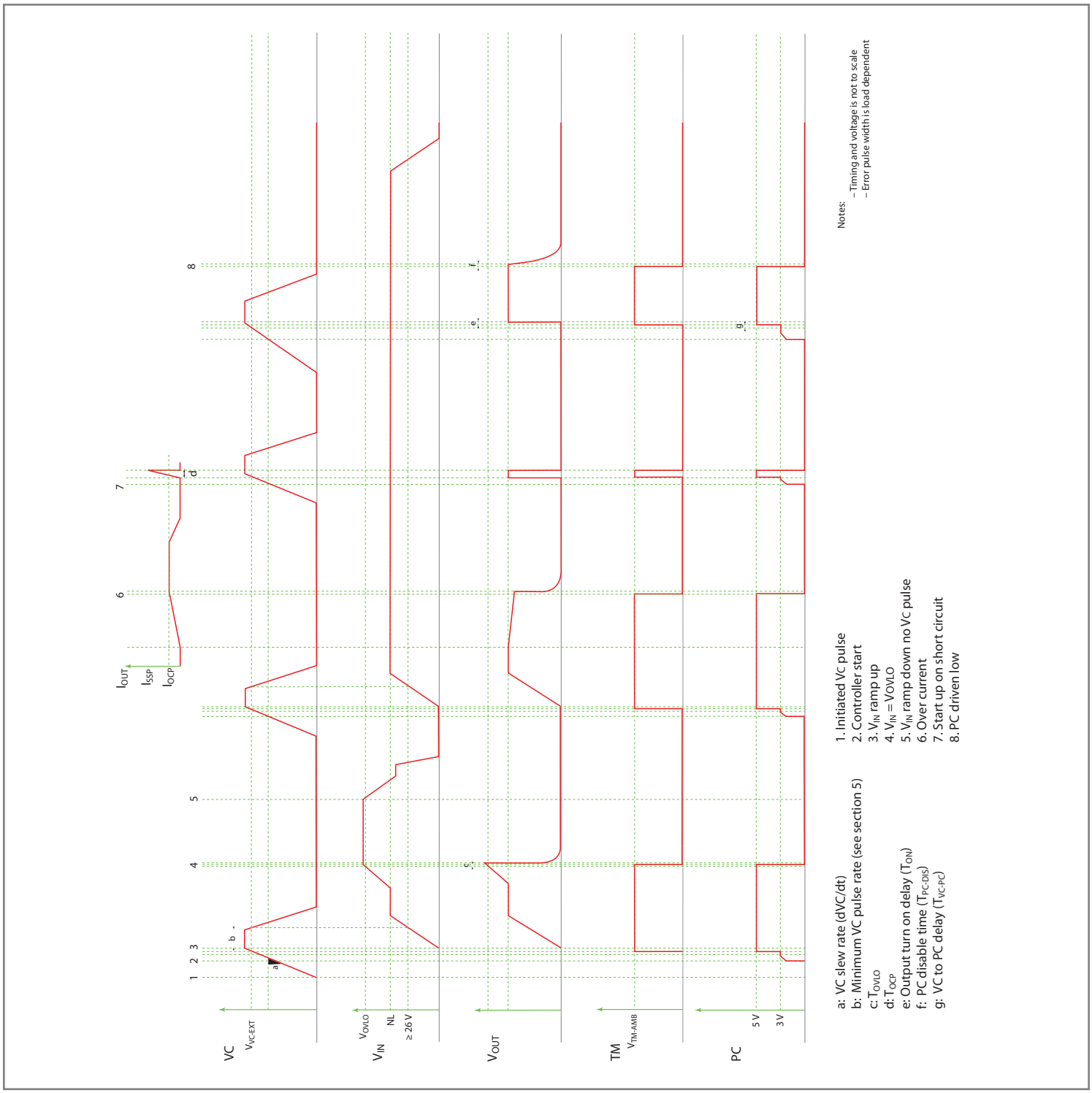


Figure 16 – *Timing diagram*

5.0 USING THE CONTROL SIGNALS VC, PC, TM, IM

The VTM Control VC pin is an input pin which powers the internal VCC circuitry when within the specified voltage range of 12 V to 17 V. This voltage is required in order for the VTM to start, and must be applied as long as the input is below 26 V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range. Depending on the sequencing of the VC with respect to the input voltage, the behavior during startup will vary as follows:

- **Normal Operation (VC applied prior to V_{IN}):** In this case the controller is active prior to the input. When the input voltage is applied, the VTM output voltage will track the input allowing for a soft start (See Figure 11). If the VC voltage is removed prior to the input reaching 26 V, the VTM will shut down.
- **Stand Alone Operation (VC applied after V_{IN}):** In this case the VTM output will begin to rise upon the application of the VC voltage (See Figure 10). The output rate of rise will vary depending on the amount of output capacitance in order to limit the inrush current. In this mode of operation, the maximum output capacitance is 1,000 µF due to limitations of the inrush limiting circuitry.

Some additional notes on the using the VC pin:

- In most applications, the VTM will be powered by an upstream PRM, in which case the PRM will provide a 10 ms VC pulse during startup. In these applications the VC pins of the PRM and VTM should be tied together.
- The fault response of the VTM is latching. A positive edge on VC is required in order to restart the unit.
- The VTM is not designed for continuous operation with VC applied. The VC voltage must be removed within 20 ms of application.
- The VIV0102THJ is not capable of reverse operation during startup. If a voltage is present at the output of the VTM which satisfies the condition

$$V_{OUT} > V_{IN} \bullet K$$

at the time the VC voltage is applied, then the device will not start. Once the unit is running it is capable of processing power in the reverse direction as long as the input and output voltages are within the specified range.
The VIV0102THJ is not qualified for continuous operation in the reverse direction.

The Primary Control (PC) pin can be used to accomplish the following functions:

- **Delayed start:** Upon the application of VC, the PC pin will source a constant 100 µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start
- **Auxiliary voltage source:** Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5 V, 2 mA voltage source
- **Output Disable:** PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 850 Ω.
- **Fault detection flag:** The PC 5V voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of PC signal. It is important to notice that PC doesn't have current sink capability (only 150 kΩ pull down is present), therefore in an array PC line will not be capable of disabling all the modules if a fault is detected on one of them.

The Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in degrees Kelvin is equal to the voltage on the TM pin scaled by x100. (i.e. 3.0 V = 300°K = 27°C). It is important to remember that V•I Chips are multi-chip modules, whose temperature distribution greatly vary for each part number as well with input/output conditions, thermal management and environmental conditions. Therefore, TM cannot be used to thermally protect the system.
- Fault detection flag: the TM voltage source is internally turned off as soon as a fault is detected.

The Current Monitor (IM) pin provides a voltage proportional to the output current of the VTM. The voltage will vary between 0.4 V and 2.4 V over the output current range of the VTM (See Figure 7). The accuracy of the IM pin will be within 25% under all line and temperature conditions between 50% and 100% load. The accuracy of the pin can be improved using a predictive algorithm based on the input voltage and internal temperature. Please contact Applications Engineering for more information.

6.0 FUSE SELECTION

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. Input line fusing of V•I Chips is recommended at system level, to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum VTM current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t

7.0 CURRENT SHARING

The SAC topology bases its performance on efficient transfer of energy through a transformer, without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array (with same K factor), the VTM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

It is important to notice that, when successfully started, VTMs are capable of bi-directional operations (reverse power transfer is enabled if the VTM input falls within its operating range and the VTM is otherwise enabled). In parallel arrays, because of the resistive behavior, circulating currents are never experienced, because of energy conservation law.

General recommendations to achieve matched array impedances are (see also AN016 for further details):

- to dedicate common copper planes within the PCB to deliver and return the current to the modules
- to provide the PCB layout as symmetric as possible
- to apply same input/output filters (if present) to each unit

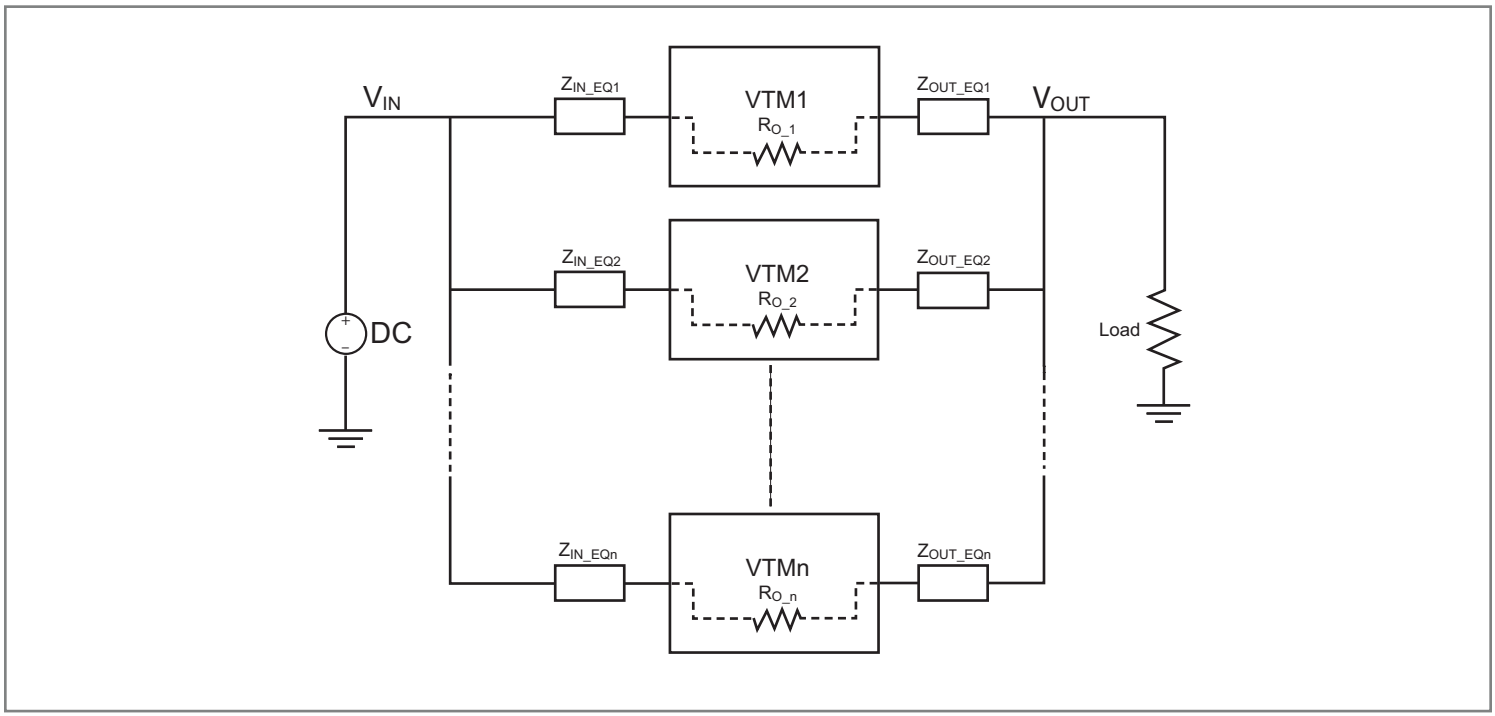


Figure 17 – *VTM Array*

8.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of a SAC systems versus conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance:

   To take full advantage of the VTM dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 47 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response:

   Given the wide bandwidth of the VTM, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the VTM multiplied by its K factor.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:

   The V•I Chip input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Owing to the wide bandwidth and low output impedance of the VTM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the VTM.

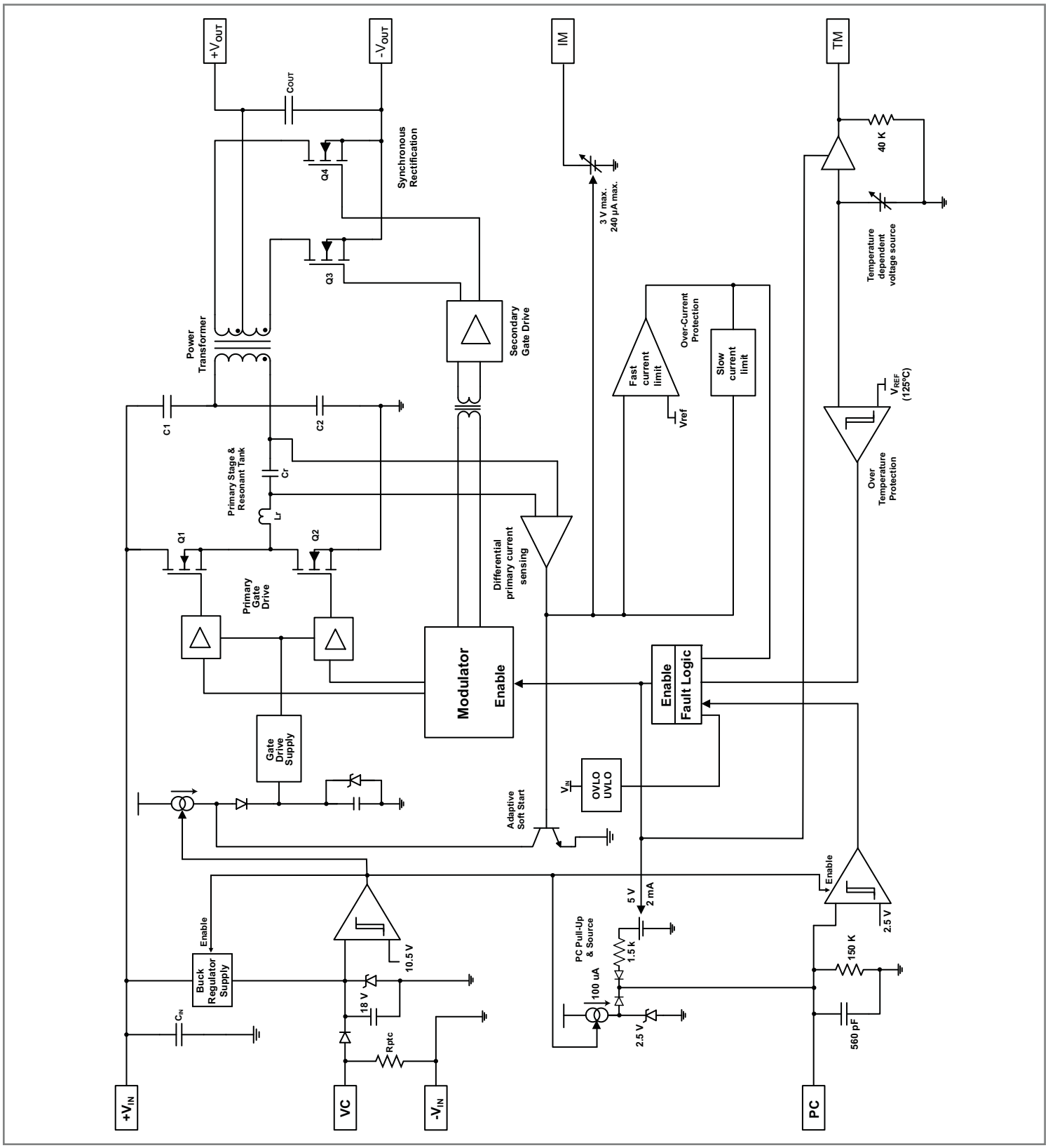


Figure 18 – *VTM block diagram*

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