

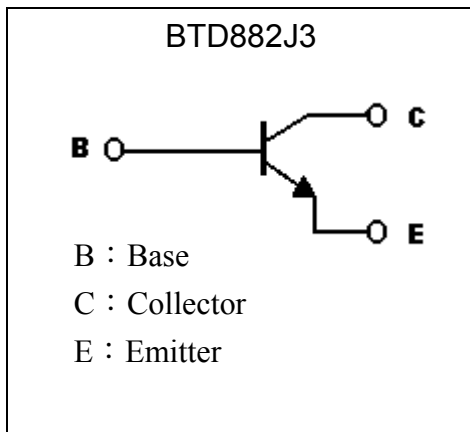
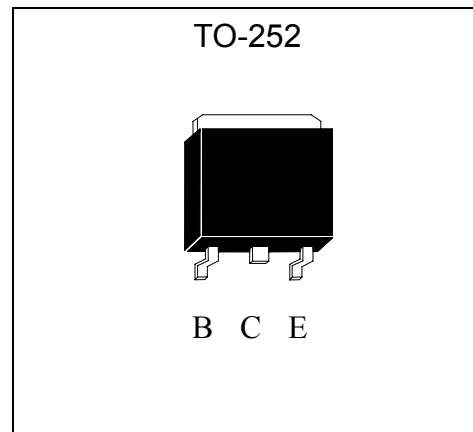
Low Vcesat NPN Epitaxial Planar Transistor

BTD882J3

BV_{CEO}	30V
I_C	3A
R_{CESAT}	125m Ω typ.

Features

- Low $V_{CE(sat)}$, typically 0.25V at $I_C / I_B = 2A / 0.2A$
- Excellent current gain characteristics
- Complementary to BTB772J3
- RoHS compliant package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V_{CBO}	40	V
Collector-Emitter Voltage	V_{CEO}	30	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	$I_C(\text{DC})$	3	A
	$I_C(\text{Pulse})$	7 *1	A
Power Dissipation	$P_d(T_a=25^\circ\text{C})$	1	W
	$P_d(T_c=25^\circ\text{C})$	10	
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

Note : *1. Single Pulse $P_w \leq 350\mu\text{s}$, Duty $\leq 2\%$.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	40	-	-	V	I _C =50μA, I _E =0
BV _{CEO}	30	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	5	-	-	V	I _E =50μA, I _C =0
I _{CBO}	-	-	1	μA	V _{CB} =30V, I _E =0
I _{EBO}	-	-	1	μA	V _{EB} =3V, I _C =0
*V _{CE(sat)}	-	0.25	0.5	V	I _C =2A, I _B =0.2A
*V _{BE(sat)}	-	-	2	V	I _C =2A, I _B =0.2A
*h _{FE1}	150	-	-	-	V _{CE} =2V, I _C =20mA
*h _{FE2}	180	-	560	-	V _{CE} =2V, I _C =1A
f _T	-	90	-	MHz	V _{CE} =5V, I _C =0.1A, f=100MHz
Cob	-	45	-	pF	V _{CB} =10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

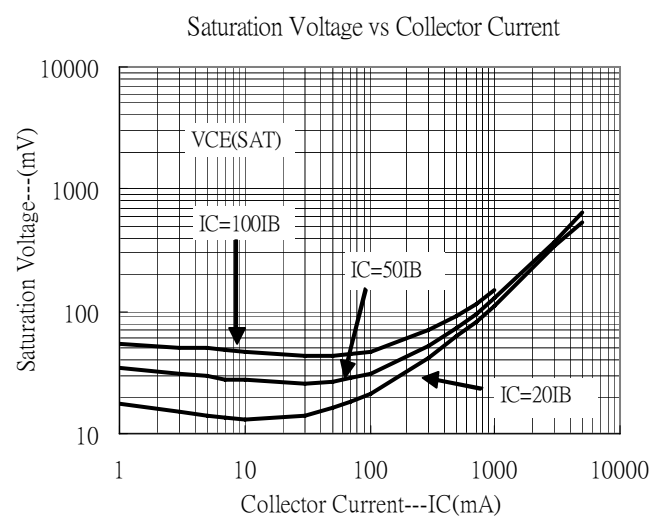
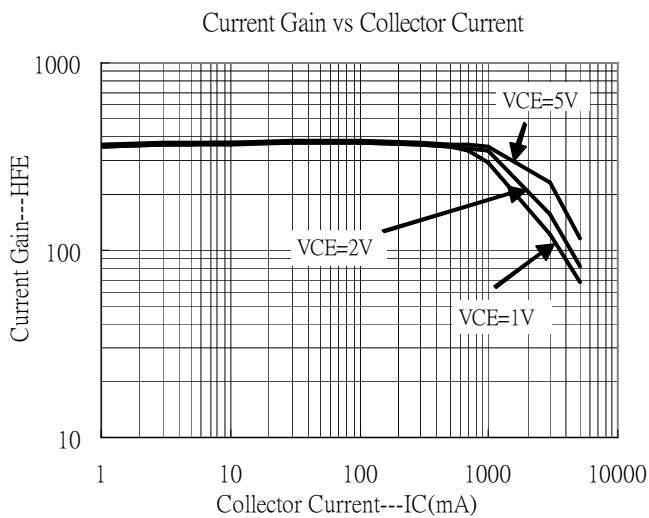
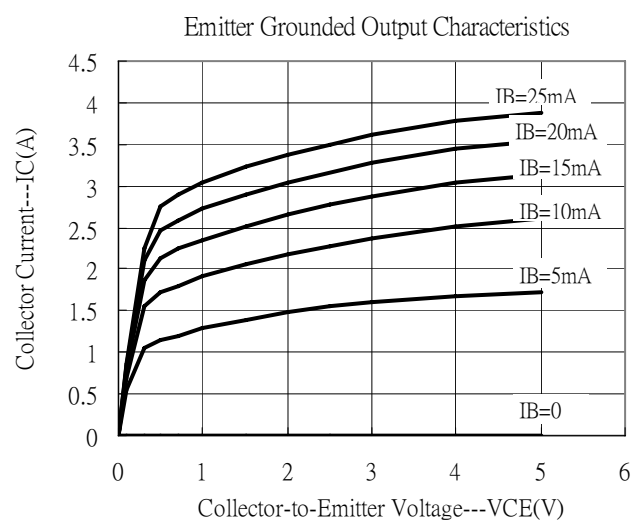
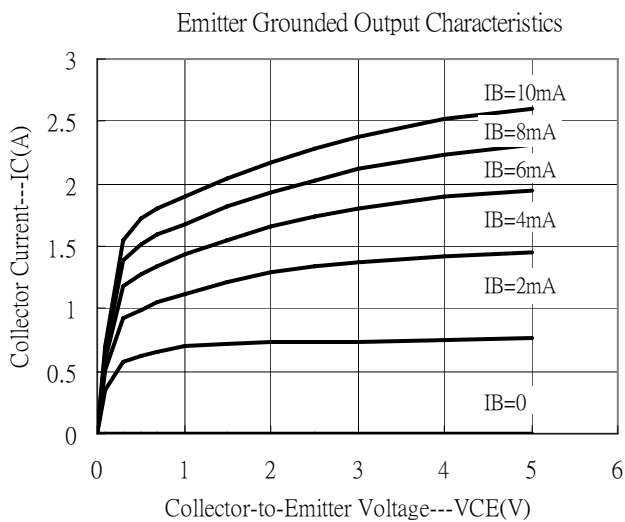
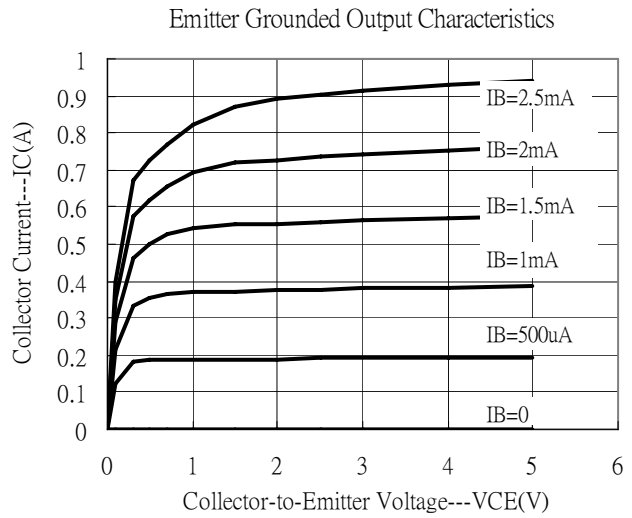
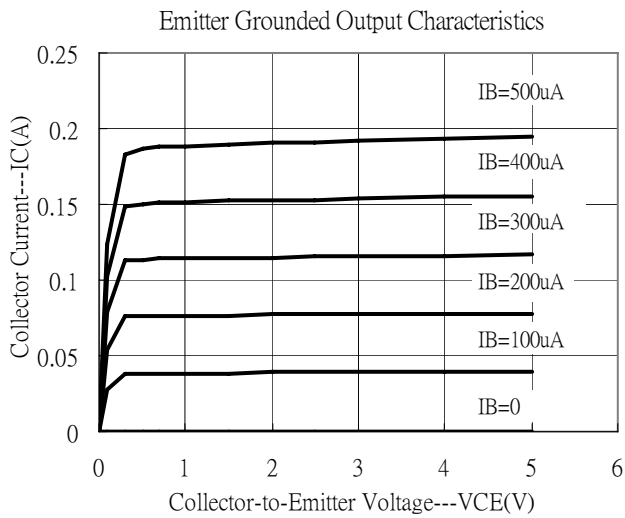
Classification Of h_{FE2}

Rank	P	E
Range	180~390	270~560

Ordering Information

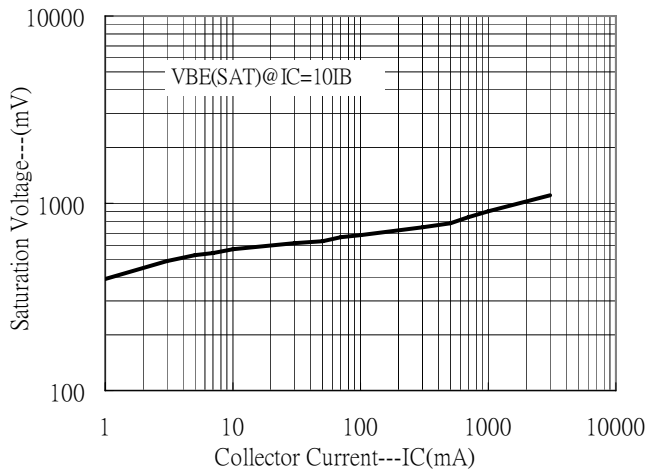
Device	Package	Shipping	Marking
BTD882J3	TO-252 (RoHS compliant)	2500 pcs/Tape & Reel	D882

Characteristic Curves

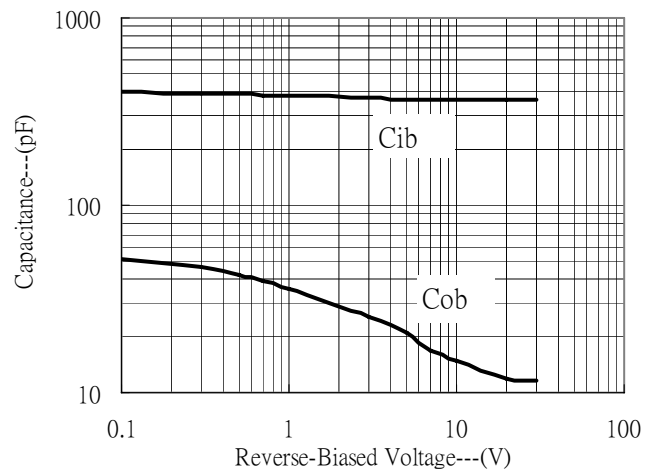


Characteristic Curves(Cont.)

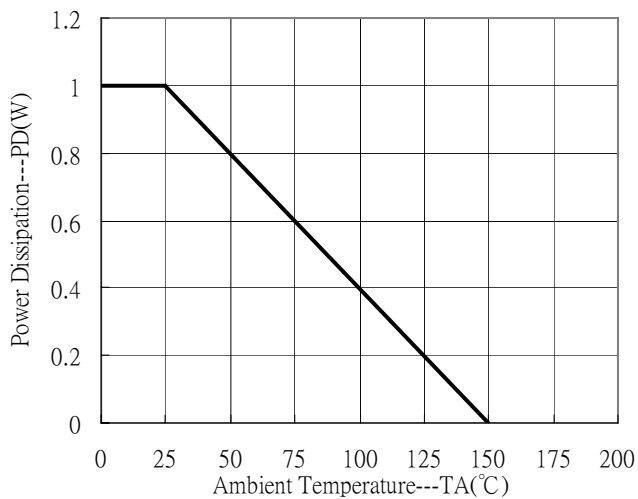
Saturation Voltage vs Collector Current



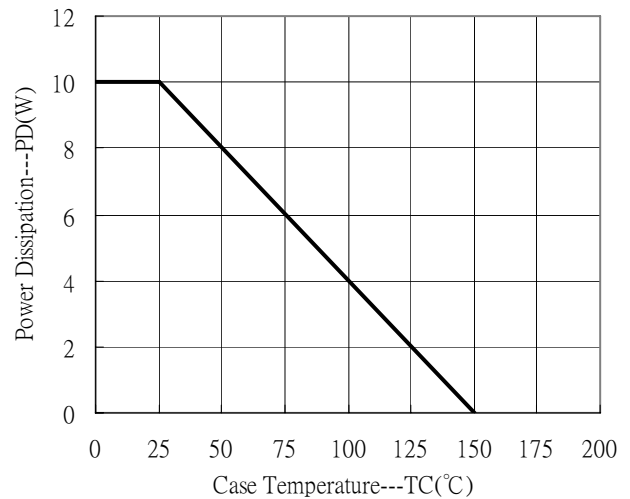
Capacitance vs Reverse-Biased Voltage



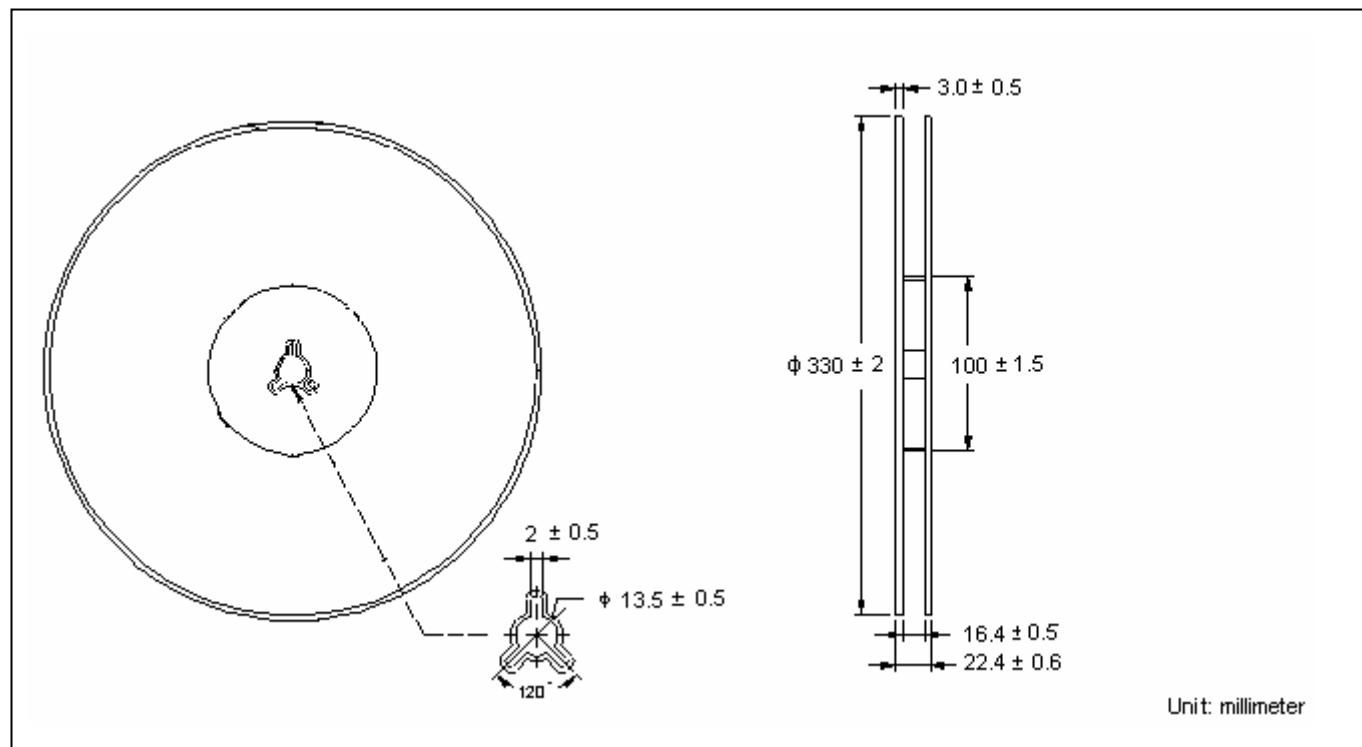
Power Derating Curve



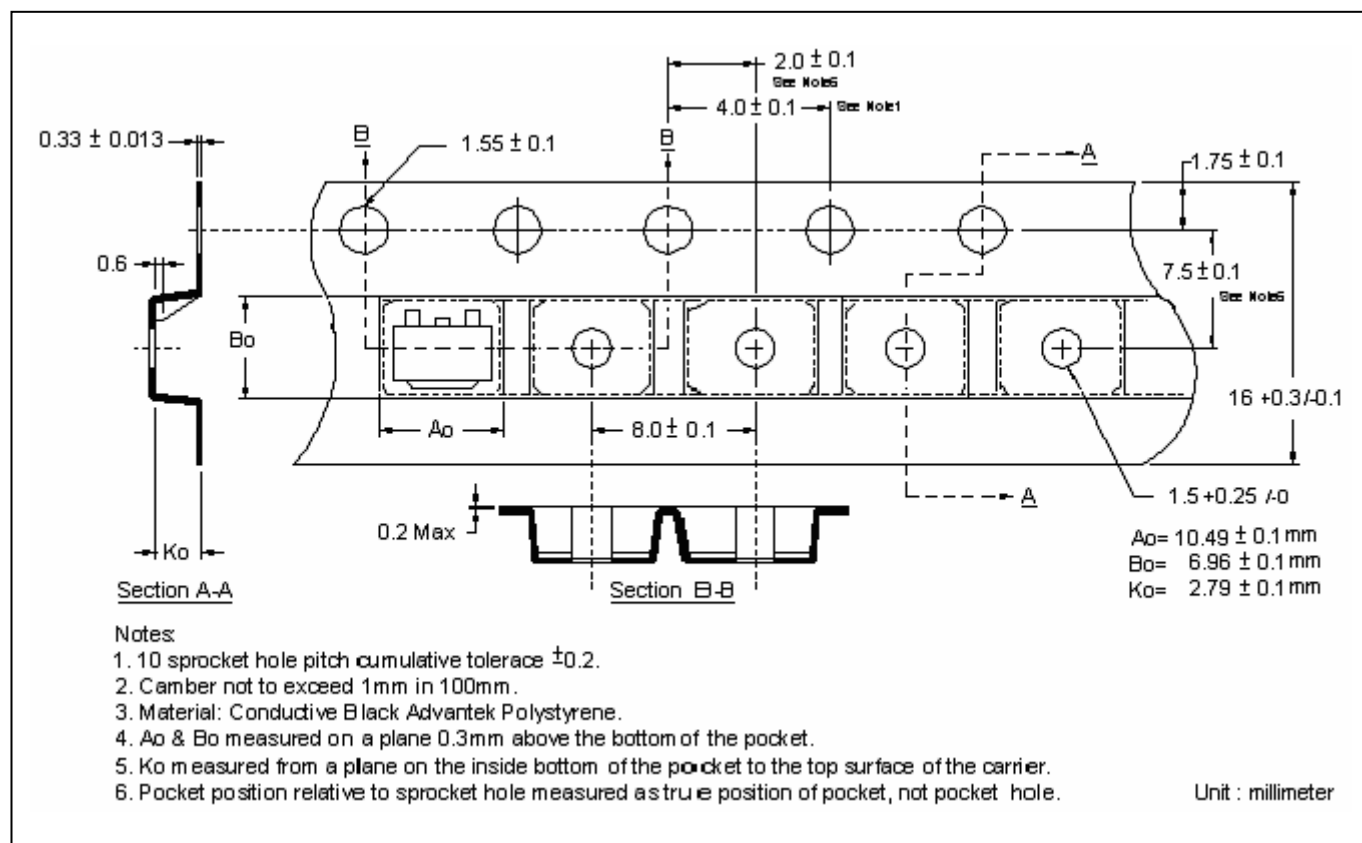
Power Derating Curve



Reel Dimension



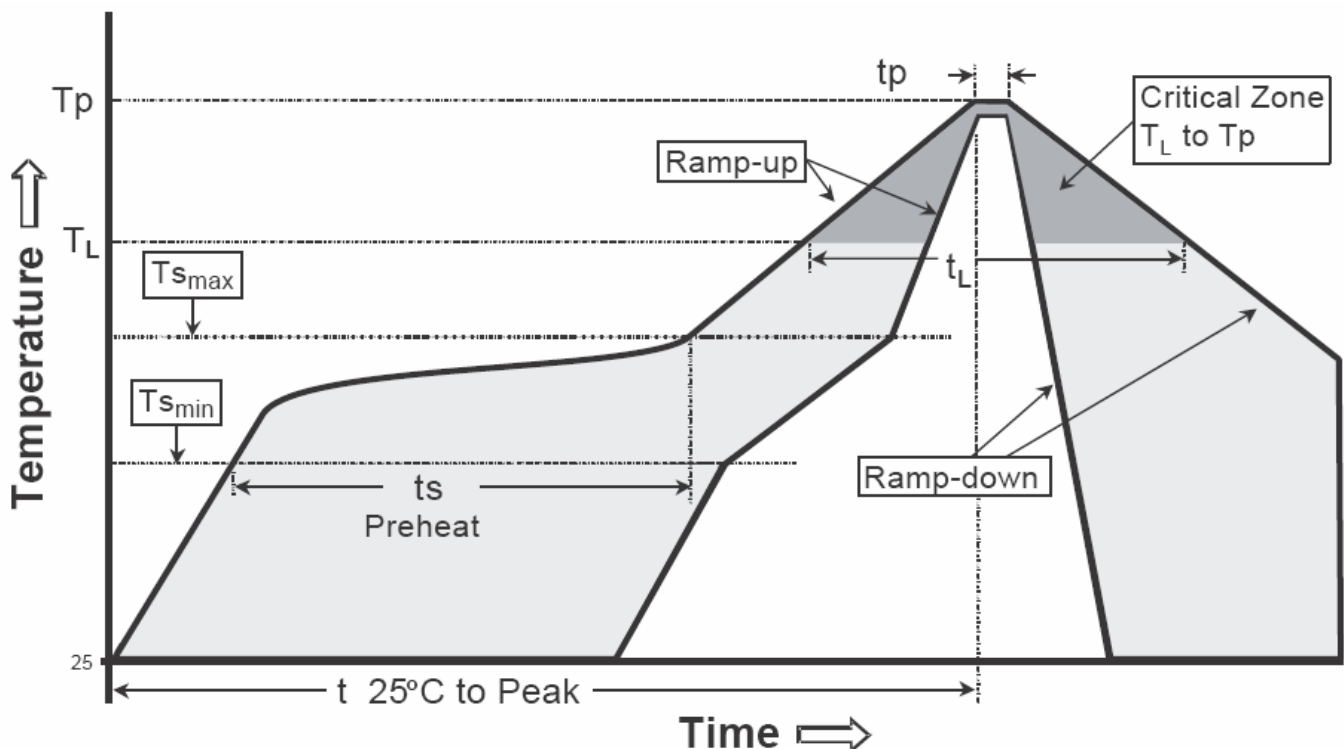
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

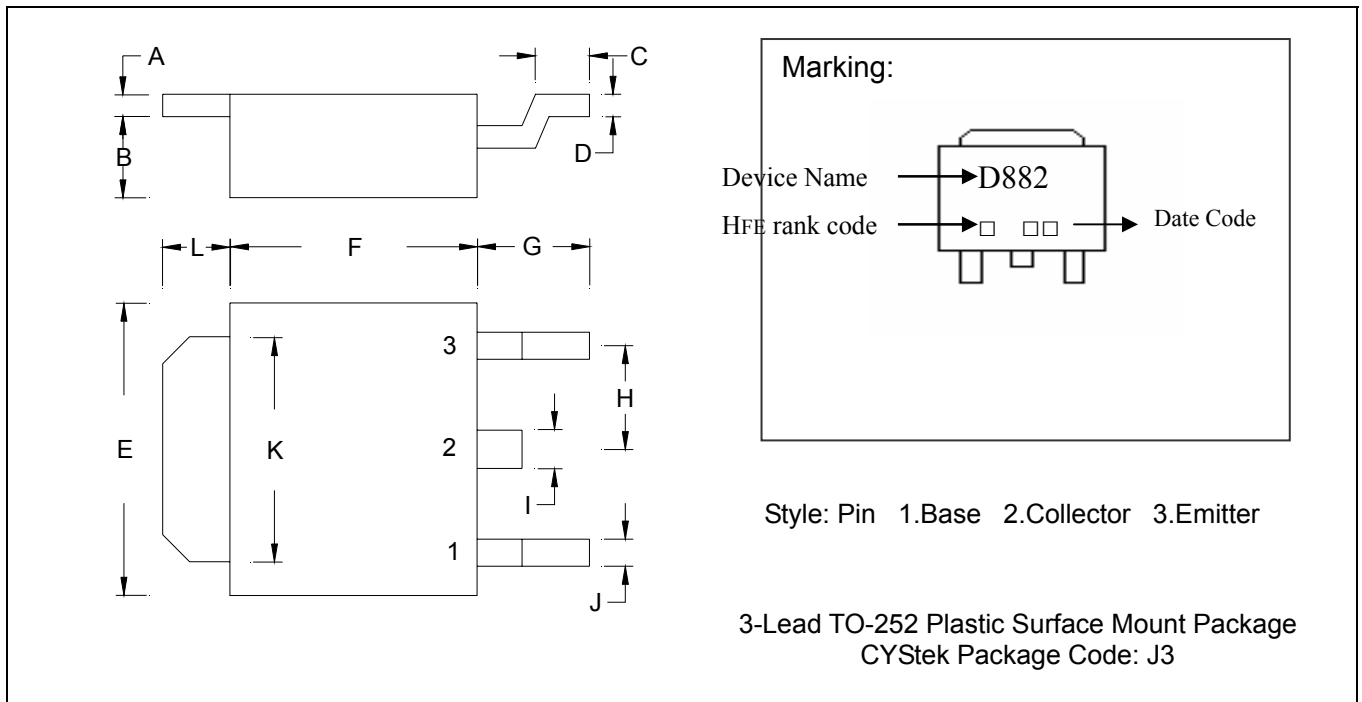
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.0866	0.1102	2.20	2.80
B	0.0650	0.0768	1.65	1.95	H	-	*0.0906	-	*2.30
C	0.0354	0.0591	0.90	1.50	I	-	0.0449	-	1.14
D	0.0177	0.0236	0.45	0.60	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2125	0.2283	5.40	5.80	L	0.0551	0.0630	1.40	1.60

Notes: 1.Controlling dimension: millimeters.

2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: KFC; pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.