Low Profile Transceiver Module for Telecom Applications 9.6 kbit/s to 1.152 Mbit/s Data Transmission Rate

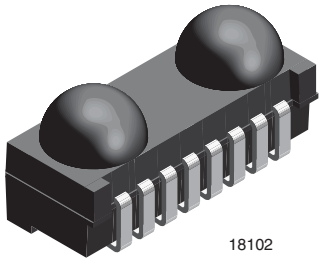
Description

The miniaturized TFDU5107 in the well-known Baby Face package is an ideal transceiver for applications in telecommunications like mobile phones, pagers, and PDAs of all kinds. The devices are designed for optimum performance and minimum package size.

The device covers the IrDA® physical layer specification up to 1.152 Mbit/s (MIR).

A current limiter is implemented to operate the device without external resistor in an IrDA compliant mode (> 1 m). For reduced current as for the 'Low Power' mode a current limiting resistor might be added.

The device covers the supply voltage from 5.5 V down to 2.4 V and with its low power consumption it is optimum suited for battery-powered applications. Double eye safety protection by pulse duration and current limitation is integrated.



Features

- Package:
  TFDU5107 Universal (Baby Face)
  SMD Side and Top View Solderability
- Internal IRED current limitation
  to operate without external resistor.
  With external resistor adaptable to power reduced operation as IrDA 'Low Power' Standard
- Wide supply voltage range (2.4 V to 5.5 V)
- Operational down to 2.0 V
- **Logic Input and Output Voltage 1.5 V to 5.5 V set by external control pin**
- Tri - State - receiver output
- Lowest power consumption, typically 500 µA in receive mode, <1 µA shutdown
- Fewest external components
- High EMI immunity
- Eye safety protection integrated
- Pin assignment backward compatible to legacy Baby Face package
- Split power supply, transmitter and receiver can be operated from two power supplies withrelaxed requirements saving costs, US-Patent No. 6,157476
- Lead (Pb)-free device
- Device in accordabce to RoHS 2002/95/EC and WEEE 2002/96/EC

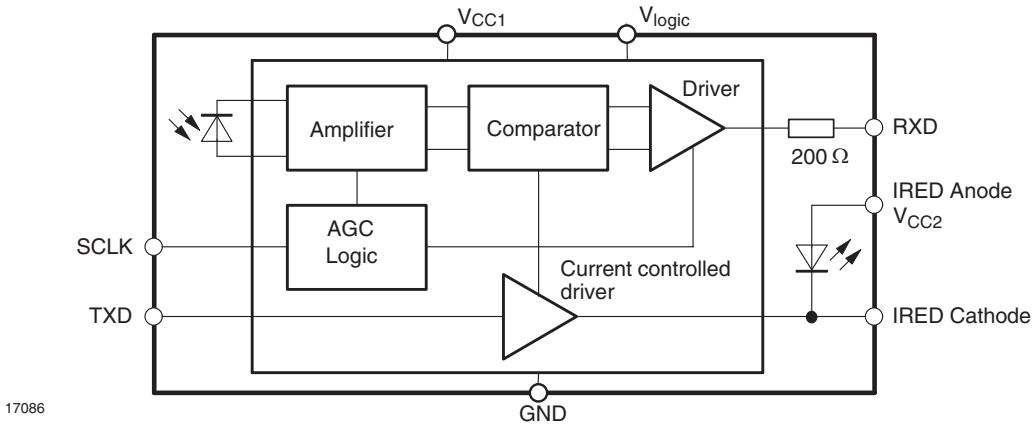
Applications

- Mobile phones, pagers, hand-held battery Operated equipment
- Computers (WinCE, PalmPC, PDAs)
- Digital still and video cameras
- Extended IR adapters
- Medical and industrial data collection

Parts Table

Part	Description	Qty / Reel
TFDU5107-TR3	Oriented in carrier tape for side view surface mounting	1000 pcs.
TFDU5107-TT3	Oriented in carrier tape for top view surface mounting	1000 pcs

Functional Block Diagram



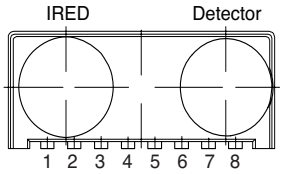
Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	Connect IRED anode directly to a power supply. Adding an external resistor at this pin will make the module to work in "Low Power Mode".		
2	IRED Cathode	IRED Cathode, internally connected to the driver transistor		
3	TXD	Transmit Data Input	I	HIGH
4	RXD	Received Data Output, push-pull CMOS driver output capable of driving standard CMOS or TTL loads. No external pull-up or pull-down resistor is required. Pin is floating with a weak pull-up to V_{CC}, when device is in shutdown mode. RXD output is quiet during transmission.	O	LOW
5	SD	Shutdown, will switch the device into shutdown after a delay of 1 ms	I	HIGH
6	V_{CC}	Supply Voltage		
7	V_{logic}	Defines the input and output logic swing voltage.	I	
8	GND	Ground		

Pinout

TFDU5107
weight 200 mg

BabyFace (Universal)



Absolute Maximum Ratings

Reference Point Ground, Pin 8, unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range	0 V < V_{dd2} < 6 V	V_{dd1}	- 0.5		6	V
	0 V < V_{dd1} < 6 V	V_{dd2}	- 0.5		6	V
	0 V < V_{dd2} < 6 V, 0 V < V_{dd1} < 6 V	V_{logic}	- 0.5		6	V
Input current	all pins (Pin 1 excluded)				10	mA
Output sinking current, RXD	Pin 4				25	mA
Rep. pulsed IRED current	Pin 1, t_{on} < 20 %, < 20 µs	$I_{IRED(RP)}$			500	mA
Average IRED current		$I_{IRED(DC)}$			125	mA
Power dissipation		P_{tot}			450	mW
Junction temperature		T_J			125	°C
Ambient temperature range (operating)		T_{amb}	- 25		+ 85	°C
Storage temperature range		T_{stg}	- 25		+ 85	°C
Soldering temperature	see chapter Recommended Solder Profile				260	°C
Transmitter data and shutdown input voltage	2.4 V < V_{dd1} < 5.5 V	V_{TXD}, V_{SD}	- 0.5		6	V
Receiver data output voltage		V_{RXD}	- 0.5		V_{logic} + 0.5	V
Virtual source size	Method: (1 - 1/e) encircled energy	d	2.5	2.8		mm
Maximum intensity for class 1 operation of IEC825 or EN60825	IEC60825-1 or EN60825-1, edition Jan. 2001				320[1)]	mW/sr

[1)] Due to the protocol real IRDA®data transfers in SIR and MIR mode have an equal distribution of ‘0‘ and ‘1‘ data, therefore the limit is typically a factor of 2 larger than the value for lab testing. The device is protected against TXD short (single fault condition) by an internal shut-off when the pulse duration is exceeding maximum IrDA specification value of pulse duration.

Electrical Characteristics

Transceiver

T_{amb} = 25 °C, V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supported data rates, RXD pulse duration 400 ns	base band, SIR mode		9.6		115.2	kbit/s
	base band, 1.152 Mbit/s		9.6		1152	kbit/s
Supply voltage range	specified operation	V_{dd1}	2.4		5.5	V
Supply current receive mode	V_{dd1} = 2.4 V to 5.5 V	I_S		500	900	µA
Supply current shutdown mode	V_{dd1} = 2.4 V to 5.5 V	I_{SSD}		0.1	1	µA
Average supply current[1], standard MIR transmit mode I_e > 100 mW/sr	V_{dd1} = 2.4 V to 5.5 V, above V_{dd1} = 3.3 V a serial resistor for reducing the internal power dissipation should be implemented, e.g. R_L = 2.7 Ω	I_S		60	110	mA
Shutdown/ mode clock pulse duration		t_{prog}	0.2		20	µs
Shutdown delay 'Receive off'		t_{prog}	1		1.5	ms
Shutdown delay 'Receive on'		t_{prog}	40		100	µs
Transceiver 'Power on' settling time	Time from switching on V_{dd1} to established specified operation				50	µs

[1] Maximum data is for 20 % (25 %) duty cycle for SIR (MIR 1.152 Mbit/s) Low power mode. The typical value is given for the case of normal operation with statistical and equal '0' and '1' - distribution.

Optoelectronic Characteristics

Receiver

V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance SIR 9.6 kbit/s to 115.2 kbit/s [1]	$\lvert \alpha \rvert \leq \pm 15°$, V_{dd1} = 2.4 V to 5.5 V	$E_{e, min}$		20	35	mW/m^2
Minimum detection threshold irradiance 9.6 kbit/s to 115.2 kbit/s [1]	$\lvert \alpha \rvert \leq \pm 15°$, V_{dd1} = 2.4 V to 5.5 V	$E_{e, min}$		50	80	mW/m^2
Maximum detection threshold irradiance	$\lvert \alpha \rvert \leq \pm 90°$, V_{dd1} = 5 V	$E_{e, max}$	3300	5000		W/m^2
	$\lvert \alpha \rvert \leq \pm 90°$, V_{dd1} = 3 V	$E_{e, max}$	8000	15000		W/m^2
Logic low receiver input irradiance		$E_{e, max,low}$	4			mW/m^2
Output voltage RXD	active, C = 15 pF, R = 2.2 kΩ	V_{OL}		0.5	0.8	V
	non active, C = 15 pF, R = 2.2 kΩ	V_{OH}	V_{logic} - 0.5			V
Output current RXD	V_{OL} < 0.8 V				4	mA
Rise time at load	C = 15 pF, R = 2.2 kΩ, 1.5 V ≤ V_{logic} ≤ 5.5 V	t_r	20		70	ns
Fall time at load	C = 15 pF, R = 2.2 kΩ, 1.5 V ≤ V_{logic} ≤ 5.5 V	t_f	20		70	ns
RXD signal electrical output pulse width	1.5 V ≤ V_{logic} ≤ 5.5 V	t_p	300	400	500	ns
Latency		t_L		100	200	µs

[1] RXD output pulse duration 400 ns

Transmitter

V_{dd1} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Logic CMOS high/low decision threshold		$V_{IL(TXD)}$		1/2 x V_{logic}		V
Logic low transmitter input voltage		$V_{IL(TXD)}$	0		0.2[1] V_{logic}	V
Logic high transmitter input voltage	1.5 < V_{logic} < 5.5 V	$V_{IH(TXD)}$	0.8[1] V_{logic}		V_{logic} + 0.5	V
Forward current limitation	V_{dd1} = 3.3 V	I_F		400		mA
Output radiant intensity, standard MIR level	$\lvert \alpha \rvert \leq \pm 15°$, I_{F6} = 400 mA resistor limited	I_e	110	250	320	mW/sr
Maximum output pulse width (eye safety protection)	P_{WI} > 23 µs	P_{WOmin}	23		80	µs
Optical pulse width	P_{WI} = 1.6 µs	P_{WO}	1.45		1.75	µs
	P_{WI} = 217 ns	P_{WO}	210		226	ns
Optical rise/fall time		t_r, t_f			40	ns
Peak wavelength of emission		λ_p	880		900	nm
Spectral optical radiation bandwidth		$\Delta\lambda$		45		nm
Output radiant intensity	TXD logic low level				0.04	µW/sr
Overshoot, optical					25	%
Rising edge peak to peak jitter		t_j			0.2	µs

[1] Switch, current can be defined by external resistor, internal current limitation to 500 mA peak

Identification

The TFDU5107 has a hidden identification option. A device identification can be recalled by setting the SD active followed by activating TXD for a short period. With the low going edge of TXD a single pulse is generated at RXD.
The SD is intended to activate the shutdown function after a delay of 1 ms. Therefore the full sequence should be run with that 1 ms time limitation, see drawing.

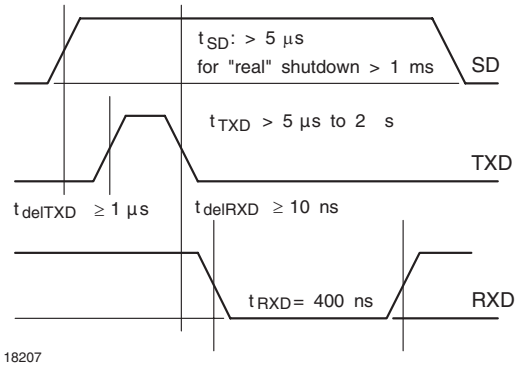


Figure 1. Timing Diagram

Truth table

Inputs			Outputs	
SD	TXD	Optical input Irradiance mW/m^2	RXD	LED drive current resulting intensity I_e in mW/sr
high < 1 ms	pulse	x	low going TXD triggers monostable to edit 400 ns low pulse	0
high > 1 ms	x	x	floating (500 kΩ to V_{dd})	0
low	high	x	high	10 < I_e < 300 defined by an external resistor
	high ≥ 80 µs	x	high	0
	low	< 4	high	0
	low	> 40	low, pulse of 400 ns edge triggered	0

Recommended Solder Profile

Solder Profile for Sn/Pb soldering

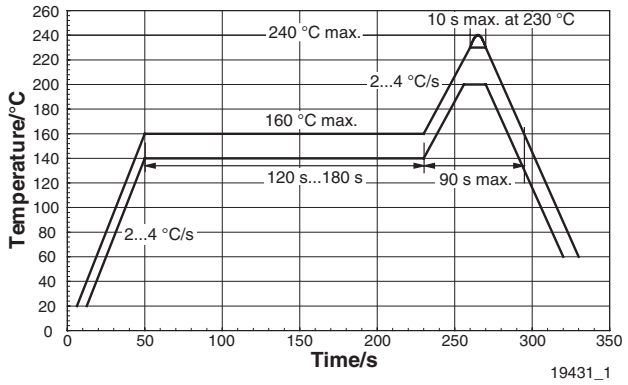


Figure 2. Recommended Solder Profile for Sn/Pb soldering

Lead-Free, Recommended Solder Profile

The lead-frame based transceivers (all types with the name TFDUxxxx) are lead (Pb)-free and qualified for lead (Pb)-free and lead - bearing processing.

In case of using a lead-bearing process we recommend a solder profile as shown in figure 4.

For lead (Pb)-free solder paste like Sn-(3.0-4.0)Ag-(0.5-0.9)Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 5 and figure 6 are VISHAY's recommende profiles for use with the TFDUxxxx transceivers for lead (Pb)-free processing.

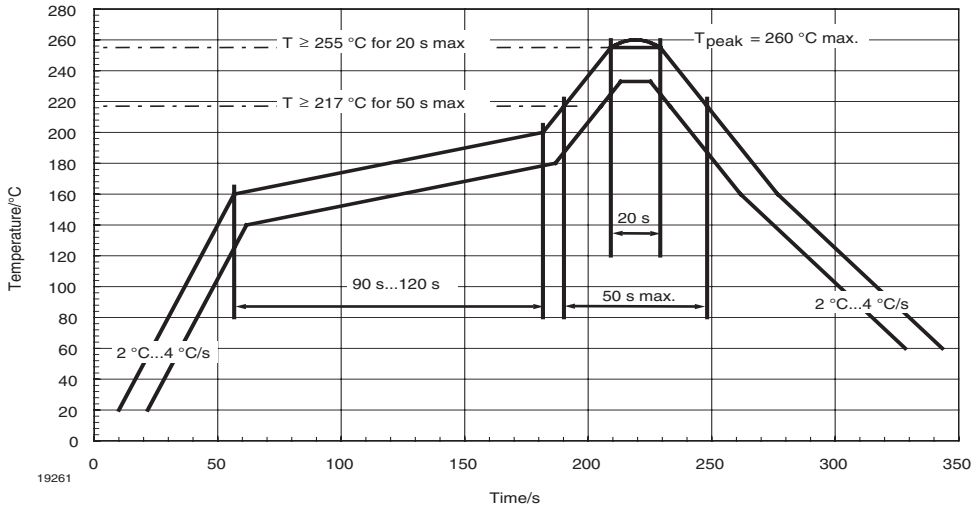


Figure 3. Solder Profile, RSS Recommendation

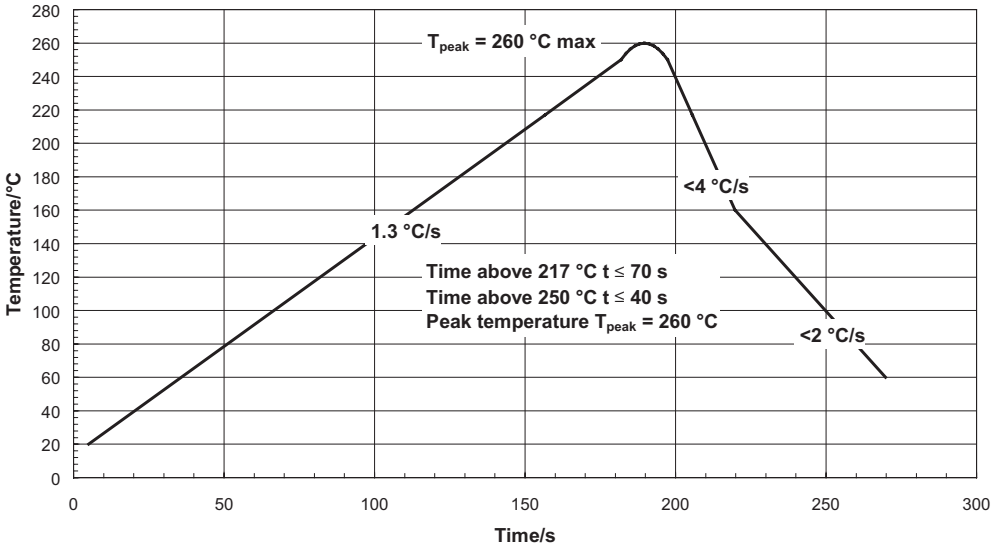


Figure 4. Solder Profile, RTS Recommendation

A ramp-up rate less than 0.9°C/s is not recommended. Ramp-up rates faster than 1.3°C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Current Derating Diagram

Figure 4 shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to Ground for supply voltages above 4 V. In that case the device can be operated up to 85 °C, too.

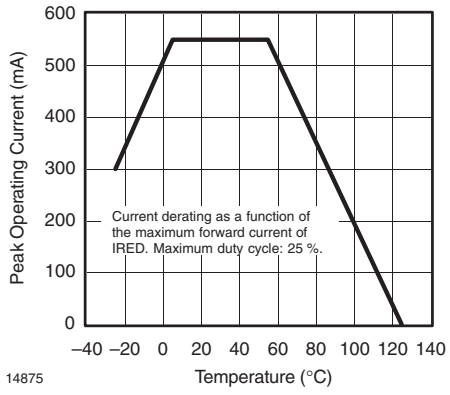


Figure 5. Current Derating Diagram

Typical Characteristics (Tamb = 25 °C unless otherwise specified)

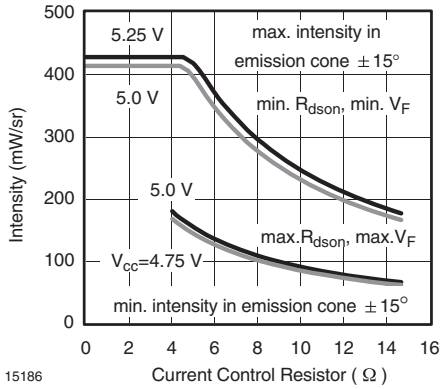


Figure 6. Intensity I_e vs. Current Control Resistor R2, 5 V Applications

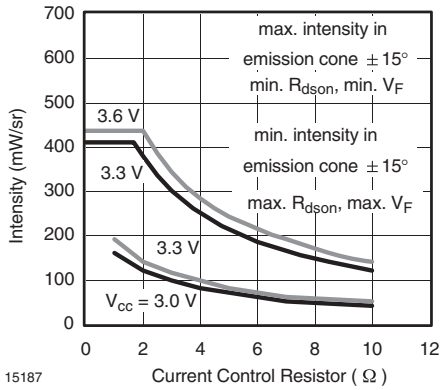


Figure 7. Intensity I_e vs. Current Control Resistor R1, 3 V Applications

Package Dimensions

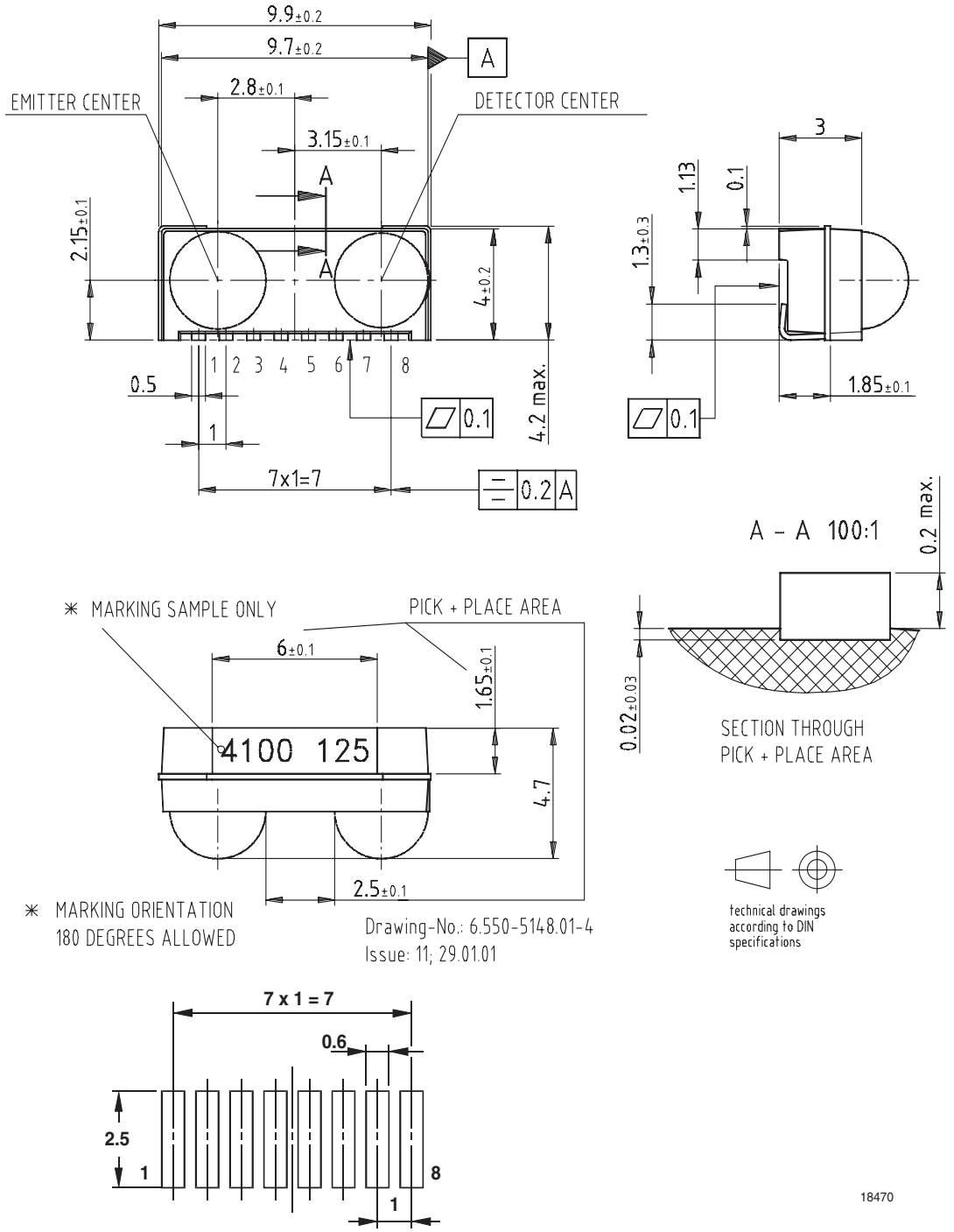


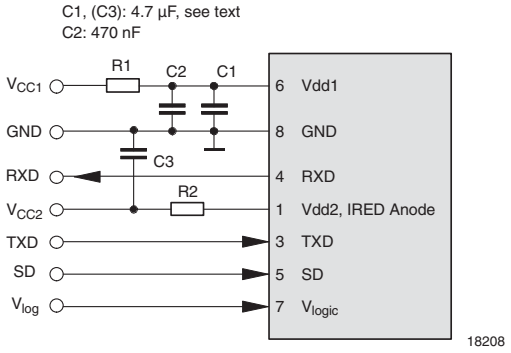
Figure 8. Package drawing and solder footprint TFDU5107, dimensions in mm, tolerance ± 0.2 mm if not otherwise mentioned

Appendix
Application Hints

The TFDU5107 does not need any external components when operated with a "clean" power supply. In a more noisy ambient it is recommended to add a combination of a resistor and capacitor (R1, C1, C2) for noise suppression as shown in the figure below. A combination of a electrolytic for the low frequency range and a ceramic capacitor for suppressing the high frequency disturbance will be most effective. The capacitor C3 is only necessary when inductive wiring is used or the power supply cannot deliver the operating peak pulse current.

The inputs TXD and SD are high impedance CMOS inputs. Therefore, the lines from the I/O to those inputs should be carefully designed not to pick up ambient noise. If long lines are used, loads at the TXD input of the TFDx5x07 and at the RXD input of the controller (!) are recommended. At the IRED Anode voltage supply line an additional capacitor might be necessary when inductive wiring is used. However, a low impedance layout is the better and more cost efficient solution. For adjusting the intensity depending on the application, see the diagrams.

Recommended Circuit Diagram



Shut down

To shut down the TFDx5x07 into a standby mode the SD pin has to be set active. After a delay of < 1 ms it will switch to the standby mode.

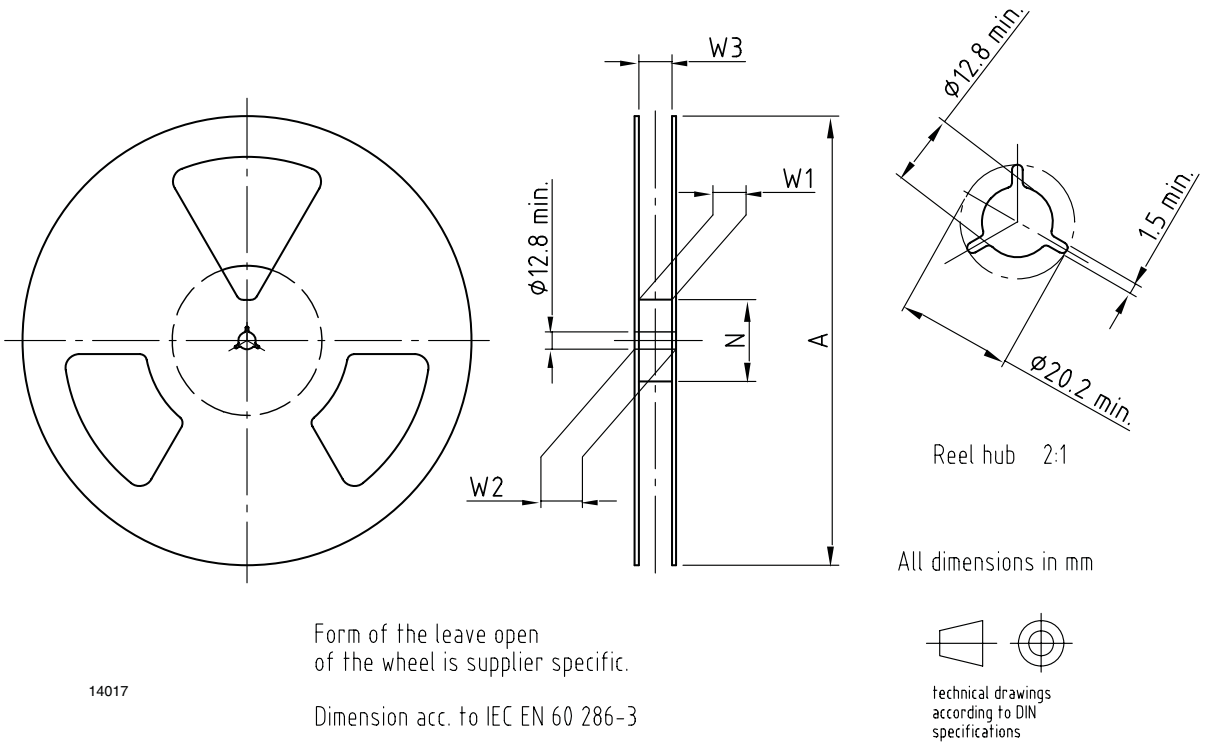
Latency

The receiver is in specified conditions after the defined latency. In a UART related application after that time (typically 50 µs) the receiver buffer of the UART must be cleared. Therefore the transceiver has to wait at least the specified latency after receiving the last bit before starting the transmission to be sure that the corresponding receiver is in a defined state.

Recommended Application Circuit Components

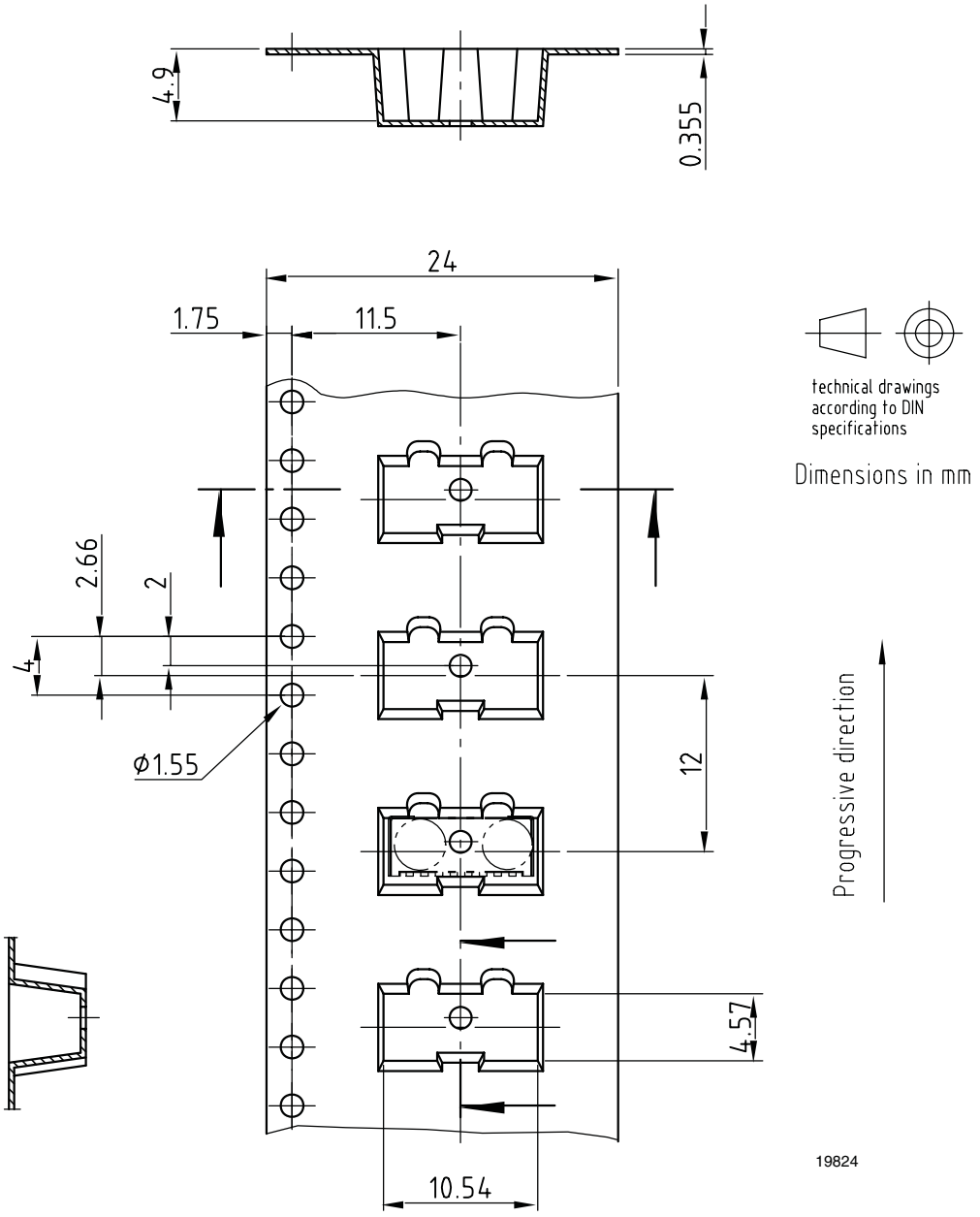
Component	Recommended Value	Vishay Part Number
C1, C3	4.7 µF, 16 V	293D 475X9 016B
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	47 Ω, 0.125 W	CRCW-1206-47R0-F-RT1
R2	**5 V supply voltage:** 14 Ω 0.25 W (recommended using two 6.8 Ω, 0.125 W resistors in series) **3.3 V supply voltage:** 4.5 Ω 0.25 W (recommended using two 2.3 Ω, 0.125 W resistors in series)	CRCW-1206-6R80-F-RT2 CRCW-1206-2R26-F-RT1

Reel Dimensions



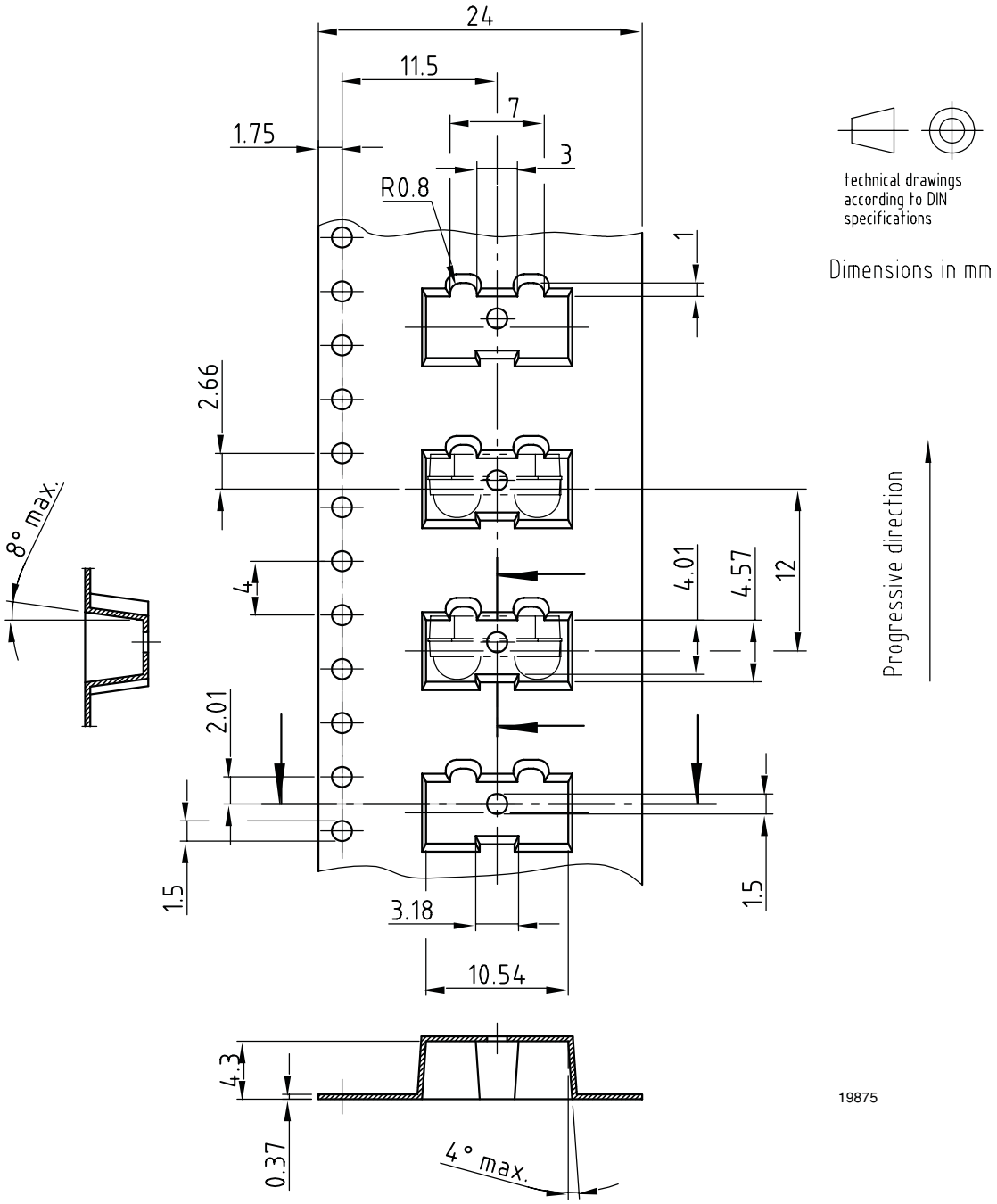
Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
24	330	60	24.4	30.4	23.9	27.4

Tape Dimensions



Drawing-No.: 9.700-5251.01-4
Issue: 3; 02.09.05

Figure 9. Tape drawing, TFDU5107 for top view mounting, tolerance ± 0.1 mm



Drawing-No.: 9.700-5297.01-4
Issue: 1; 08.04.05

Figure 10. Tape drawing, TFDU5107 for side view mounting, tolerance ± 0.1 mm

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany

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