CS5466

Low-cost Power/Energy IC with Pulse Output

Features

- Single-chip Power Measurement Solution
- Energy Data Linearity:
  ±0.1% of Reading, over 1000:1 Dynamic Range
- On-chip functions: Measures Power and Performs Energy-to-pulse Conversions
- Meets Accuracy Spec for IEC, ANSI, & JIS.
- High-pass Filter Option
- Four Input Ranges for Current Channel
- On-chip, 2.5 V Reference
- Pulse Outputs for Stepper Motor or Mechanical Counter
- On-chip Energy Direction Indicator
- Ground-referenced Input Signals with Single Supply
- High-frequency Output for Calibration
- On-chip, Power-on Reset (POR)
- Power Supply Configurations:
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to 5 V

Description

The CS5466 is a low-cost power meter solution incorporating dual delta-sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs), an energy-to-frequency converter, and energy pulse outputs on a single chip. The CS5466 is designed to accurately measure and calculate energy for single phase, 2- or 3-wire power metering applications with minimal external components.

The low-frequency pulse outputs, $\overline{\text{E1}}$ and $\overline{\text{E2}}$, provide pulses at a frequency which is proprtional to the active power and can be used to drive a stepper motor or a mechanical counter. Energy direction output, NEG, indicates when pulse outputs $\overline{\text{E1}}$ and $\overline{\text{E2}}$ represent negative active power. The high-frequency pulse output FOUT is designed to assist in system calibration.

The CS5466 has configuration pins which allow for direct configuration of pulse output frequency, current channel input range, and high-pass filter enable option.

The CS5466 also has a power-on reset function which holds the part in reset until the supply reaches an operable level.

ORDERING INFORMATION

See page 16.

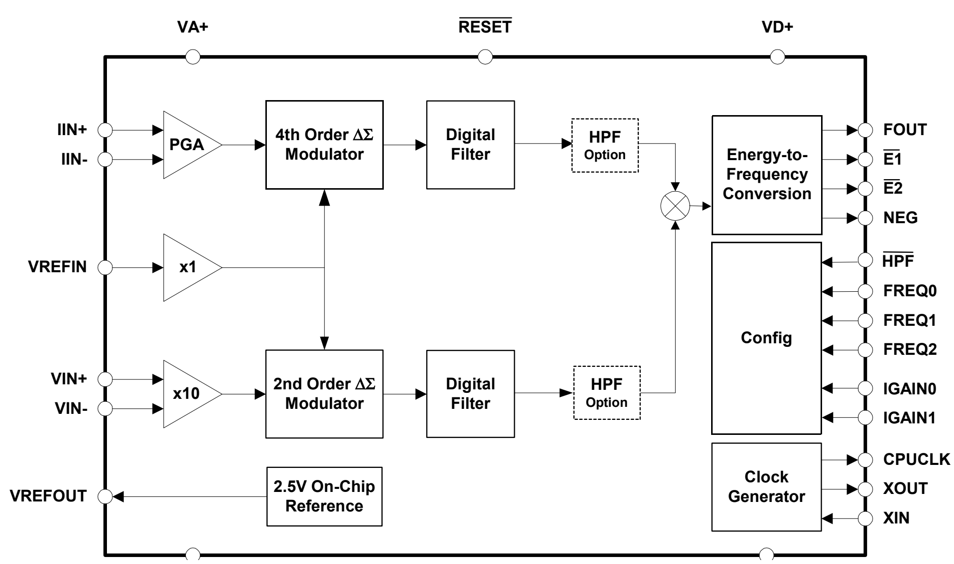


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. OVERVIEW

The CS5466 is a CMOS monolithic power measurement device with an energy computation engine. The CS5466 combines a programmable gain amplifier, two ΔΣ ADCs, and energy-to-frequency conversion circuitry on a single chip.

The CS5466 is designed for energy measurement applications and is optimized to interface to a shunt or current transformer for current measurement, and to a resistive divider or transformer for voltage measurement. The current channel has a programmable gain amplifier (PGA) which provides four full-scale input options. With a single +5 V supply on VA+/AGND, both of the CS5466's input channels accommodate common-mode plus signal levels between (AGND - 0.25 V) and VA+.

The CS5466 has three pulse output pins: $\overline{E1}$, $\overline{E2}$, and FOUT. $\overline{E1}$ and $\overline{E2}$ can be used to directly drive a mechanical counter or stepper motor, or interface to a microcontroller. The FOUT pin conveys active (real) power at a pulse frequency many times higher than that of the $\overline{E1}$ or $\overline{E2}$ pulse frequency, allowing for high-speed calibration.

2. PIN DESCRIPTION

Crystal Out	**XOUT**	1	24	**XIN**	Crystal In
CPU Clock Output	**CPUCLK**	2	23	**FREQ0**	Frequency Select 0
Positive Power Supply	**VD+**	3	22	**$\overline{\text{E1}}$**	Energy Output 1
Digital Ground	**DGND**	4	21	**$\overline{\text{E2}}$**	Energy Output 2
Gain Select 0	**IGAIN0**	5	20	**FREQ1**	Frequency Select 1
Negative Energy Indicator	**NEG**	6	19	**$\overline{\text{RESET}}$**	Reset
Gain Select 1	**IGAIN1**	7	18	**FOUT**	High-frequency Output
High-pass Filter Enable	**$\overline{\text{HPF}}$**	8	17	**FREQ2**	Frequency Select 2
Differential Voltage Input	**VIN+**	9	16	**IIN+**	Differential Current Input
Differential Voltage Input	**VIN-**	10	15	**IIN-**	Differential Current Input
Voltage Reference Output	**VREFOUT**	11	14	**VA+**	Positive Analog Supply
Voltage Reference Input	**VREFIN**	12	13	**AGND**	Analog Ground

Clock Generator		
Crystal Out **Crystal In**	1, 24	**XOUT, XIN** - A single stage amplifier inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins		
Gain Select	5, 7	**IGAIN1, IGAIN0 -** Used to select the current channel input gain range.
Frequency Select	17, 20, 23	**FREQ2,FREQ1,FREQ0 -** Used to select max pulse output frequency for $\overline{\text{E1}}$, $\overline{\text{E2}}$, and FOUT.
High Pass Filter Enable	8	**$\overline{\text{HPF}}$ -** High disables the HPF. Low activates HPF on Voltage channel. Connecting $\overline{\text{HPF}}$ pin to FOUT pin activates HPF on Current channel.
Reset	19	**$\overline{\text{RESET}}$ -** Low activates Reset.
Energy Pulse Outputs		
Energy Output	22, 21	**$\overline{\text{E1}}$, $\overline{\text{E2}}$ -** Active low alternating pulses with an output frequency that is proportional to the active (real) power.
High Freq Output	18	**FOUT** - Outputs energy pulses at a frequency higher than $\overline{\text{E1}}$ and $\overline{\text{E2}}$ outputs. Used for calibration purposes.
Neg Energy Indicator	6	**NEG** - High indicates negative energy.
Analog Inputs/Outputs		
Differential Voltage Inputs	9, 10	**VIN+, VIN- -** Differential analog input pins for voltage channel.
Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference output pin. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN -** Voltage input to this pin establishes the voltage reference for the on-chip modulators.
Differential Current Inputs	16, 15	**IIN+, IIN- -** Differential analog input pins for current channel.
Power Supply Connections		
Positive Digital Supply	3	**VD+ -** The positive digital supply.
Digital Ground	4	**DGND -** Digital Ground.
Analog Ground	13	**AGND -** Analog Ground.
Positive Analog Supply	14	**VA+ -** The positive analog supply.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all operating ponditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs (Current Channel)					
Differential Input Range (Gain = 10) [(I_{IN}+)-(I_{IN}-)] (Gain = 50) (Gain = 100) (Gain = 150)	I_{IN}	- - - -	±250 ±50 ±25 ±16.7	- - - -	mV mV mV mV
Input Capacitance (All Gain Ranges)	$C_{in}I$	-	25	-	pF
Effective Input Impedance (All Gain Ranges)	$Z_{in}I$	30	-	-	kΩ
Analog Inputs (Voltage Channel)					
Differential Input Range [(V_{IN}+)-(V_{IN}-)]	V_{IN}	-	-	±250	mV
Input Capacitance	$C_{in}V$	-	0.2	-	pF
Effective Input Impedance	$Z_{in}V$	2	-	-	MΩ
Accuracy (Energy Outputs)					
Active Energy Linearity All Gain ranges (Note 1) Input Range 0.1% - 100%	-	-	±0.1	-	%
Full-scale Error (Note 2)	-	-	4.0	-	%FS
Offset Error (Note 2)	-	-	0.06	-	%FS

Notes: 1. Applies when the HPF option is enabled
2. Applies before system calibration. Specified as a percentage of full scale (FS).

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Currents	I_{A+} I_{D+} (VA+ = VD+ = 5 V) I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	- - -	- - -	1.3 2.9 1.7	- - -	mA mA mA
Power Consumption (Note 3)	(VA+ = VD+ = 5 V) (VA+ = 5 V, VD+ = 3.3 V)	- -	- -	21 11.6	25 -	mW mW
Power Supply Rejection Ratio (Note 4)	(50, 60 Hz) Voltage Channel (Gain = 10) Current Channel (All Gains)	PSRR	45 56	- 55 75	- - -	dB dB

Notes: 3. All outputs unloaded. All inputs CMOS level.

4. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sine wave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The “+” and “-” input pins of both input channels are shorted to VA-. Then the CS5466 is put into an internal test mode and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel’s inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$\mathrm{PSRR} = 20 \cdot \log\left\{\frac{0.150\mathrm{V}}{\mathrm{V_{eq}}}\right\}$$

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		REFOUT	+2.4	+2.5	+2.6	V
VREFOUT Temperature Coefficient	(Note 5)	TC_{VREF}	-	25	60	ppm/°C
Load Regulation	(Note 6)	ΔV_R	-	6	10	mV
Reference Input						
Input Voltage Range		VREFIN	-	+2.5	-	V
Input Capacitance		-	-	4	-	pF
Input CVF Current		-	-	70	-	nA

Notes: 5. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\left(1.0 \times 10^{6}\right)$$

6. Specified at maximum recommended output current of 1 μA, source or sink.

DIGITAL CHARACTERISTICS (Note 7)

- Min / Max characteristics and specifications are guaranteed over all operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
Master Clock Frequency	Internal Gate Oscillator	MCLK	3	4.096	5	MHz
Master Clock Duty Cycle		-	40	-	60	%
CPUCLK Duty Cycle	(Note 8 and 9)	-	40	-	60	%
Filter Characteristics						
High-pass Filter Corner Frequency	-3 dB	-	-	0.125	-	Hz
Input/Output Characteristics						
High-level Input Voltage	XIN $\overline{\text{RESET}}$	V_{IH}	(VD+) - 0.5 0.8 VD+	- -	- -	V V
Low-level Input Voltage (VD = 5 V)	XIN $\overline{\text{RESET}}$	V_{IL}	- -	- -	1.5 0.2 VD+	V V
Low-level Input Voltage (VD = 3.3 V)	XIN $\overline{\text{RESET}}$	V_{IL}	- -	- -	0.3 0.2 VD+	V V
High-level Output Voltage (except XOUT)	I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage (except XOUT)	I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF
Drive Current FOUT, $\overline{\text{E1}}$, $\overline{\text{E2}}$, NEG	(Note 10)	I_{DR}	-	50	-	mA

Notes:
7. All measurements performed under static conditions.
8. If external MCLK is used, then the duty cycle must be between 45% and 55% to maintain this specification.
9. The frequency of CPUCLK is equal to MCLK.
10. V_{OL} and V_{OH} are not specified under this condition.

SWITCHING CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times	Digital Output (Note 11)	t_{rise}	-	50	-	ns
Fall Times	Digital Output (Note 11)	t_{fall}	-	50	-	ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 12)	t_{ost}	-	60	-	ms
$\overline{E1}$ and $\overline{E2}$ Timing (Note 13 and 14)						
Period		t_1	500	-	-	ms
Pulse Width		t_2	250	-	-	ms
Rising Edge to Falling Edge		t_3	250	-	-	ms
$\overline{E1}$ Falling Edge to $\overline{E2}$ Falling Edge		t_4	250	-	-	ms
FOUT Timing (Note 13 and 14)						
Period		t_5	0.10	$1 / f_{FOUT}$		ms
Pulse Width	(Note 15)	t_6	-	0.5^*t_5	90	ms
FOUT Low		t_7	-	0.5^*t_5	-	ms

Notes: 11. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

12. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.
13. Pulse output timing is specified at MCLK = 4.096 MHz. Current and voltage signals are at unity power factor. See *"Energy Pulse Outputs"* on page 11. for more information on pulse output pins.
14. Timing is proportional to the frequency of MCLK.
15. When FREQ2 = 0, FREQ1=1 and FREQ0=1, FOUT will have a typical pulse width of 20 µs at MCLK = 4.096 MHz.

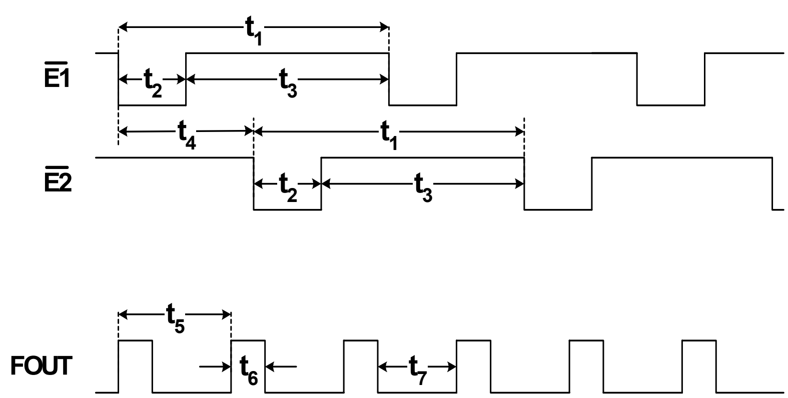


Figure 1. Timing Diagram for $\overline{E1}$, $\overline{E2}$ and FOUT (Not to Scale)

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 16 and 17)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 18, 19, 20)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 21)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 16. VA+ and AGND must satisfy {(VA+) - (AGND)} ≤ + 6.0 V.

17. VD+ and AGND must satisfy {(VD+) - (AGND)} ≤ + 6.0 V.
18. Applies to all pins including continuous over-voltage conditions at the analog input pins.
19. Transient current of up to 100 mA will not cause SCR latch-up.
20. Maximum DC input current for a power supply pin is ±50 mA.
21. Total power dissipation, including all input currents and output currents.

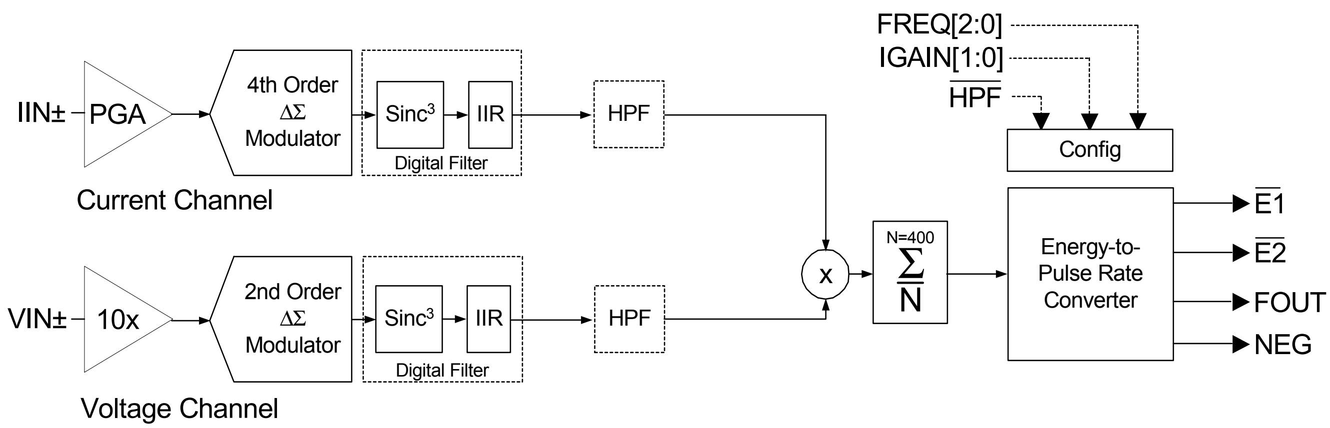


Figure 2. Data Flow

4. THEORY OF OPERATION

The CS5466 is a dual-channel analog-to-digital converter (ADC) followed by a computation engine that performs an energy-to-pulse conversion. The flow diagram for the two data paths is depicted in Figure 2. The analog inputs are structured with two dedicated channels, voltage and current, then optimized to simplify interfacing to sensing elements.

The voltage-sensing element introduces a voltage waveform on the voltage channel input VIN± and is subject to a fixed 10x gain amplifier. A second-order delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current sensing element introduces a voltage waveform on the current channel input IIN± and is subject to four programmable gains. The amplified signal is sampled by a fourth-order delta-sigma modulator for digitization. Both converters sample at a rate of MCLK / 8. The over-sampling provides a wide dynamic range and simplified anti-alias filter design.

4.1 Digital Filters

The decimating digital filters on both channels are Sinc^3 filters followed by fourth-order IIR filters. The single-bit data is passed to the low-pass decimation filter and output at a fixed word rate. The output word is passed to the IIR filter to compensate for the magnitude roll-off of the low-pass filtering operation.

An optional digital high-pass filter (*HPF* in Figure 2) removes any DC component from the selected signal path. By removing the DC component from the voltage or current channel, any DC content will also be removed from the calculated average active (real) power as well.

4.2 Active Power Computation

The instantaneous voltage and current data samples are multiplied to obtain the instantaneous power. The product is then averaged over 400 conversions to compute the active power value used to drive pulse outputs $\overline{\text{E1}}$, $\overline{\text{E2}}$, and FOUT. Output pulse rate of $\overline{\text{E1}}$ and $\overline{\text{E2}}$ can be set to one of four frequencies to directly drive a stepper motor or a electromechanical counter or interface to a microcontroller or infrared LED. The alternating output pulses of $\overline{\text{E1}}$ and $\overline{\text{E2}}$ allows for use with low-cost electromechanical counters.

Output FOUT provides a uniform pulse stream that is proportional to the active power and is designed for system calibration. The FREQ[2:0] inputs set the output pulse rate of $\overline{\text{E1}}$, $\overline{\text{E2}}$, and FOUT. See *"Energy Pulse Outputs"* on page 11. for more details.

5. FUNCTIONAL DESCRIPTION

5.1 Analog Inputs

The CS5466 is equipped with two fully differential input channels. The inputs VIN± and IIN± are designated as the voltage and current channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±250 mV_P.

5.1.1 Voltage Channel

The output of the line-voltage resistive divider or transformer is connected to the VIN+ and VIN- input pins of the CS5466. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave, the maximum RMS voltage is:

$$\frac{250mV_P}{\sqrt{2}} \cong 176.78mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage.

5.1.2 Current Channel

The output of the current-sense resistor or transformer is connected to the IIN+ and IIN- input pins of the CS5466. To accommodate different current-sensing devices, the current channel incorporates programmable gains which can be set to one of four input ranges. Input pins IGAIN1 and IGAIN0 (See Table 1) define the four gain selections and corresponding maximum input signal level.

IGAIN1	IGAIN0	Maximum Input Range	
0	0	±250mV	10x
0	1	±50mV	50x
1	0	±25mV	100x
1	1	±16.67mV	150x

Table 1. Current Channel PGA Setting

For example, if IGAIN1=IGAIN0=0, the current channel's gain is set to 10x. If the input signals are pure sinusoids with zero phase shift, the maximum peak differential signal on the current or voltage channel is ±250 mV_P. The input signal levels are approximately 70.7% of maximum peak voltage producing a full-scale energy pulse registration equal to 50% of absolute maximum energy pulse registration. This will be discussed further in Section 5.3 *Energy Pulse Outputs* on page 11.

5.2 High-pass Filter

By removing the offset from either channel, no error component will be generated at DC when computing the active power. Input pin $\overline{\text{HPF}}$ defines the three options:

- High-pass Filter (HPF) is disabled when pin $\overline{\text{HPF}}$ is connected high.
- HPF is enabled in the voltage channel when pin $\overline{\text{HPF}}$ is connected low.
- HPF is enabled in the current channel when pin $\overline{\text{HPF}}$ is connected to pin FOUT.

5.3 Energy Pulse Outputs

The CS5466 provides three output pins for energy registration. The $\overline{\text{E1}}$ and $\overline{\text{E2}}$ pins provide a simple interface from which energy can be registered. These pins are designed to directly connect to a stepper motor or electromechanical counter. The pulse rate on the $\overline{\text{E1}}$ and $\overline{\text{E2}}$ pins are in the range of 0 to 4 Hz and all frequency settings are optimized to be used with standard meter constants. The FOUT pin is designated for system calibration and the pulse rate can be selected to reach a frequency of 8000 Hz.

5.3.1 Pulse Output Format.

The CS5466 produces alternating pulses on $\overline{\text{E1}}$ and $\overline{\text{E2}}$. This pulse format is designed to drive a stepper motor. Each pin produces active-low pulses with a minimum pulse width of 250 ms when MCLK = 4.096 MHz. Refer to *"Switching Characteristics"* on page 8 for timing parameters.

The FOUT pin issues active-high pulses. The pulse width is equal to 90 ms (typical), unless the period falls below 180 ms. At this time the pulses will be equal to half the period. In mode 3 (FREQ[2:0] = 3), the pulse width of all FOUT pulses is typically 20 µs regardless of the pulse rate (MCLK = 4.096 MHz).

5.3.2 Selecting Frequency of $\overline{\text{E1}}$ and $\overline{\text{E2}}$

The pulse rate on $\overline{\text{E1}}$ and $\overline{\text{E2}}$ can be set to one of four frequency ranges. Input pins FREQ1 and FREQ0 (See Table 2) determine the maximum frequency on $\overline{\text{E1}}$ and $\overline{\text{E2}}$ for pure sinusoidal inputs with zero phase shift. As shown in Figure 1 on page 8, the frequency of $\overline{\text{E2}}$ is equal to the frequency of $\overline{\text{E1}}$ with active-low alternating pulses.

As discussed in Section 5.1.2 *Current Channel* on page 11, the maximum frequency on the $\overline{\text{E1}}$ and $\overline{\text{E2}}$ output pins is equal to the selected frequency in Table 2 if the maximum peak differential signal applied to both channels is a sine wave with zero phase shift.

Frequency Select			Maximum Frequency for a Sine Wave *(Notes 1, 2 and 3)*			
FREQ2	**FREQ1**	**FREQ0**	**$\overline{E1}$ or $\overline{E2}$**	**$\overline{E1}$+$\overline{E2}$**	**FOUT**	
0	0	0	0.125 Hz	0.25 Hz	64x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	0	1	0.25 Hz	0.5 Hz	32x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	1	0	0.5Hz	1.0 Hz	16x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	1	1	1.0 Hz	2.0 Hz	2048x($\overline{E1}$+$\overline{E2}$)	4,096 Hz
1	0	0	0.125 Hz	0.25 Hz	128x($\overline{E1}$+$\overline{E2}$)	32 Hz
1	0	1	0.25 Hz	0.5 Hz	64x($\overline{E1}$+$\overline{E2}$)	32 Hz
1	1	0	0.5 Hz	1.0 Hz	32x($\overline{E1}$+$\overline{E2}$)	32 Hz
1	1	1	1.0 Hz	2.0 Hz	16x($\overline{E1}$+$\overline{E2}$)	32 Hz

Notes: 1 A pure sinusoidal input with zero phase shift is applied to the voltage and current channel.
2 MCLK = 4.096 MHz
3 See *Figure 1 on page 8* *for $\overline{E1}$ and $\overline{E2}$ timing diagram.*

Table 2. Maximum Frequency for $\overline{E1}$, $\overline{E2}$, and FOUT

5.3.3 Selecting Frequency of FOUT

The pulse output FOUT is designed to assist with meter calibration. Using the FREQ[2:0] pins, FOUT can be set to frequencies higher than that of $\overline{E1}$ and $\overline{E2}$. The FOUT frequency is directly proportional to the $\overline{E1}$ and $\overline{E2}$ frequencies. Table 2 defines the maximum frequencies for FOUT and the dependency of FOUT on $\overline{E1}$ and $\overline{E2}$.

5.3.4 Absolute Max Frequency on $\overline{E1}$ and $\overline{E2}$

The CS5466 supports input signals on the voltage and current channels that may not be a sine wave. A typical situation of achieving the absolute maximum frequency on $\overline{E1}$ and $\overline{E2}$ would be if a 250 mV dc signal is applied to the VIN and IIN input pins. The digital high-pass filter should be disengaged by selecting $\overline{HPF}$ = 1.

The absolute maximum pulse rate observed on $\overline{E1}$ and $\overline{E2}$, determined by the FREQ[2:0] selection is defined below in Table 3.

Frequency Select			Absolute Max Frequency	
FREQ2	**FREQ1**	**FREQ0**	**$\overline{E1}$ or $\overline{E2}$**	**$\overline{E1}$+$\overline{E2}$**
x	0	0	0.25 Hz	0.5 Hz
x	0	1	0.5 Hz	1.0 Hz
x	1	0	1.0 Hz	2.0 Hz
x	1	1	2.0 Hz	4.0 Hz

Table 3. Absolute Max Frequency on $\overline{E1}$ and $\overline{E2}$

5.3.5 $\overline{E1}$ and $\overline{E2}$ Frequency Calculation

The pulse output frequency of $\overline{E1}$ and $\overline{E2}$ is directly proportional to the active power calculated from the input signals. To calculate the output frequency on $\overline{E1}$ and $\overline{E2}$, use the following transfer function:

$$FREQ_{E1,E2} = \frac{VIN \times 10 \times IIN \times IGAIN \times PF \times FREQ_{max}}{VREFIN^2}$$

$FREQ_{E1,E2}$ = Actual frequency of $\overline{E1}$ and $\overline{E2}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain selection (10, 50, 100, 150)
PF = Power Factor
$FREQ_{max}$ = Absolute Max Frequency for $\overline{E1}$ and $\overline{E2}$ [Hz]
VREFIN = Voltage at VREFIN pin [V]

Example:

For a given application, assume a 50 Hz line frequency and a purely resistive load (unity power factor), the following configuration is used:

– FREQ[2:0] = 3 ∴ $FREQ_{max}$ = 2 Hz
– IGAIN[1:0] = 2 ∴ IGAIN = 100
– VREFIN = VREFOUT = 2.5 V

In this configuration, the maximum sine wave that can be applied is 250 mVp on the voltage channel and 25 mVp on the current channel. Using the above equation, the output frequency of energy pulse $\overline{E1}$ or $\overline{E2}$ is calculated:

$$\frac{0.25V_p \times 10 \times 0.025V_p \times 100 \times 1 \times 2Hz}{\sqrt{2} \times \sqrt{2} \times 2.5V^2} = 1Hz$$

With maximum pure sinusoidal input signals, the frequency of $\overline{E1}$ or $\overline{E2}$ is half the absolute maximum frequency set with FREQ[2:0].

To calculate the frequency of FOUT for the example above, assume FREQ2 = 0.

$$FOUT = 2048 \times (\overline{E1} + \overline{E2}) = 2048 \times 2Hz = 4096Hz$$

5.4 Energy Direction Indicator

The NEG pin indicates the sign of the calculated active power. If negative active power is detected, the NEG output pin will become active-high and will remain active-high until positive active power is detected. The NEG pin is valid at least 250ns prior to any assertion of $\overline{E1}$ or $\overline{E2}$, and FOUT, to indicate the sign of a given energy output. The NEG pin is updated at a rate of 10 Hz at MCLK = 4.096 MHz.

5.5 Power-on Reset

Upon powering up, the digital circuitry is held in reset until the analog voltage reaches 4.0 V. At that time, an eight-XIN-clock-period delay is enabled to allow the oscillator to stabilize. The CS5466 will then initialize. The device reads the control pins IGAIN[1:0], FREQ[2:0] and $\overline{HPF}$, and begins performing energy measurements.

5.6 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier which can be configured as an on-chip oscillator, as shown in Figure 3. The oscillator circuit is designed to work with a quartz crystal. To reduce circuit

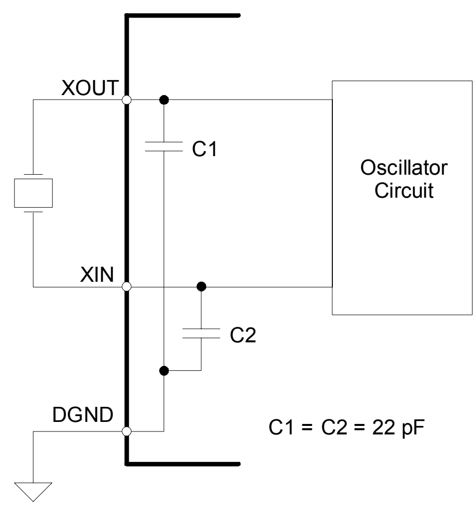


Figure 3. Oscillator Connection

cost, two load capacitors C1 and C2 are integrated in the device, one between XIN and DGND and the other between XOUT and DGND. Lead lengths to/from the crystal should be minimized to reduce stray capacitance. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS-level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

5.7 Basic Application Circuit

Figure 4 shows the CS5466 configured to measure power in a single-phase, 2-wire system while operating in a single-supply configuration. In this diagram, a shunt resistor is used to sense the line current and a voltage divider is used to sense the line voltage. In this type of shunt resistor configuration, the common-mode level of the CS5466 must be referenced to the line side of the power line. This means that the common-mode potential of the CS5466 will track the high voltage levels, as well as low voltage levels, with respect to earth ground potential.

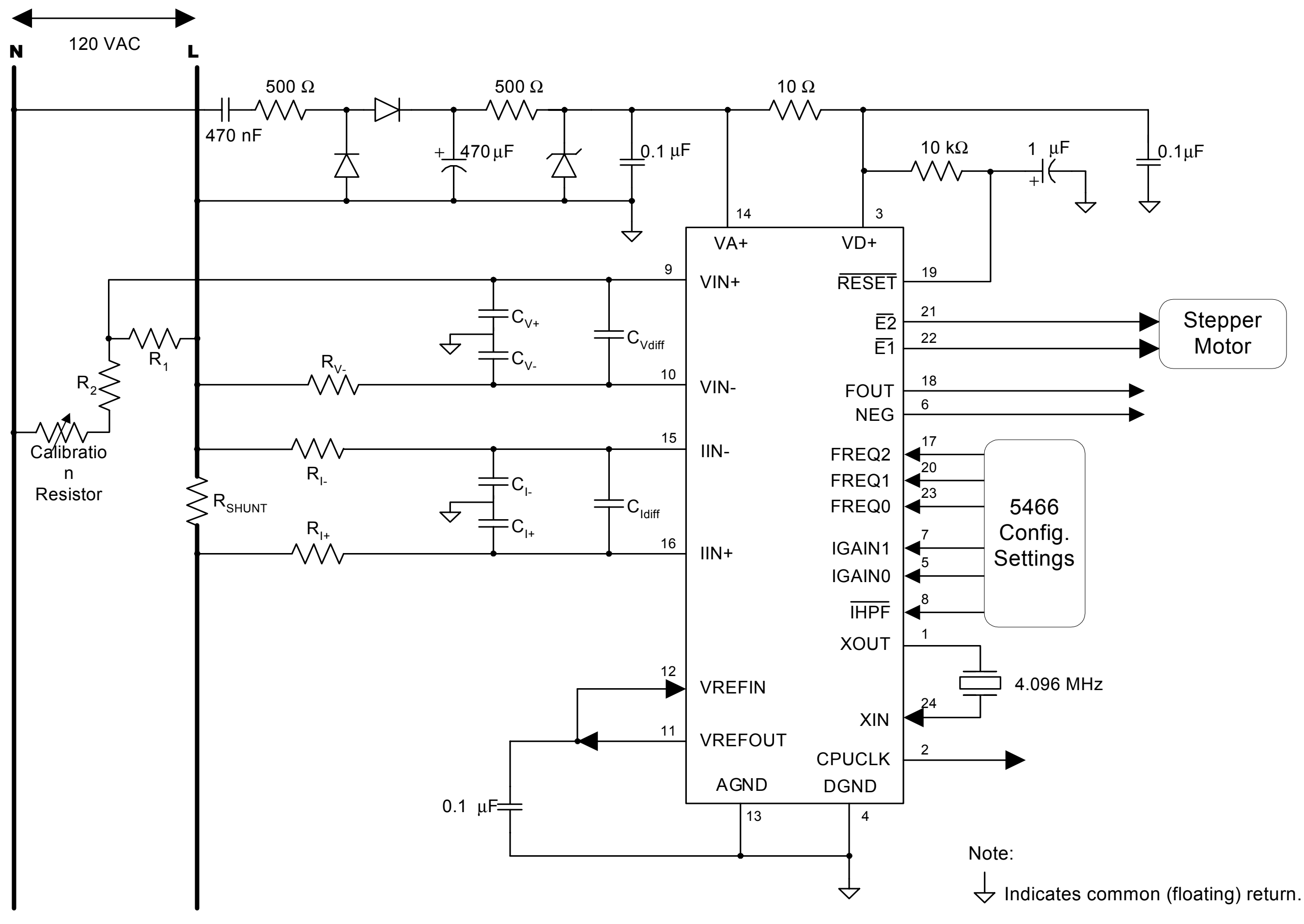
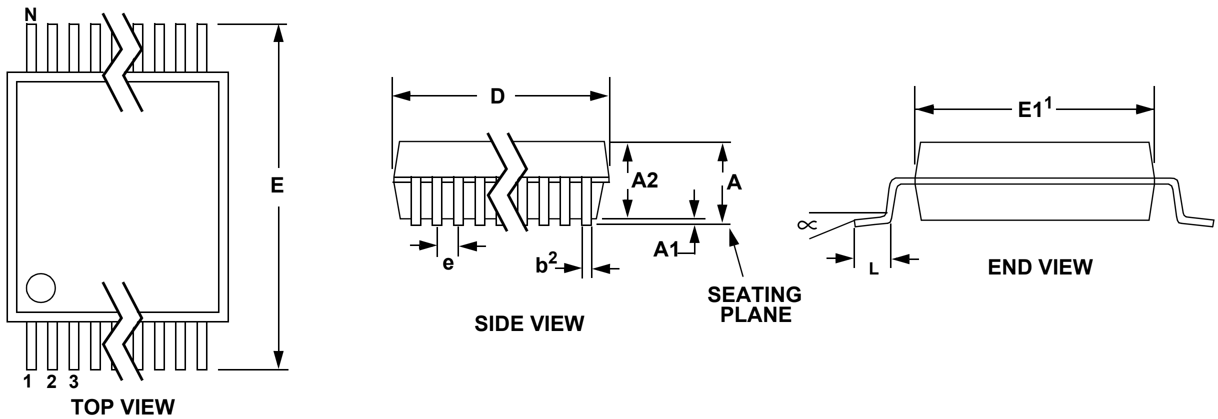


Figure 4. Typical Connection Diagram

6. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:
1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

7. ORDERING INFORMATION

Model	Temperature	Package
CS5466-IS	-40 to +85 °C	24-pin SSOP
CS5466-ISZ (lead free)		

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5466-IS	240 °C	2	365 Days
CS5466-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

9. REVISION HISTORY

Revision	Date	Changes
PP1	SEP 2004	Initial Release
PP2	OCT 2004	Corrected table heading on Page 6.
PP3	JUN 2005	Minor edits
F1	AUG	Updated with most-current characterization data. corrected energy pulse output rate equation on p13. Added MSL data.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com