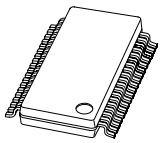


IP4777CZ38

DVI and HDMI interface ESD protection, DDC buffering, hot plug control and backdrive protection

Rev. 02 — 12 February 2009 Product data sheet

1. General description

The IP4777CZ38 is designed for HDMI transmitter host interface protection. The IP4777CZ38 includes DDC buffering and decoupling, hot plug detect, backdrive protection, CEC slew rate control, and high-level ESD protection diodes for the TMDS lines.

The DDC lines use a new buffering concept which decouples the internal capacitive load from the external capacitive load. This allows greater design flexibility of the DDC lines with respect to the maximum load of 50 pF specified in the *HDMI 1.3 specification*. This buffering also boosts the DDC signals, allowing the use of longer HDMI cables having a higher capacitive load than 700 pF. The CEC slew rate limiter prevents ringing on the CEC line. The internal hot plug detect module simplifies the application of the HDMI transmitter to control the hot plug signal.

The DDC, hot plug and CEC lines are backdrive protected to guarantee HDMI interface signals are not pulled down if the system is powered down or enters standby mode.

All TMDS intra-pairs are protected by a special diode configuration offering a low line capacitance of 0.7 pF only (to ground) and 0.05 pF between the TMDS pairs. These diodes provide protection to components downstream from ESD voltages of up to ±8 kV contact in accordance with the IEC 61000-4-2, level 4 standard.

2. Features

- HDMI 1.3 compliant
- Pb-free and RoHS compliant; Dark Green
- Robust ESD protection without degradation after several ESD strikes
- Low leakage even after several hundred ESD discharges
- Very high diode switching speed (ns) and low line capacitance of 0.7 pF to ground and 0.05 pF between channel can ensure signal integrity
- DDC capacitive decoupling between system side and HDMI connector side and buffering to drive cable with high capacitive load (> 700 pF)
- Hot plug detect module
- CEC ringing prevention by slew rate limiter
- All TMDS lines with integrated rail-to-rail clamping diodes with downstream ESD protection of ±8 kV in accordance with IEC 61000-4-2, level 4 standard
- Matched 0.5 mm trace spacing

- Highest integration in a small footprint, PCB-level, optimized RF routing, 38-pin TSSOP lead-free package

3. Applications

- The IP4777CZ38 can be used for a wide range of HDMI source devices, consumer and computing electronics e.g.:
  - SD and HD DVD player
  - Set-top box
  - PC graphic card
  - Game console
  - HDMI picture performance quality enhancer module

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4777CZ38	TSSOP38	plastic thin shrink small outline package: 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1
IP4777CZ38/V			

5. Functional diagram

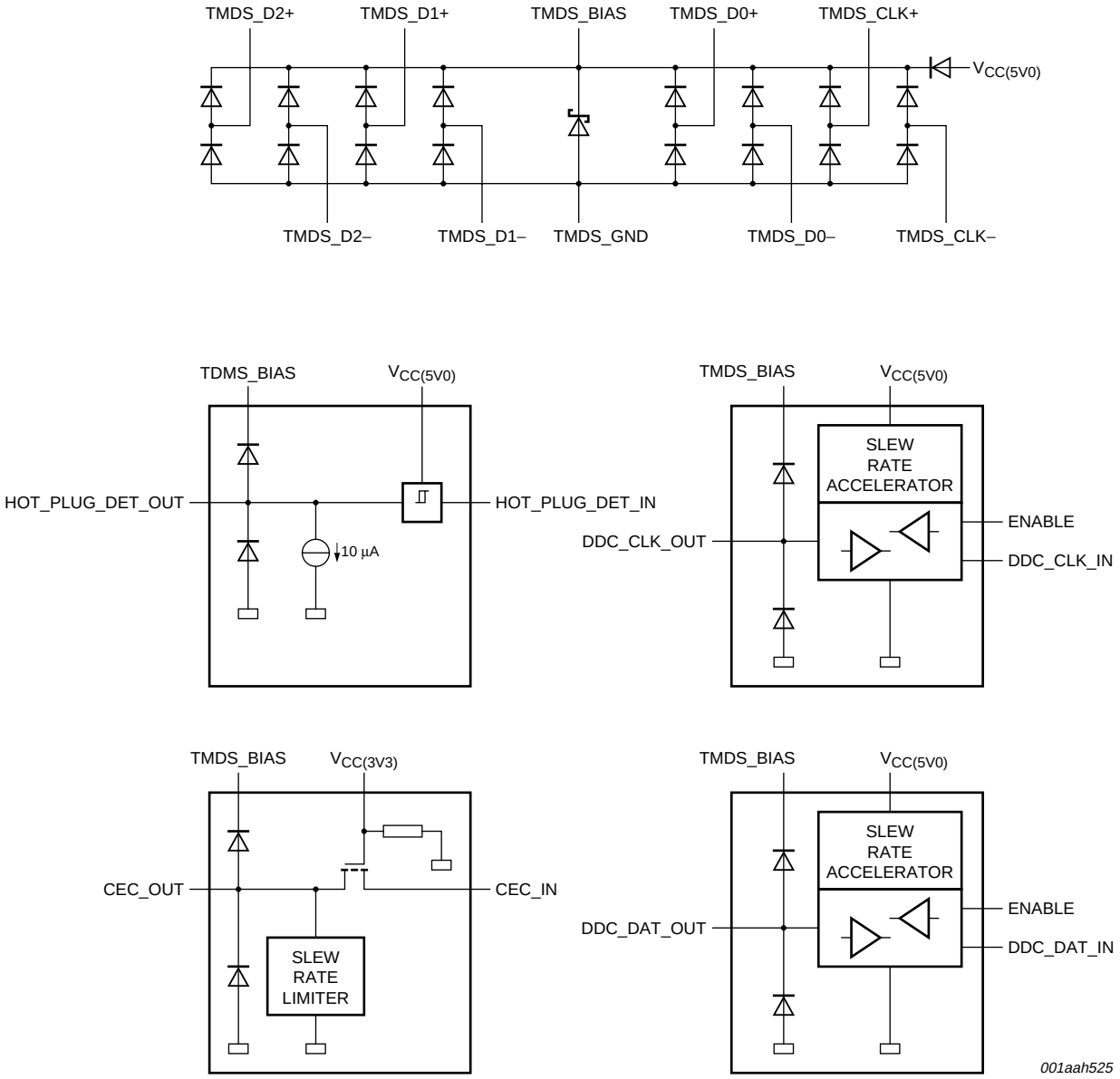


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

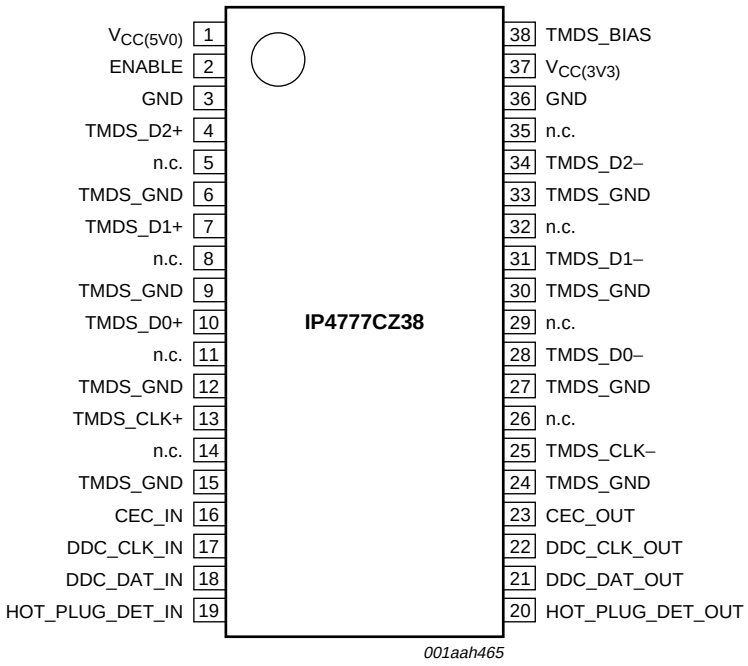


Fig 2. Pin configuration IP4777CZ38

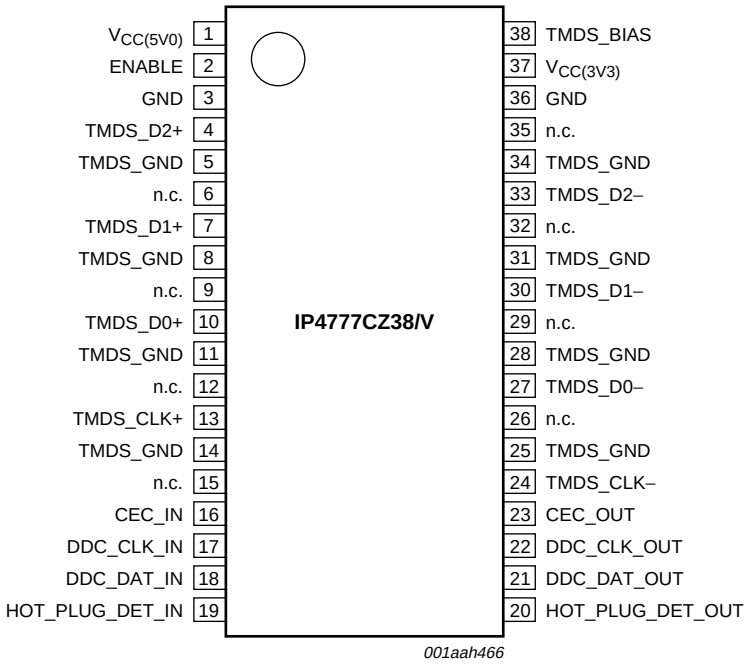


Fig 3. Pin configuration IP4777CZ38/V

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	IP4777CZ38	IP4777CZ38/V[1]	
$V_{CC(5V0)}$	1	1	supply voltage for DDC and hot plug circuits
ENABLE	2	2	enable input for DDC and hot plug circuits
GND	3	3	ground for DDC, hot plug and CEC circuits
TMDS_D2+	4	4	ESD protection TMDS channel D2+
n.c.	5	6	not connected
TMDS_GND	6	5	ground for TMDS channel
TMDS_D1+	7	7	ESD protection TMDS channel D1+
n.c.	8	9	not connected
TMDS_GND	9	8	ground for TMDS channel
TMDS_D0+	10	10	ESD protection TMDS channel D0+
n.c.	11	12	not connected
TMDS_GND	12	11	ground for TMDS channel
TMDS_CLK+	13	13	ESD protection TMDS channel CLK+
n.c.	14	15	not connected
TMDS_GND	15	14	ground for TMDS channel
CEC_IN	16	16	CEC signal input to system controller
DDC_CLK_IN	17	17	DDC clock input to system controller
DDC_DAT_IN	18	18	DDC data input to system controller
HOT_PLUG_DET_IN	19	19	hot plug detect input from system GPIO
HOT_PLUG_DET_OUT	20	20	hot plug detect output to HDMI connector
DDC_DAT_OUT	21	21	DDC data output to HDMI connector
DDC_CLK_OUT	22	22	DDC clock output to HDMI connector
CEC_OUT	23	23	CEC signal output to HDMI connector
TMDS_GND	24	25	ground for TMDS channel
TMDS_CLK–	25	24	ESD protection TMDS channel CLK–
n.c.	26	26	not connected
TMDS_GND	27	28	ground for TMDS channel
TMDS_D0–	28	27	ESD protection TMDS channel D0–
n.c.	29	29	not connected
TMDS_GND	30	31	ground for TMDS channel
TMDS_D1–	31	30	ESD protection TMDS channel D1–
n.c.	32	32	not connected
TMDS_GND	33	34	ground for TMDS channel
TMDS_D2–	34	33	ESD protection TMDS channel D2–
n.c.	35	35	not connected

Table 2. Pin description *…continued*

Symbol	Pin		Description
	IP4777CZ38	IP4777CZ38/V[1]	
GND	36	36	ground for DDC, hot plug and CEC circuits
$V_{CC(3V3)}$	37	37	supply voltage for CEC circuit
TMDS_BIAS	38	38	bias input for TMDS ESD protection. This pin must be connected to a 0.1 µF capacitor.

[1] Type number IP4777CZ38/V is pin compatible with type number IP4776CZ38.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			GND – 0.5	5.5	V
V_I	input voltage	input pins		GND – 0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	connector side pins (to ground); IEC 61000-4-2, level 4 (contact)	[1]	–8	+8	kV
		board side pins; IEC 61000-4-2, level 1 (contact)	[2]	–2	+2	kV
P_{tot}	total power dissipation	DDC operating at 100 kHz		-	14	mW
T_{stg}	storage temperature			–55	+125	°C

[1] Connector side pins:
TMDS_D2+, TMDS_D2–, TMDS_D1+, TMDS_D1–, TMDS_D0+, TMDS_D0–
TMDS_CLK+, TMDS_CLK–
CEC_OUT
DDC_DAT_OUT and DDC_CLK_OUT
HOT_PLUG_DET_OUT

[2] Board side pins:
CEC_IN
DDC_DAT_IN and DDC_CLK_IN
HOT_PLUG_DET_IN
ENABLE

8. Static characteristics

Table 4. TMDS protection circuit

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Zener diode							
V_{BRzd}	Zener diode breakdown voltage	I = 1 mA		6	-	9	V
R_{dyn}	dynamic resistance	I = 1 A; IEC 61000-4-5/9					
		positive transient		-	2.4	-	Ω
		negative transient		-	1.3	-	Ω
Protection diode							
I_{bck}	back current	from pins TMDS_x to pin TMDS_BIAS; $V_{CC(5V0)}$ = 0 V; $V_{CC(3V3)}$ = 0 V		-	0.1	1	µA
$I_{L(r)}$	reverse leakage current	V_I = 3.0 V		-	1	-	µA
V_F	forward voltage			-	0.7	-	V
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV per IEC 61000-4-2; voltage 30 ns after trigger		-	8	-	V
TMDS channel: pins TMDS_x							
$C_{ch(TMDS)}$	TMDS channel capacitance	$V_{CC(5V0)}$ = 5 V; f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.7	-	pF
$\Delta C_{ch(TMDS)}$	TMDS channel capacitance difference	$V_{CC(5V0)}$ = 5 V; f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.05	-	pF
$C_{ch(mutual)}$	mutual channel capacitance	between signal pin TMDS_x and pin n.c.; $V_{CC(5V0)}$ = 0 V; f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.07	-	pF

[1] This parameter is guaranteed by design.

Table 5. DDC circuit

$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies: pins $V_{CC(5V0)}$ and $V_{CC(3V3)}$						
$V_{CC(5V0)}$	supply voltage (5.0 V)	connector side	4.5	5.0	5.5	V
$V_{CC(3V3)}$	supply voltage (3.3 V)	board side	2.7	3.3	5.5	V
$I_{CC(5V0)}$	supply current (5.0 V)	$V_{CC(5V0)}$ = 5.5 V; both channels HIGH: DDC_DAT_OUT = $V_{CC(5V0)}$; DDC_CLK_OUT = $V_{CC(5V0)}$	-	1.4	2.5	mA
		$V_{CC(5V0)}$ = 5.5 V; both channels LOW: DDC_DAT_IN = GND; DDC_CLK_IN = GND; DDC_DAT_OUT = open; DDC_CLK_OUT = open	-	1.4	2.5	mA
$I_{CC(3V3)}$	supply current (3.3 V)	no pull-up resistor connected to $V_{CC(3V3)}$	-	-	0.1	µA

Table 5. DDC circuit *…continued*

$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: pins DDC_CLK_IN and DDC_DAT_IN						
Used as input						
V_{IH}	HIGH-level input voltage		-	410	-	mV
V_{IL}	LOW-level input voltage		-	400	-	mV
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-	70	µA
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.2	V
I_{LI}	input leakage current	V_I = 3.6 V	-	-	±1	µA
C_i	input capacitance	V_I = 3 V or 0 V				
		$V_{CC(3V3)}$ = 3.3 V	-	6	7	pF
		$V_{CC(3V3)}$ = 3.0 V	-	6	7	pF
Used as output						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA or 3 mA	-	700	-	mV
I_{OH}	HIGH-level output current	V_O = 3.6 V	-	-	10	µA
C_o	output capacitance	V_I = 3 V or 0 V				
		$V_{CC(3V3)}$ = 3.3 V	-	6	7	pF
		$V_{CC(3V3)}$ = 3.0 V	-	6	7	pF
Connector side: pins DDC_CLK_OUT and DDC_DAT_OUT						
Used as input						
V_{IH}	HIGH-level input voltage		$0.7 \times V_{CC(5V0)}$	-	5.5	V
V_{IL}	LOW-level input voltage		–0.5	-	$0.3 \times V_{CC(5V0)}$	V
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-	1	µA
V_{IK}	input clamping voltage	I_I = –18 mA	-	-	–1.2	V
I_{LI}	input leakage current	V_I = 3.6 V	-	-	±1	µA
C_i	input capacitance	V_I = 3 V or 0 V				
		$V_{CC(3V3)}$ = 3.3 V	-	8	10	pF
		$V_{CC(3V3)}$ = 3.0 V	-	8	10	pF
Used as output						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA or 6 mA	-	200	-	mV
I_{OH}	HIGH-level output current	V_O = 3.6 V	-	-	10	µA
C_o	output capacitance	V_I = 3 V or 0 V				
		$V_{CC(3V3)}$ = 3.3 V	-	8	10	pF
		$V_{CC(3V3)}$ = 3.0 V	-	8	10	pF

Table 6. CEC circuit

$V_{CC(3V3)}$ = 2.7 V o 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Board side: input pin CEC_IN							
$C_{I(ch-GND)(levsh)}$	level shifting input capacitance from channel to ground	$V_{CC(3V3)}$ = 0 V; f = 1 MHz; V_{bias} = 2.5 V	[1]	-	14	16	pF
SR_r	rising slew rate	V_I > 1.8 V		-	10	-	mV/µs
N-FET							
ΔV_{on}	on-state voltage drop	N-FET state = on; $V_{CC(3V3)}$ = 2.5 V; V_S = GND; I_{DS} = 3 mA		-	125	140	mV
Connector side: output pin CEC_OUT							
I_{LO}	output leakage current	V_{bias} = 3.6 V		-	-	0.1	µA
R_{dyn}	dynamic resistance	I = 1 A; IEC 61000-4-5/9					
		positive transient		-	2.4	-	Ω
		negative transient		-	1.3	-	Ω
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV per IEC 61000-4-2; voltage 30 ns after trigger; T_{amb} = 25 °C		-	8	-	V

[1] This parameter is guaranteed by design.

Table 7. Enable circuit

$V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: input pin ENABLE[1]						
V_{IH}	HIGH-level input voltage	HIGH = enable	0.7 × $V_{CC(3V3)}$	-	$V_{CC(3V3)}$ + 0.5	V
V_{IL}	LOW-level input voltage	LOW = disable	–0.5	-	0.3 × $V_{CC(3V3)}$	V
I_{IL}	LOW-level input current	V_I = 0.2 V; $V_{CC(3V3)}$ = 5.5 V	-	10	-	µA
I_{LI}	input leakage current	V_{bias} = 3.6 V	–1	+0.1	+1	µA
C_i	input capacitance	V_I = 3 V or 0 V	-	3	7	pF

[1] The ENABLE pin has to be connected permanently to $V_{CC(3V3)}$ if no enable control is needed.

Table 8. Hot plug control circuit

$V_{CC(5V0)}$ = 4.5 V to 5.5 V; $V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Board side: input pin HOT_PLUG_DET_OUT						
V_{IH}	HIGH-level input voltage		-	1.9	-	V
V_{IL}	LOW-level input voltage		-	200	-	mV
I_{IL}	LOW-level input current	pull-down current to ground; V_I = 2 V; $V_{CC(5V0)}$ = 5.5 V	-	10	-	µA
C_i	input capacitance	V_I = 3 V or 0 V	-	6	7	pF

Table 8. Hot plug control circuit *...continued*

$V_{CC(5V0)}$ = 4.5 V to 5.5 V; $V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Connector side: output pin HOT_PLUG_DET_IN						
V_{IH}	HIGH-level output voltage		-	$V_{CC(3V3)}$	-	V

9. Dynamic characteristics

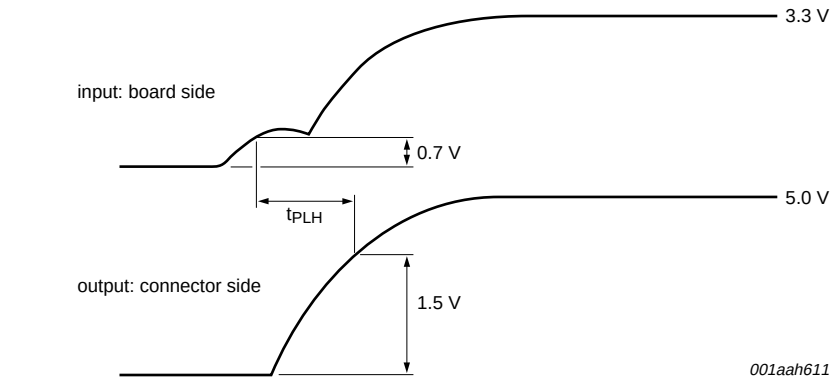
Table 9. DDC circuits

$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

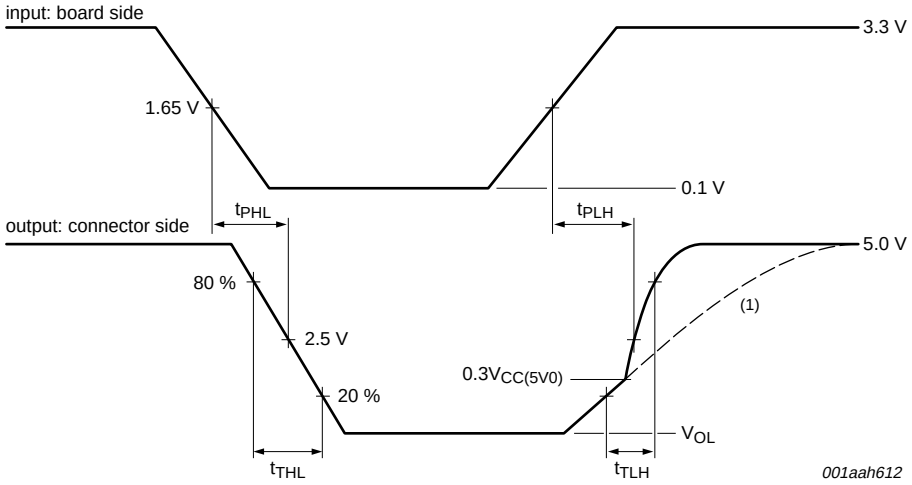
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Board side to connector side; see Figure 4							
Pins DDC_CLK_IN to DDC_CLK_OUT and DDC_DAT_IN to DDC_DAT_OUT							
t_{PLH}	LOW-to-HIGH propagation delay		[1]	275	300	325	ns
t_{PHL}	HIGH-to-LOW propagation delay		[1]	195	210	225	ns
Pins DDC_CLK_OUT and DDC_DAT_OUT							
t_{TLH}	LOW to HIGH transition time	R_L =1.35 kΩ; C_L = 50 pF		90	110	130	ns
t_{THL}	HIGH to LOW transition time		[1]	1	3	5	ns
Connector side to board side; see Figure 5							
Pins DDC_CLK_OUT to DDC_CLK_IN and DDC_DAT_OUT to DDC_DAT_IN							
t_{PLH}	LOW-to-HIGH propagation delay			110	130	150	ns
t_{PHL}	HIGH-to-LOW propagation delay		[1]	20	30	40	ns
Pins DDC_CLK_IN and DDC_DAT_IN							
t_{TLH}	LOW to HIGH transition time			100	120	140	ns
t_{THL}	HIGH to LOW transition time		[1]	2	3	5	ns
Enable: pin ENABLE							
t_{su}	set-up time	pin ENABLE = HIGH before start condition	[2]	100	-	-	ns
t_h	hold time	pin ENABLE = HIGH after stop condition	[2]	100	-	-	ns

[1] Typical values are measured at $V_{CC(3V3)}$ = 3.3 V, $V_{CC(5V0)}$ = 5.0 V and T_{amb} = 25 °C.

[2] The ENABLE pin should only change when the DDC bus is in an idle state.



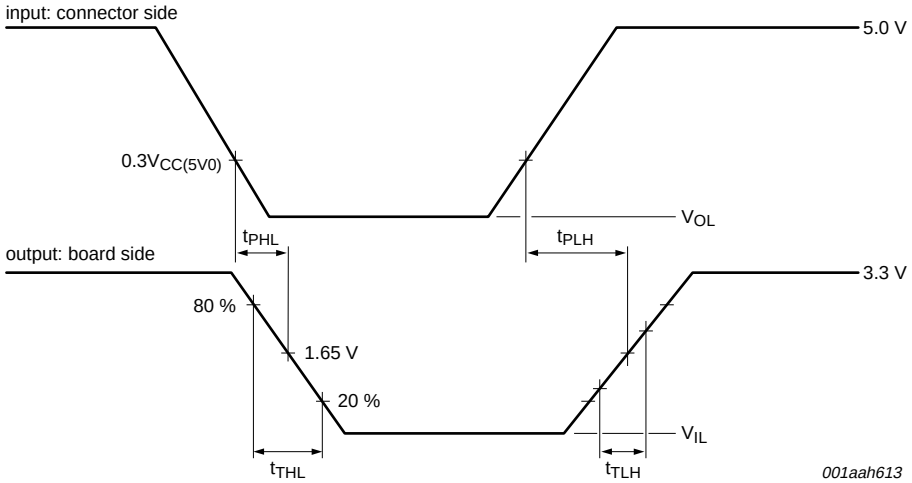
a. Propagation delay t_{PLH}



(1) Dotted line indicates effect without slew rate accelerator.

b. Propagation delay t_{PHL} and transition time

Fig 4. Board side to connector side operation



Propagation delay output to input and transition time input

Fig 5. Connector side to board side operation

10. Application information

10.1 TMDS

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, the IP4777CZ38 provides ESD protection with a low capacitive load. The dominant value for the TMDS line impedance is the capacitive load to ground. The IP4777CZ38 has a capacitive load of only 0.7 pF.

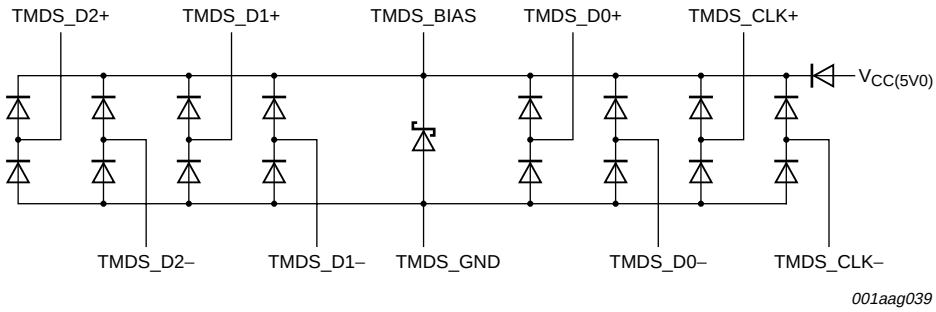


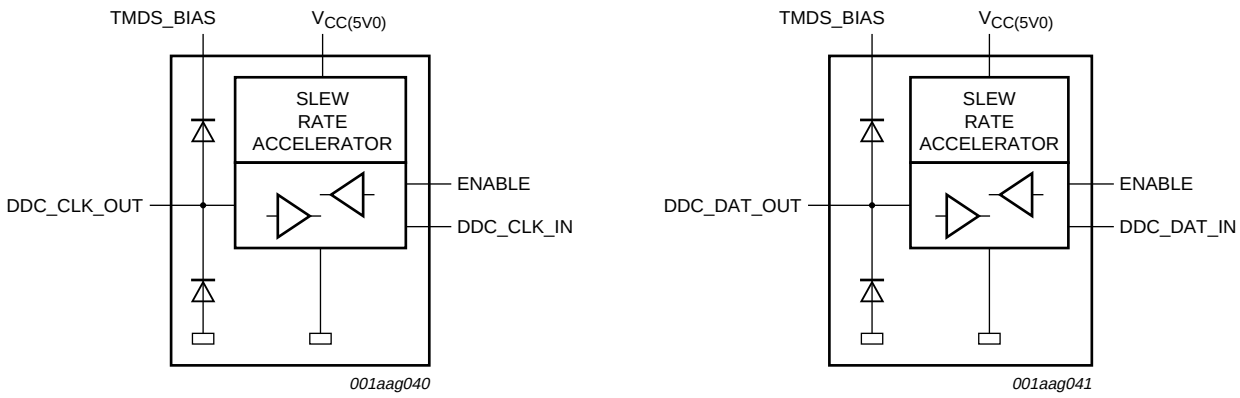
Fig 6. ESD protection of TMDS lines

10.2 DDC circuit

The DDC bus circuit contains full capacitive decoupling between the HDMI connector and the DDC bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is within the 50 pF maximum of the HDMI specification.

The slew rate accelerator supports high capacitive load on the HDMI cable side. Various HDMI cable suppliers produce low-cost and long (typically 25 m) HDMI cables with a capacitive load of up to 6 nF.

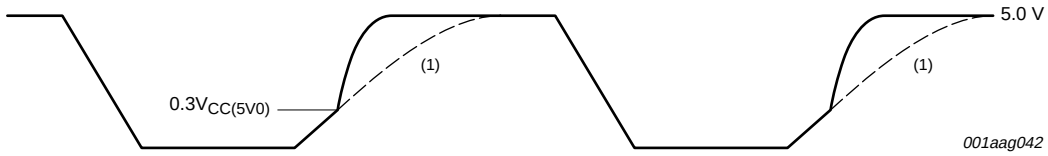
The slew rate accelerator boosts the DDC signal independent of which side of the bus is releasing the signal. The DDC circuit provides a level shifting option. The ENABLE signal is enabling and disabling the complete DDC buffer.



a. DDC clock

b. DDC data

Fig 7. DDC circuit



(1) Dotted line indicates effect without slew rate accelerator.

Fig 8. DDC output waveform

10.3 Hot plug detect circuit

The IP4777CZ38 includes a hot plug detect circuit that simplifies the hot plug application. The circuit generates a standard logic level from the hot plug signal.

The hot plug detect circuit is pulling down the signal to avoid any floating signal. The comparator guarantees a save detection of the 2 V hot plug signal without any glitches and oscillation at the hot plug output.

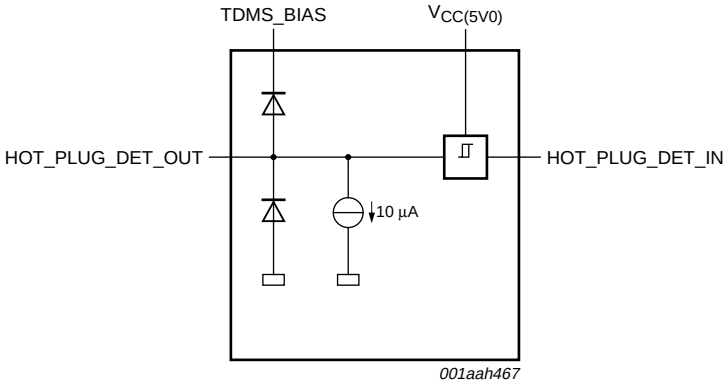


Fig 9. Hot plug detect circuit

10.4 CEC

The CEC signal can generate distortions caused by signal ringing in a 1 kHz domain. The CEC slew rate limiter ensures that a signal does not ring independently of the CEC slave that is releasing the signal.

A MOSFET transistor implements the backdrive protection which blocks signals in a power-down state.

The slew rate of the CEC bus is controlled by a slew rate that is defined independently of the load (resistive and capacitive) at the CEC bus.

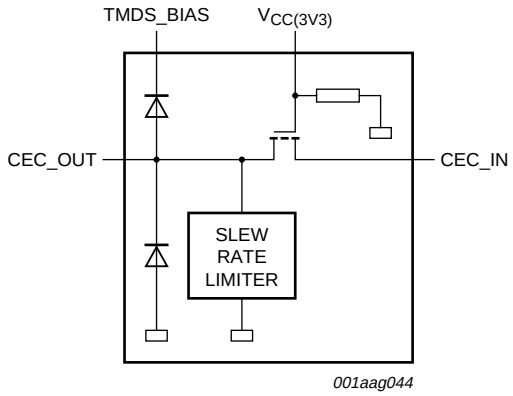
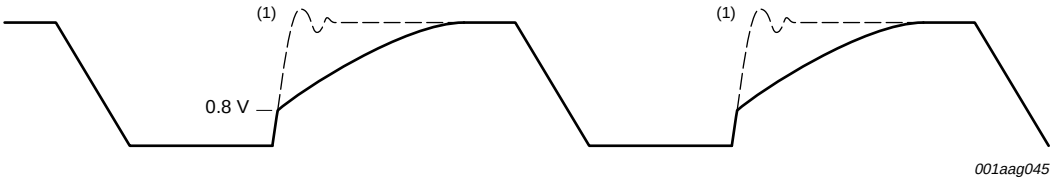


Fig 10. CEC module



(1) Dotted line indicates effect without slew rate limiter.

Fig 11. CEC output waveform

10.5 Backdrive protection

The HDMI contains various signals which can partly supply current into an HDMI device that is powered down.

Typically, the DDC lines and the CEC signals can force 5 V into the switched off device. The IP4777CZ38 ensures that at power-down, the critical signals are blocked to prevent any damage to the HDMI sink and HDMI source.

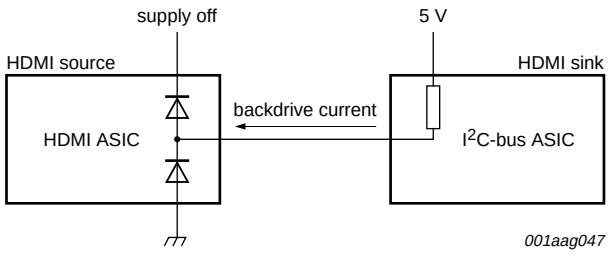


Fig 12. Backdrive protection

10.6 Schematic view of application

Only a few external components are needed at the application to adapt the HDMI port to the parameters of the HDMI transmitter device.

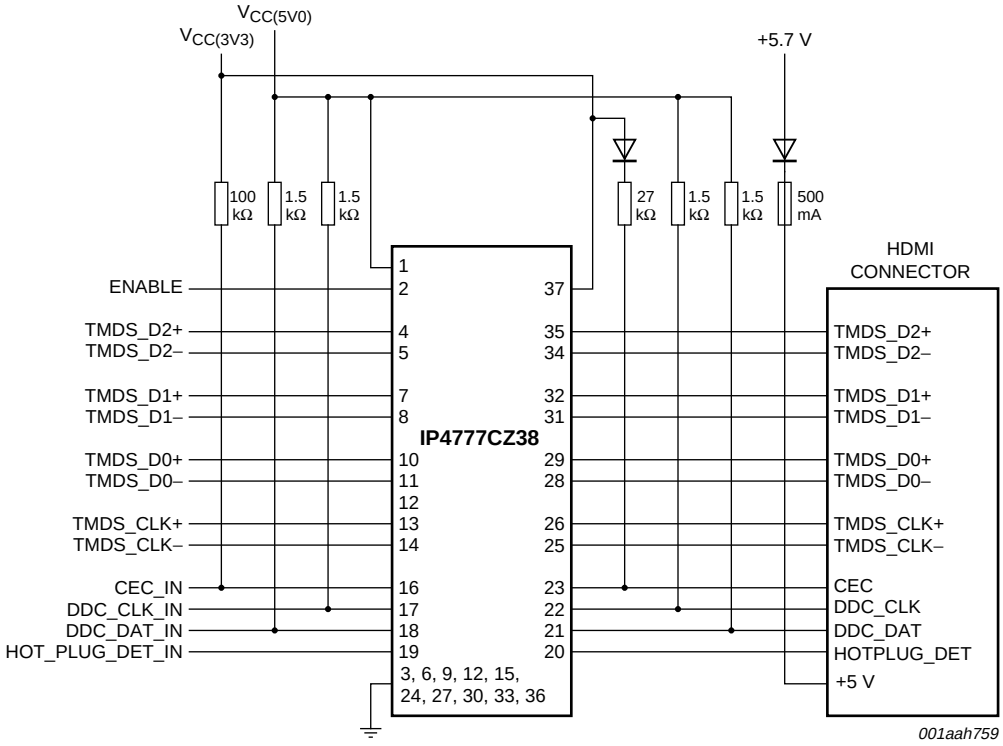


Fig 13. Schematic view of IP4777CZ38 application

10.7 Typical application

The optimized pinning variant simplifies the printed-circuit board design. The pinning optimizes the design of the microstrip lines for defined impedance.

Underneath the device a solid ground plane is part of the microstrip lines.

This application requires only a few external components to adapt the HDMI port to the parameters of the HDMI transmitter device or HDMI multiplexer.

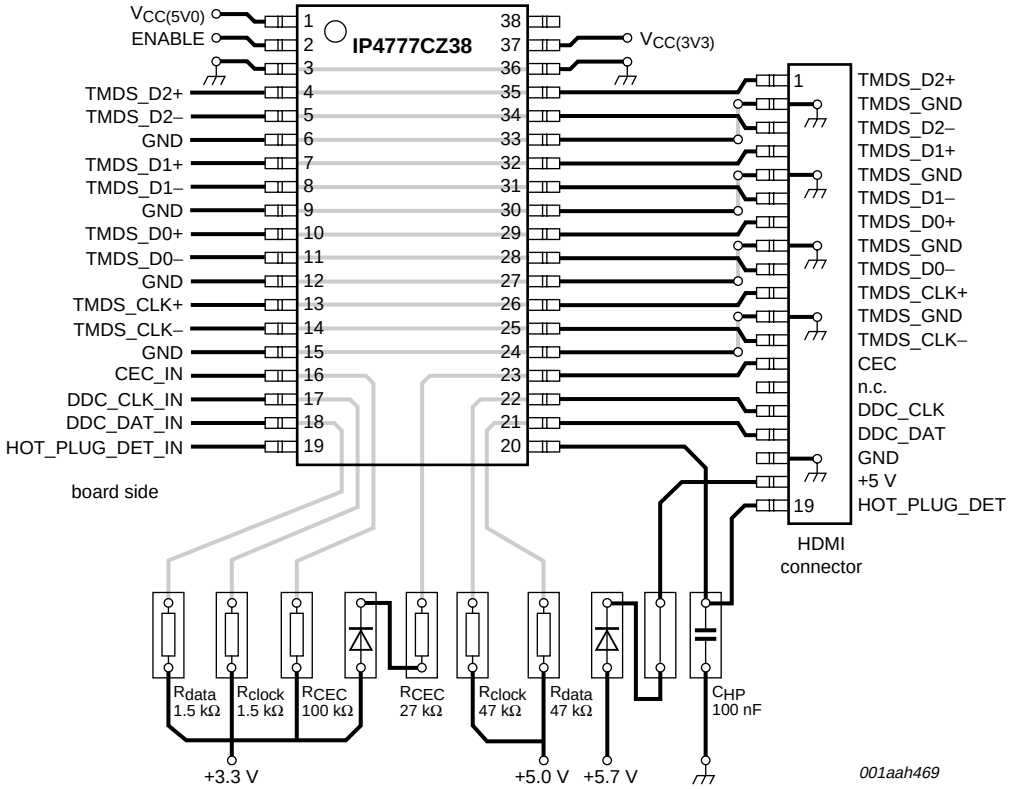
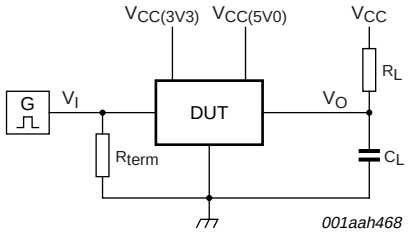


Fig 14. Application of the IP4777CZ38 showing optimized PCB microstrip lines

11. Test information



See Table 10 for test data.

R_{term} = termination resistance should be equal to output impedance Z_o of the pulse generator.

R_L = load resistance.

C_L = load capacitance.

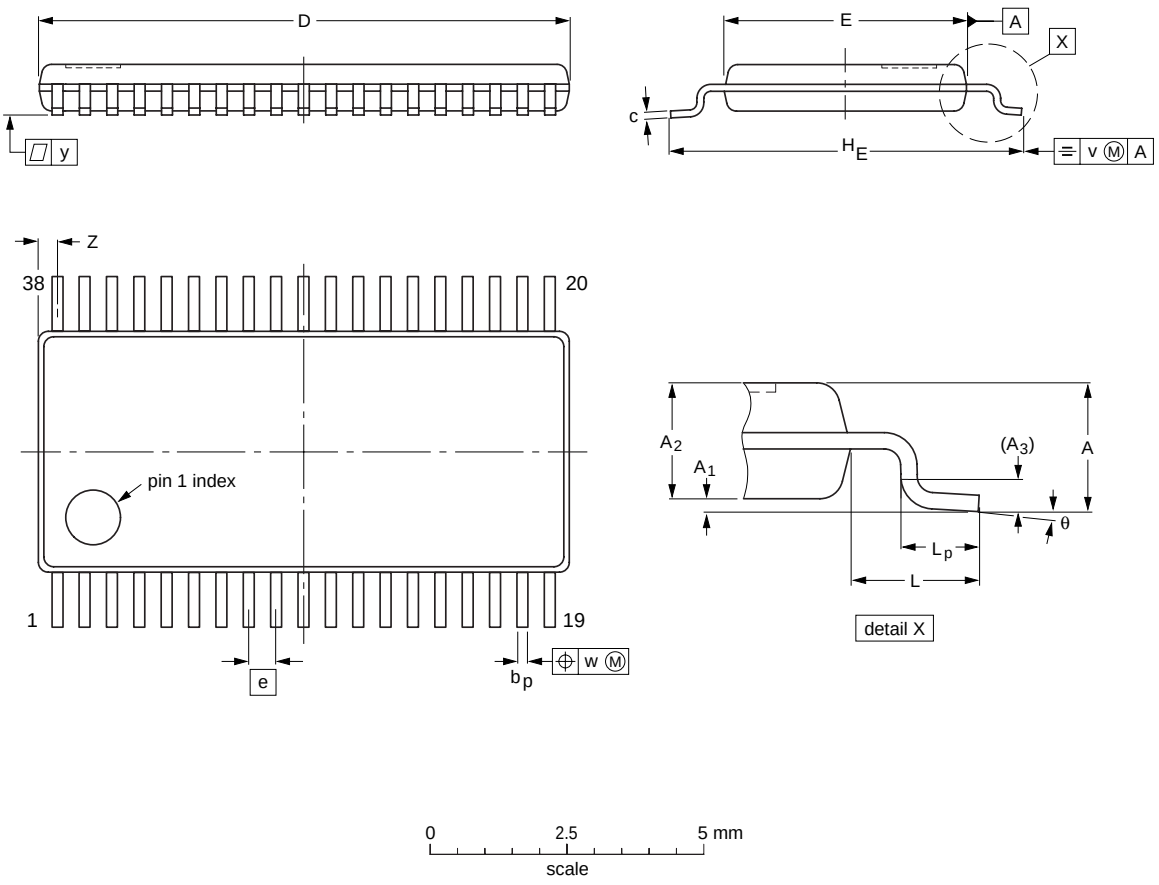
Fig 15. Test circuit for DDC and CEC lines

Table 10. Test data

Test	R_L	C_L	V_{CC}
DDC lines	1.35 kΩ	50 pF	$V_{CC(5V0)}$
CEC line	27 kΩ	50 pF	$V_{CC(3V3)}$

12. Package outline

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm **SOT510-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.27 0.17	0.20 0.09	9.8 9.6	4.5 4.3	0.5	6.4	1	0.7 0.5	0.2	0.08	0.08	0.49 0.21	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT510-1		MO-153				~~03-02-18~~ 05-11-02

Fig 16. Package outline SOT510-1 (TSSOP38)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

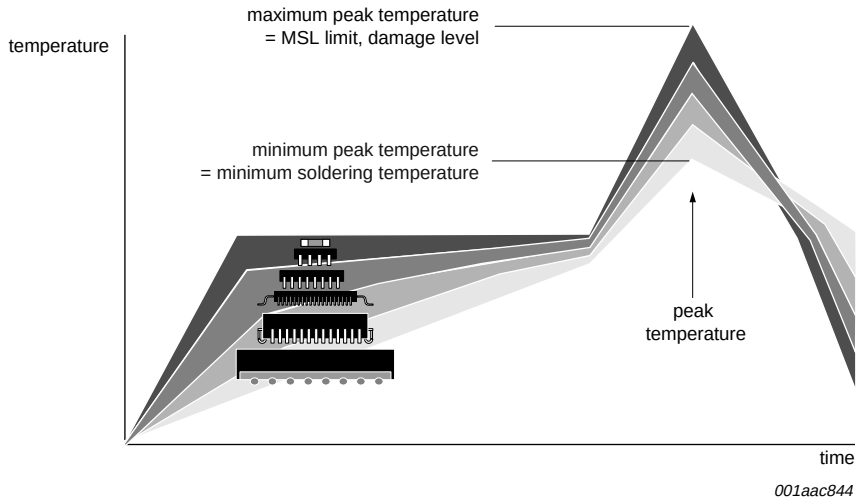
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuit
CEC	Consumer Electronic Control
DDC	Data Display Channel
DVD	Digital Versatile Disc
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input Output
HD	High Definition
HDMI	High Definition Multimedia Interface
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
RoHS	Restriction of the use of certain Hazardous Substances
SD	Standard Definition
TMDS	Transition Minimized Differential Signaling

15. Glossary

HDMI sink — Device which receives HDMI signals e.g. a TV set.

HDMI source — Device which transmit HDMI signal e.g. DVD player.

16. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4777CZ38_2	20090212	Product data sheet	-	IP4777CZ38_1
Modifications:	• Table 3: updated value of P_{tot}. • Table 5: updated values. • Table 6: updated values. • Table 7: updated values. • Table 8: updated values and removed last four rows. • Table 9: updated values.			
IP4777CZ38_1	20080415	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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