3.3V SDRAM Buffer for Mobile PCS with 4 SO-DIMMs

Features

- One input to 10 output buffer/driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- Serial interface for output control
- Low skew outputs
- Up to 133MHz operation
- Multiple V_{DD} and V_{SS} pins for noise reduction
- Dedicated OE pin for testing
- Space-saving 28 Pin SSOP package
- 3.3V operation

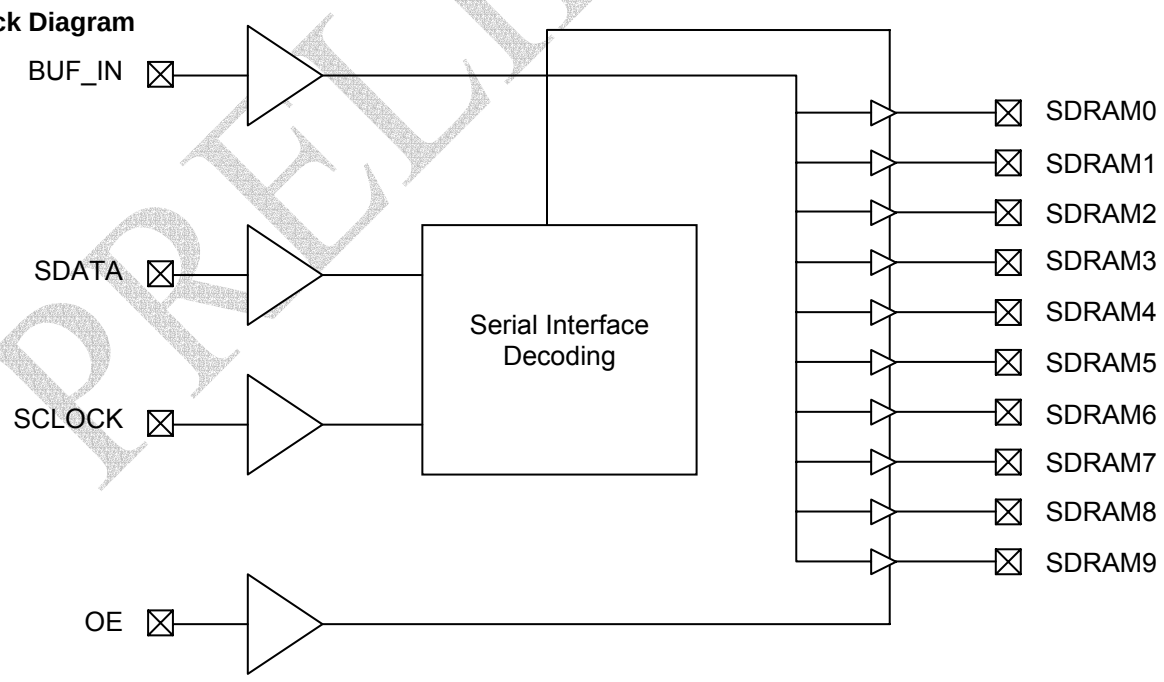
Functional Description

The PCS2I2310ANZ is a 3.3V buffer designed to distribute high-speed clocks in mobile PC applications. The part has 10 outputs, 8 of which can be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133MHz, thus making it compatible with Pentium II[®i] processors.

The PCS2I2310ANZ also includes a serial interface (IIC), which can enable or disable each output clock. The IIC is Slave Receiver only and is Standard mode compliant. IIC Master can write into the IIC registers but cannot read back. The first two bytes after address should be ignored by IIC Block and data is valid after these two bytes as given in IIC Byte Flow Table. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

[i] Pentium II is a registered trademark of Intel Corporation

Block Diagram



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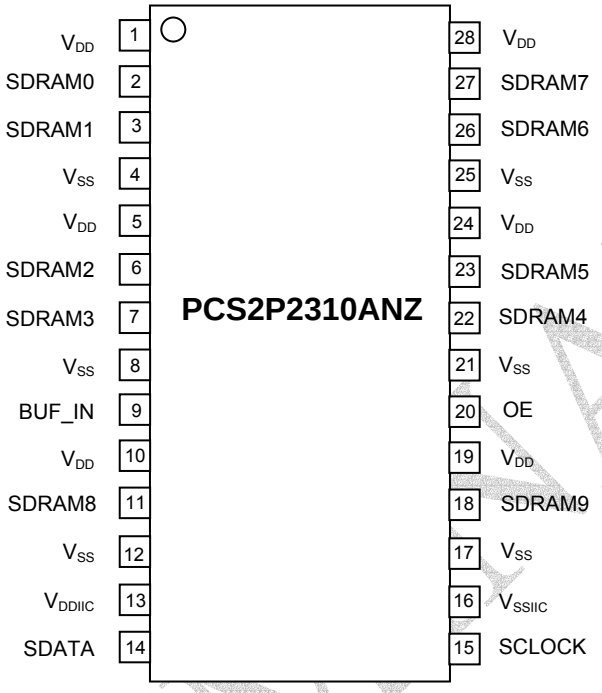
Pin Configuration

28 Pin SSOP Package-- Top View



28 pin SSOP

Pin Description

Pins	Name	Type	Description
1, 5, 10, 19, 24, 28	V_{DD}	P	3.3V Digital voltage supply
4, 8, 12, 17, 21, 25	V_{SS}	P	Ground
13	V_{DDIIC}	P	3.3V Serial interface voltage supply
16	V_{SSIIC}	P	Ground for serial interface
9	BUF_IN	I	Input clock, 5V tolerant
20	OE	I	Output Enable, three-states outputs when LOW. Internal pull-up to V_{DD}
14	SDATA	I/O	Bi-directional Serial data pin. Internal pull-up to $V_{DD.}$ 5V tolerant
15	SCLK	I	Serial clock input. Internal pull-up to $V_{DD.}$ 5V tolerant
2, 3, 6, 7	SDRAM [0–3]	O	SDRAM byte 0 Clock Outputs
22, 23, 26, 27	SDRAM [4–7]	O	SDRAM byte 1 Clock Outputs
11, 18	SDRAM [8–9]	O	SDRAM byte 2 Clock Outputs

Device Functionality

OE	SDRAM [0–17]
0	High-Z
1	1 x BUF_IN

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits can be programmed to either "0" or "1".
- Serial interface address for the PCS2I2310ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: SDRAM Active/Inactive Register[1]
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	--	Unused
Bit 6	--	Unused
Bit 5	--	Unused
Bit 4	--	Unused
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Byte 1: SDRAM Active/Inactive Register[1]
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	--	Unused
Bit 2	--	Unused
Bit 1	--	Unused
Bit 0	--	Unused

Byte 2: SDRAM Active/Inactive Register[1]
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	--	Reserved
Bit 4	--	Reserved
Bit 3	--	Reserved
Bit 2	--	Reserved
Bit 1	--	Reserved
Bit 0	--	Reserved

Note 1 : When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

IIC Byte Flow

Byte	Description
1	IIC Address
2	Command (dummy value, ignored)
3	Byte Count (dummy value, ignored)
4	IIC Data Byte 0
5	IIC Data Byte 1
6	IIC Data Byte 2

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage to Ground Potential	-0.5V to +7.0	V
V_{IN}	DC Input Voltage (Except BUF_IN)	-0.5V to V_{DD} + 0.5	V
V_{INB}	DC Input Voltage (BUF_IN)	-0.5V to +7.0	V
T_{STG}	Storage Temperature	-65°C to +150	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2000	V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance	20	30	pF
C_{IN}	Input Capacitance		7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage	Except serial interface pins			0.8	V
V_{ILIIC}	Input LOW Voltage	For serial interface pins only			0.7	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{OL}	Output LOW Voltage[1]	I_{OL}= 25 mA			0.4	V
V_{OH}	Output HIGH Voltage[1]	I_{OH} = –36 mA	2.4			V
I_{CC}	Quiescent Supply Current	V_{DD}= 3.465V, V_i = V_{DD} or GND I_O =0		50	100	µA
I_{OZ}	High Impedance Output Current	V_{DD}= 3.465V, V_i = V_{DD} or GND			±10	µA
I_{OFF}	OffState Current (for SCL ,SDATA)	V_{DD}= 0V, V_i = 0V or 5.5V			50	µA
ΔI_{CC}	Change in Supply Current	V_{DD}= 3.135V to 3.465V One Input at V_{DD}-0.6, All other Inputs at V_{DD} or GND			500	µA
I_i	Input Leakage	V_{DD}= 3.465V or GND (Applicable to all Input Pins)	-5		+5	µA
I_{DD}	Supply Current[1]	Unloaded outputs, 133MHz			266	mA
I_{DD}	Supply Current[1]	Loaded outputs, 30pF, 133MHz			360	mA
I_{DD}	Supply Current[1]	Unloaded outputs, 100MHz			200	mA
I_{DD}	Supply Current[1]	Loaded outputs, 30pF,100MHz			290	mA
I_{DD}	Supply Current[1]	Unloaded outputs, 66.67MHz			150	mA
I_{DD}	Supply Current[1]	Loaded outputs, 30pF ,66.67MHz			185	mA
I_{DDS}	Supply Current	BUF_IN=V_{DD} or V_{SS}, all other inputs at V_{DD}			500	µA

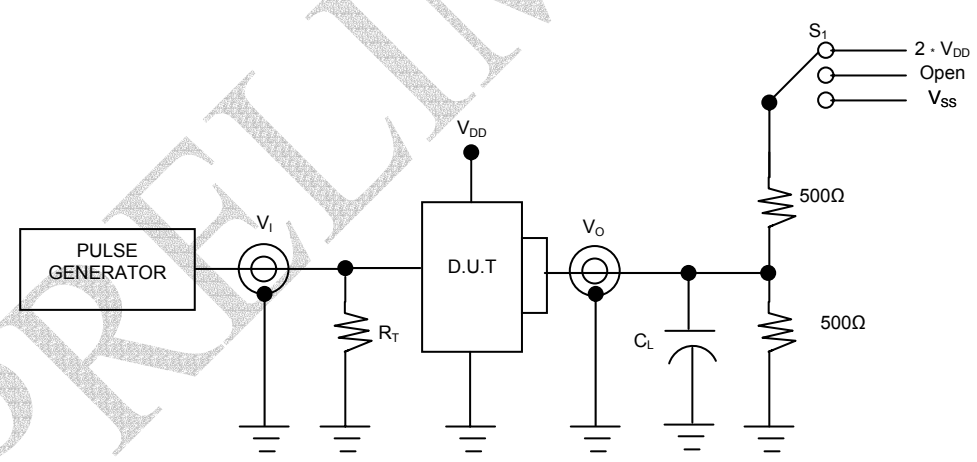
Note: 1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
f_{max}	Maximum Operating Frequency				133	MHz
t_D	Duty Cycle[2,3] = $t_2 \div t_1$	Measured at 1.5V	45.0	50.0	55.0	%
t_3	Rising Edge Rate[3]	Measured between 0.4V and 2.4V	1	2	4	V/nS
t_4	Falling Edge Rate[3]	Measured between 2.4V and 0.4V	1	2	4	V/nS
t_5	Output to Output Skew[3]	All outputs equally loaded		150	225	pS
t_6	SDRAM Buffer LH Prop. Delay[3]	Input edge greater than 1 V/nS	1	2.7	3.5	nS
t_7	SDRAM Buffer HL Prop. Delay[3]	Input edge greater than 1 V/nS	1	2.7	3.5	nS
t_{PLZ}, t_{PHZ}	SDRAM Buffer Enable Delay[3]	Input edge greater than 1 V/nS	1	3	5	nS
t_{PZL}, t_{PZH}	SDRAM Buffer Disable Delay[3]	Input edge greater than 1 V/nS	1	3	5	nS
t_r	Rise Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	C_L = 10pF	6			nS
		C_L = 400pF			250	
t_f	Fall Time for SDATA (Refer Test Circuit for IIC) Refer figure no.3	C_L = 10pF	20			nS
		C_L = 400pF			250	

Note: 1 .All parameters specified with loaded outputs.
2. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1V/nS
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Test Circuit for SDRAM Enable and Disable Times



TEST	S_1
t_6/t_7 t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2· V_{DD} V_{SS}

Figure 1. Load circuit for Switching times

SDRAM Enable and Disable Times

V_M = 1.5V
V_X = V_{OL} +0.3V
V_Y = V_{OH} -0.3V
V_{OH} and $V_{OL\ are}$ the typical Output Voltage drop that occur with the output load

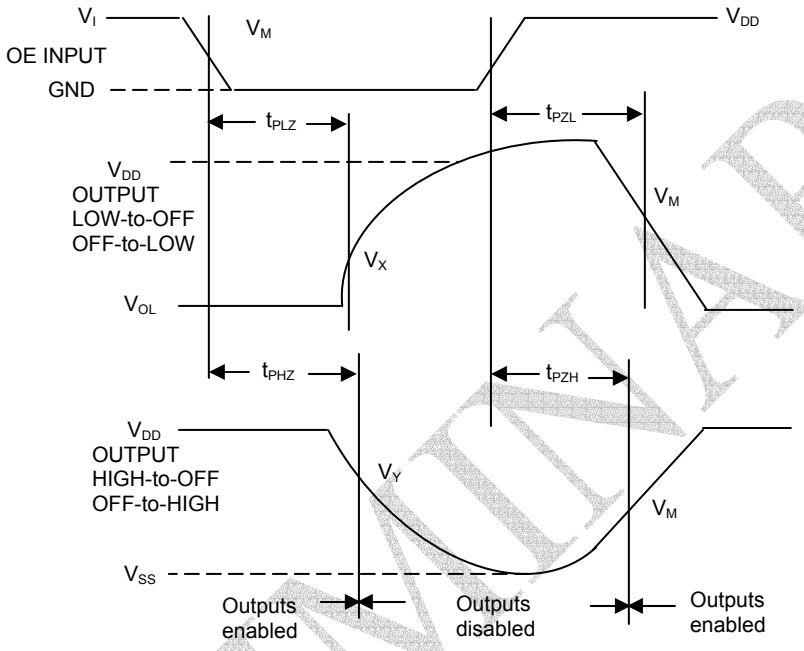


Figure 2. 3-State Enable and Disable times

Test Circuit for IIC Rise and Fall Times

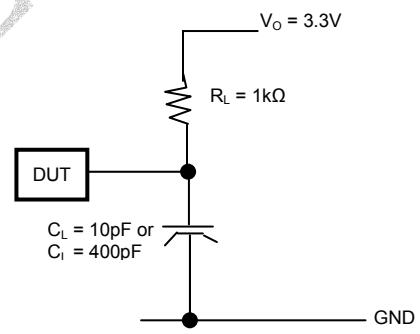
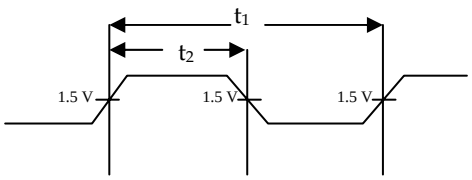


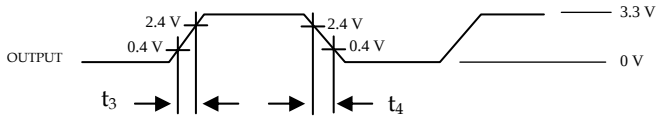
Figure 3. Test Circuit for IIC

Switching Waveforms

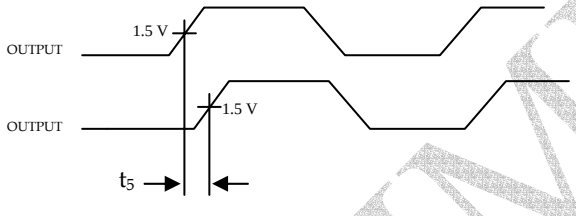
Duty Cycle Timing



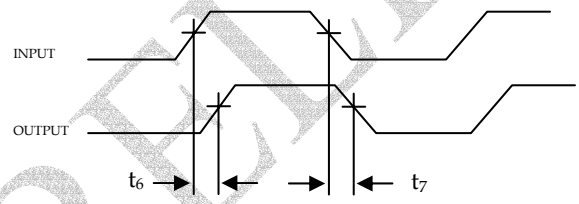
All Outputs Rise/Fall Time



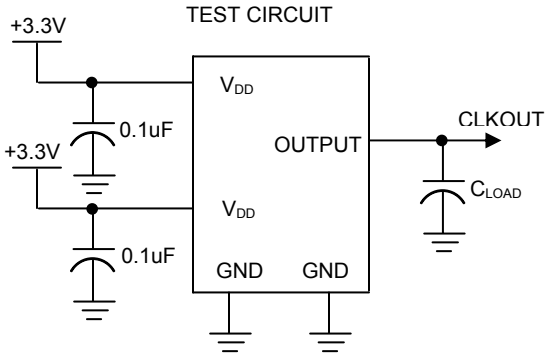
Output - Output Skew



SDRAM Buffer LH and HL Propagation Delay



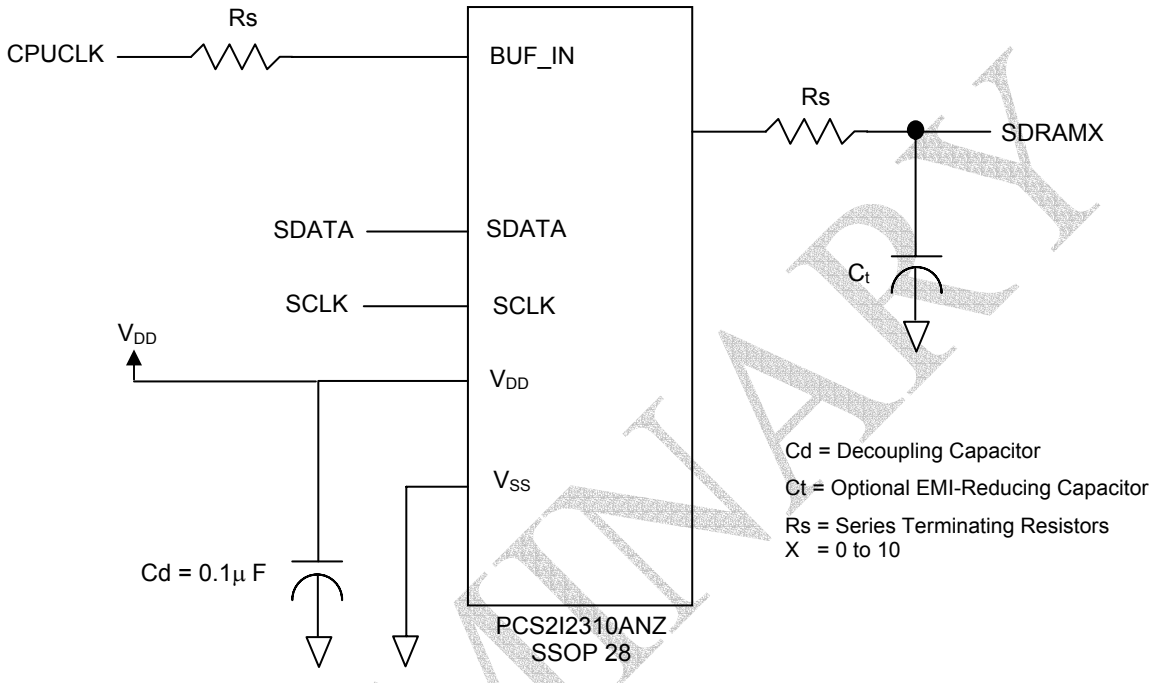
Test Circuits



rev 0.5

Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.



Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25Ω), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7pF to 22pF.
- A Ferrite Bead may be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a 10µF–22µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

IIC Serial Interface Information

The information in this section assumes familiarity with IIC programming.

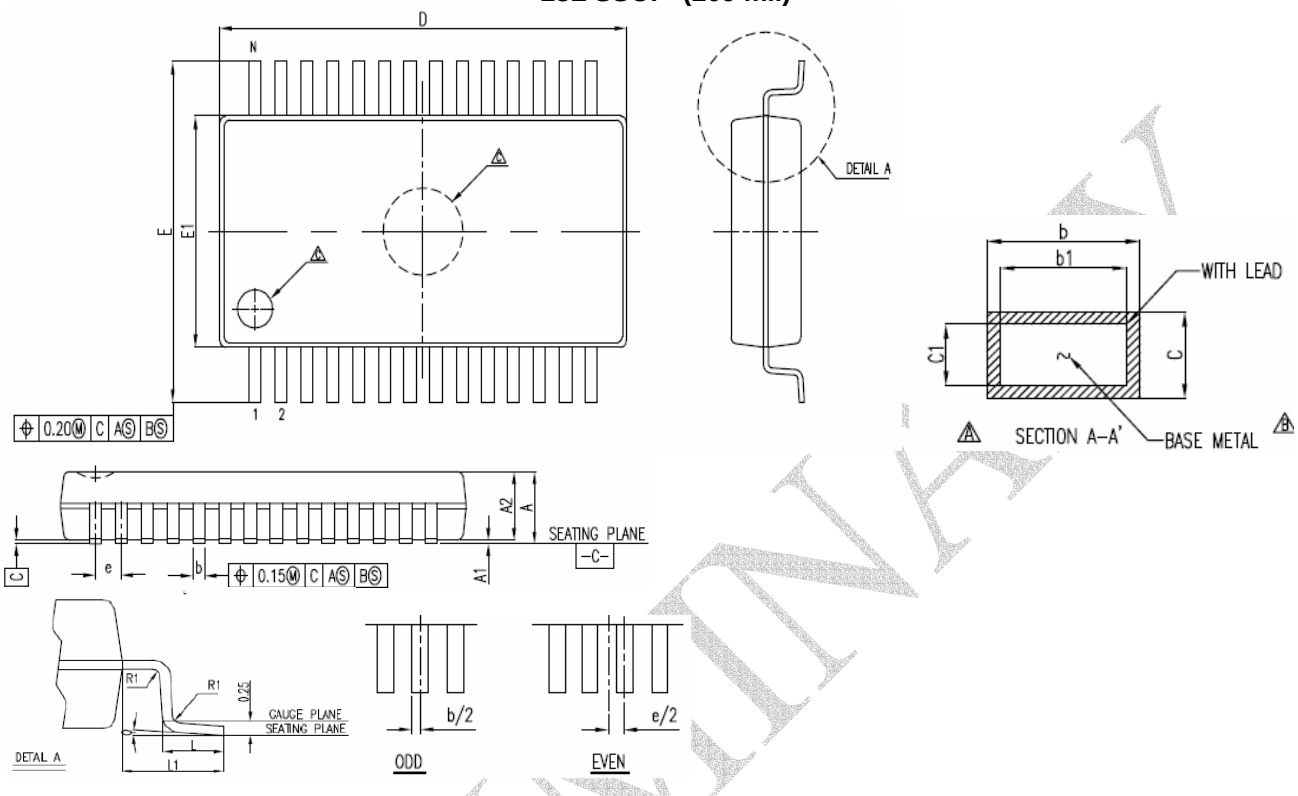
How to program PCS2I2310ANZ through IIC:

- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- PCS2I2310ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- PCS2I2310ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count
- PCS2I2310ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0
- PCS2I2310ANZ device will acknowledge Byte 0
- Master (host) sends the Byte 1
- PCS2I2310ANZ device will acknowledge Byte 1
- Master (host) sends the Byte 2
- PCS2I2310ANZ device will acknowledge Byte 2
- Master (host) sends a Stop bit.

Controller (Host)	PCS2I2310ANZ (slave/receiver)
Start Bit	
Slave Address D3(H)	
	ACK
Command Byte	
	ACK
Byte count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Stop Bit	

Package Information

28L SSOP (209 mil)

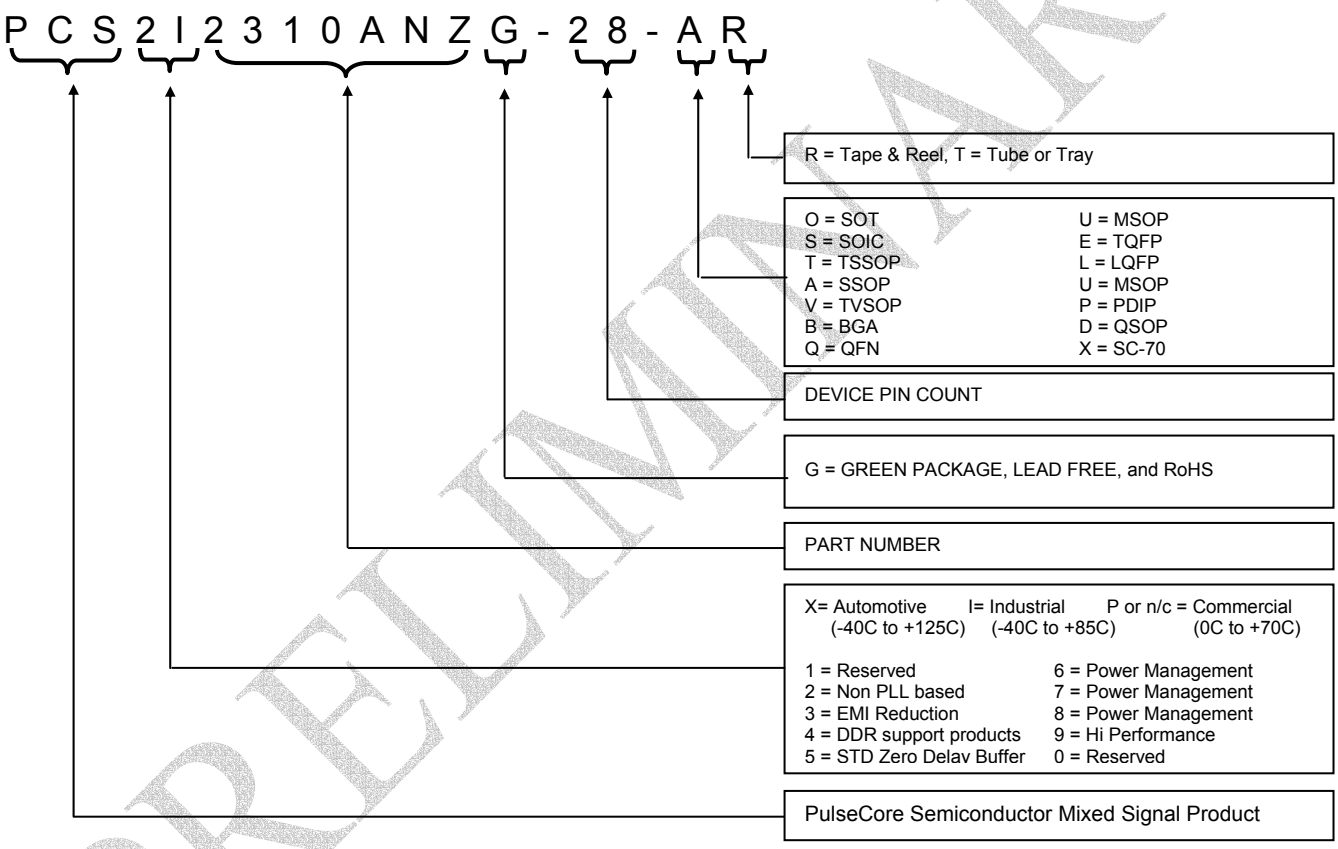


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.079	…	2.0
A1	0.002	…	0.05	…
A2	0.065	0.073	1.65	1.85
D	0.394	0.409	10.00	10.40
L	0.021	0.037	0.55	0.95
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
R1	0.004	….	0.09	…..
b	0.009	0.015	0.22	0.38
b1	0.009	0.013	0.22	0.33
c	0.004	0.010	0.09	0.25
c1	0.004	0.008	0.09	0.21
L1	0.050REF		1.25 REF	
e	0.026 BSC		0.65 BSC	
θ	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS2P2310ANZG-28-AT	2P2310ANZG	28-pin SSOP –Tube, Green	Commercial
PCS2P2310ANZG-28-AR	2P2310ANZG	28-pin SSOP –Tape and Reel, Green	Commercial
PCS2I2310ANZG-28-AT	2I2310ANZG	28-pin SSOP –Tube, Green	Industrial
PCS2I2310ANZG-28-AR	2I2310ANZG	28-pin SSOP –Tape and Reel, Green	Industrial

Device Ordering Information



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Preliminary Information
Part Number: PCS2I2310ANZ
Document Version: 0.5

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003