SECTION 6—MILITARY DEVICES

*QPL version of ULS-2003H-883.

6

SELECTION GUIDE TO HIGH-VOLTAGE/HIGH-CURRENT POWER DRIVERS TO MIL-STD-883

In order of (1) output current rating, (2) output voltage rating, and (3) number of drivers

Outputs*			Features					
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Sat. Out.	Internal Protect.	Part Number
SINK DRIVERS								
100	20	8	—	—	—	X	—	UDS-2595H/R †††
250	40	4	—	—	X	X	—	Series UHD-400
250	70	4	—	—	X	X	—	Series UHD-400-1
250	100	4	—	—	X	X	—	Series UHD-500
300	80	2	—	—	—	X	—	Series UDS-3610H†
300	80	2	—	—	—	X	—	Series UDS-5710H†
300	80	4	—	—	X	X	—	Series UDS-5700H
300	120	4	—		PIN Diode Driver		—	UDS-5791H
350	50	4	—	X	X	—	—	UCS-4801H
350	50	4	—	X	X	—	—	UCS-5800H
350	50	7	—	—	X	—	—	Series ULS-2000H/R
350	50	8	—	—	X	—	—	Series ULS-2800H/R
350	50	8	—	X	X	—	—	UCS-4801H
350	50	8	—	X	X	—	—	UCS-5801H
350	50	8	X	X	—	—	—	UCS-4821H
350	80	8	X	X	—	—	—	UCS-4822H
350	80	8	X	X	—	—	—	UCS-5822H
350	95	7	—	—	X	—	—	Series ULS-2020H/R
350	95	8	—	—	X	—	—	Series ULS-2820H/R
350	100	8	X	X	—	—	—	UCS-4823H
500	50	7	—	—	X	—	—	Series ULS-2010H/R
500	50	8	—	—	X	—	—	Series ULS-2810H/R
1250	50	4	—	—	X	—	—	Series ULS-2064H
1500	80	4	—	—	X	—	—	Series ULS-2065H
SOURCE DRIVERS								
−25	60	8	—	X	—	—	—	UCS-4815H
−25	60	8	—	X	—	—	—	UCS-5815H
−25	60	10	X	X	—	—	—	UCS-4810H
−25	60	10	X	X	—	—	—	UCS-5810H
−350	−50	8	—	—	X	—	—	UDS-2580/88H†††
−350	50	8	—	—	X	—	—	UDS-2981/82H/R
−350	80	8	—	—	X	—	—	UDS-2983/84H/R
SOURCE/SINK DRIVERS								
±800	30	3	HALF-BRIDGE		X	X	—	UDS-2933/34H

*Current is maximum testing condition. Voltage is absolute maximum rating.
†NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.
††New product. Information on commercial version is given elsewhere in this data book as UDN

SELECTION GUIDE TO SMART POWER DRIVERS TO MIL-STD-883

Logic	Output Ratings*		Diode Clamps	Part Number
PARALLEL-INPUT LATCHED DRIVERS				
4-Bit	350 mA	50 V	X	UCS-4401H
4-Bit	350 mA	50 V	X	UCS-5800H
8-Bit	−25 mA	60 V	—	UCS-4815H
8-Bit	−25 mA	60 V	—	UCS-5815H
8-Bit	350 mA	50 V	X	UCS-4801H
8-Bit	350 mA	50 V	X	UCS-5801H
SERIAL-INPUT LATCHED DRIVERS				
8-Bit	350 mA	50 V	—	UCS-4821H
8-Bit	350 mA	80 V	—	UCS-4822H
8-Bit	350 mA	80 V	—	UCS-5822H
8-Bit	350 mA	100 V	—	UCS-4823H
10-Bit	−25 mA	60 V	—	UCS-4810H
10-Bit	−25 mA	60 V	—	UCS-5810H

*Current is maximum tested condition; voltage is absolute maximum rating.

SELECTION GUIDE TO 4000B SERIES CMOS LOGIC

Function	Description	Part Number			Package Style	Features
		MIL-STD-883	MIL-M-38510†	DESC Drawing		
Gates and Inverters	NAND	883C4011BC	/05001B	/05051B	14-Pin DIP	Quad 2-Input
		883C4011UBC	—	—	14-Pin DIP	Quad 2-Input (Unbuffered)
		883C4012BC	/05002B	/05052B	14-Pin DIP	Dual 4-Input
		883C4023BC	/05003B	/05053B	14-Pin DIP	Triple 3-Input
		883C4068BC	—	—	14-Pin DIP	8-Input
	AND	883C4073BC	/17003B	—	14-Pin DIP	Triple 3-Input
		883C4081BC	/17001B	—	14-Pin DIP	Quad 2-Input
		883C4082BC	/17002B	—	14-Pin DIP	Dual 4-Input
	NOR	883C4001BC	/05252B	—	14-Pin DIP	Quad 2-Input
		883C4001UBC	/05202B	—	14-Pin DIP	Quad 2-Input (Unbuffered)
		883C4002BC	/05203B	—	14-Pin DIP	Dual 4-Input
		883C4025BC	/05204B	—	14-Pin DIP	Triple 3-Input
		883C4078BC	—	—	14-Pin DIP	8-Input
	OR	883C4071BC	/17101B	—	14-Pin DIP	Quad 2-Input
		883C4072BC	/17102B	—	14-Pin DIP	Dual 4-Input
		883C4075BC	/17103B	—	14-Pin DIP	Triple 3-Input
	Complex	883C4000BC	/05201B	—	14-Pin DIP	Dual 3-Input NOR and Inverter
		883C4007UBC	/05301B	—	14-Pin DIP	Dual Complimentary Pair and Inverter
		883C4030BC	/05303B	/05353B	14-Pin DIP	Quad 2-Input Exclusive OR
		883C4070BC	/17203B	—	14-Pin DIP	Quad 2-Input Exclusive OR
		883C4077BC	/17204B	—	14-Pin DIP	Quad Input Exclusive NOR
		883C4085BC	/17201B	—	14-Pin DIP	Dual 2-Wide AND-OR Invert
		883C4086BC	/16202B	—	14-Pin DIP	4-Wide AND-OR Invert
		883C4019BC	/05302B	/05352B	16-Pin DIP	Quad AND-OR Select Gate
	Inverters	883C4069UBC	—	—	14-Pin DIP	Hex, Pin-Compatible with 74C04
		883C4449UBC	—	—	16-Pin DIP	Hex, Pin-Compatible with 4009, 4049
	Expandable Gates	883C4402BC	—	—	16-Pin DIP	Dual 4-Input NOR
		883C4412BC	—	—	16-Pin DIP	Dual 4-Input NAND
Schmitt Triggers	Quad	883C4093BC	/17701B	—	14-Pin DIP	2-Input NAND
	Hex	883C4584BC	—	—	14-Pin DIP	Inverter
Buffers	Level Shifting	883C4009UBC	/05501B	—	16-Pin DIP	Hex Inverter, Dual Supply
		883C4010BC	/05502B	—	16-Pin DIP	Hex Non-Inverting, Dual Supply
		883C4049UBC	/05503B	—	16-Pin DIP	Hex Inverter, Single Supply
		883C4050BC	/05504B	—	16-Pin DIP	Hex Non-Inverting, Single Supply
		883C4504BC	—	—	16-Pin DIP	Hex Non-Inverting, Dual Supply
	High Current	883C4041UBC	—	—	14-Pin DIP	Quad True/Complement
		883C4441UBC	—	—	14-Pin DIP	Quad Driver
	3-State	883C4502BC	—	—	16-Pin DIP	Hex Strobed Inverting
Encoder	8-Bit Priority	883C4532BC	/17302B	—	16-Pin DIP	5 V, 10 V and 15 V Parallel Rating
Decoders	Logic Functions	883C4028BC	/05901B	/05951B	16-Pin DIP	BCD-to-Decimal
		883C4428BC	—	—	14-Pin DIP	Binary-to-Octal
		883C4514BC	—	—	24-Pin DIP	4-to-16 Line Decoder/Latch (Active High Output)
		883C4515BC	—	—	24-Pin DIP	4-to-16 Line Decoder/Latch (Active Low Output)
		883C4555BC	—	—	16-Pin DIP	Dual 2-to-4 Line (Active High Output)
		883C4556BC	—	—	16-Pin DIP	Dual 2-to-4 Line (Active Low Output)
	Display Functions	883C4026ABC	—	—	16-Pin DIP	Decade Counter, 7 Segment Output
		883C4426ABC	—	—	16-Pin DIP	4026 with Bipolar Drivers
		883C4033ABC	—	—	16-Pin DIP	Decade Counter, 7 Segment Output
		883C4433ABC	—	—	16-Pin DIP	4033 with Bipolar Drivers
		883C4511BC	—	—	16-Pin DIP	BCD to 7-Seg. Latch/Decoder, Bipolar Outputs
		883C4543BC	—	—	16-Pin DIP	BCD to 7-Seg. Latch/Decoder, LCD Outputs

†Complete Catalog Number is M38510/—Example: M38510/05001B.
Detailed technical information for 4000B Series CMOS logic is available on request.

Continued

SELECTION GUIDE TO 4000B SERIES CMOS LOGIC

Function	Description	Part Number			Package Style	Features
		MIL-STD-883	MIL-M-38510†	DESC Drawing		
Counters	Binary	883C4024BC	/05605B	—	14-Pin DIP	7-Stage
		883C4404BC	—	—	14-Pin DIP	8-Stage
		883C4040BC	—	77058	16-Pin DIP	12-Stage
		883C4020BC	/05603B	/05653B	16-Pin DIP	14-Stage
		883C4060BC	—	—	16-Pin DIP	14-Stage with Oscillator
		883C4161BC	—	—	16-Pin DIP	4-Stage with Asynchronous Clear
		883C4163BC	—	—	16-Pin DIP	4-Stage with Synchronous Clear
		883C4193BC	—	—	16-Pin DIP	4-Bit Up/Down
		883C4516BC	—	—	16-Pin DIP	4-Stage Programmable Up/Down
		883C4526BC	—	—	16-Pin DIP	4-Stage Programmable Down
	Binary/Decade	883C4029BC	—	81016	16-Pin DIP	Presettable Up/Down
	Decade	883C4520BC	—	77025	16-Pin DIP	Dual 4-Stage Up
		883C4192BC	—	—	16-Pin DIP	Presettable Up/Down
		883C4510BC	—	—	16-Pin DIP	Programmable Up/Down
		883C4160BC	—	—	16-Pin DIP	Counter with Asynchronous Clear
		883C4162BC	—	—	16-Pin DIP	Counter with Synchronous Clear
		883C4522BC	—	—	16-Pin DIP	4-Stage Programmable Down
		883C4518BC	—	—	16-Pin DIP	Dual Up
	Decoded Outputs	883C4017BC	/05601B	/05651B	16-Pin DIP	Decade Counter with 10 Outputs
		883C4022BC	/05604B	—	16-Pin DIP	Octal Counter with 8 Outputs
	Johnson	883C4018BC	/05602B	/05652B	16-Pin DIP	Presettable Divide-by-n
Dividers/Multipliers	÷ 21	883C4445BC	—	—	16-Pin DIP	On-Board Oscillator
	Rate Multiplier	883C4527BC	—	—	16-Pin DIP	BCD
	Phase-Locked Loops	883C4046BC	—	—	16-Pin DIP	Maximum Operating Freq. 3 MHz at 10 V
		883C4446BC	—	—	16-Pin DIP	Maximum Operating Freq. 4 MHz at 10 V
	Multivibrators	883C4528BC	—	77045	16-Pin DIP	Dual Monostable
		883C4047BC	—	81020	16-Pin DIP	Monostable/Astable
Arithmetic Logic	4-Bit	883C4582BC	—	—	16-Pin DIP	Look-Ahead Carry Block
		883C4585BC	—	77037	16-Pin DIP	Magnitude Comparator
		883C4008BC	/05401B	—	16-Pin DIP	Full Adder
		883C4581BC	—	—	24-Pin DIP	Arithmetic Logic Unit
	12-Bit	883C4531BC	—	—	16-Pin DIP	Parity Tree
Flip-Flops	Dual D Type	883C4013BC	/05101B	/05151B	79011	14-Pin DIP	16 MHz Toggle Rate
	Dual JK Type	883C4027BC	/05102B	—	—	16-Pin DIP	8 MHz Toggle Rate
	Quad D Type	883C4076BC	—	—	—	16-Pin DIP	3-State Outputs
	Hex D Type	883C4174BC	—	—	—	16-Pin DIP	Functional Equivalent to TTL
Latches	R-S Type	883C4043BC	/05103B	—	—	16-Pin DIP	Quad NOR with 3-State Outputs
		883C4044BC	—	—	—	16-Pin DIP	Quad NAND with 3-State Outputs
	Clocked	883C4042BC	—	—	81019	16-Pin DIP	Quad, Common Clock
		883C4508BC	—	—	—	24-Pin DIP	Dual 4-Bit With Three-State Outputs
	Addressable	883C4099BC	—	—	—	16-Pin DIP	8-Bit
Shift Registers	Serial In/Serial Out	883C4006BC	/05701B	/05751B	—	14-Pin DIP	18-Stage
	Serial In/Parallel Out	883C4015BC	/05703B	—	—	16-Pin DIP	Dual 4-Stage
	Parallel In/Serial Out	883C4014BC	—	—	—	16-Pin DIP	8-Stage, Synchronous Parallel Loading
		883C4021BC	/05704B	/05754B	79012	16-Pin DIP	8-Stage, Asynchronous Parallel Loading
	Parallel In/Parallel Out	883C4035BC	—	—	81017	16-Pin DIP	4-Stage
	Bus Registers	883C4034BC	—	—	—	24-Pin DIP	8-Stage Universal
		883C4094BC	—	—	77025	16-Pin DIP	8-Stage Shift and Store
		883C4517BC	—	—	—	16-Pin DIP	Dual 64-Bit Static
Multiplexers and Switches	Digital Mux.	883C4512BC	—	—	—	16-Pin DIP	8-Channel Data Selector
	Analog Multiplexers and Demultiplexers	883C4051BC	—	—	—	16-Pin DIP	8-Channel Analog Multiplexer
		883C4052BC	—	—	79015	16-Pin DIP	Differential 4-Channel Analog Mux./Demux.
		883C4053BC	—	—	81018	16-Pin DIP	Triple 2-Channel Analog Mux./Demux.
	Analog Switches	883C4016BC	/05801B	—	—	14-Pin DIP	Quad SPST Switch
		883C4066BC	/05802B	/05852B	—	14-Pin DIP	Quad SPST with Buffered Control Unit
		883C4416BC	—	—	—	14-Pin DIP	4016 Configured for DPDT

†Complete Catalog Number is M38510/—Example: M38510/05001B.
Detailed technical information for 4000B Series CMOS logic is available on request.

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CUSTOM DEVICES FOR MILITARY APPLICATIONS

Sprague Electric Company's Semiconductor Group has broad experience in designing and manufacturing custom integrated circuits for a wide variety of military applications. Technologies ranging from high-speed, low-power CMOS to high-voltage, high-current bipolar and BiMOS provide low-cost, space-saving, custom silicon solutions for tough military system problems. Sprague Electric offers the custom design and manufacturing resources necessary to produce high-volume, military-grade, proprietary circuits in a secure environment with a timely schedule.

In addition to custom design services, Sprague Electric also provides for customer-owned tooling (COT), an economical manufacturing capability for customers who have already designed proprietary LSI circuits compatible with Sprague processes. Two wafer fabrication facilities are available with full JAN line qualifications to MIL-M-38510.

CUSTOM MANUFACTURING SERVICES

Custom devices are available with a variety of manufacturing services. Devices may be purchased as:

DICE IN WAFER FORM
- Without Device Electrical Testing
- With 100% Electrical Testing
- Expanded Wafers

DICE IN WAFFLE PACKS
- Tested, Sorted, Inspected

PACKAGED UNITS WITH FULL ELECTRICAL TESTING
- Hermetic Dual In-Line Packages
- Plastic Dual In-Line Packages
- Leadless and Leaded Hermetic Chip Carriers
- Specialty Packages (Plastic Flatpacks, Small Outline)

These choices give the customer the flexibility to select only the services needed, minimizing custom silicon solution costs. Full military screening per MIL-STD-883, with compliant fabrication, assembly, testing, and qualification, is standard.

SERIES UHD-400, UHD-400-1, AND UHD-500 POWER AND RELAY DRIVERS

MIL-STD-883 Compliant

FEATURES

- 500 mA Output Current-Sink Capability
- Four Logic Types
- Pinning Compatible with 54/74 Logic Series
- High-Voltage Output:
  100 V Series UHD-500
  70 V Series UHD-400-1
  40 V Series UHD-400

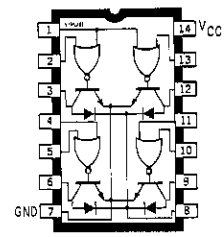
COMBINING LOGIC GATES and high-current switching transistors, these hermetically packaged, monolithic devices are used to drive incandescent or LED lamps, relays, solenoids, small dc motors, and other peripheral power loads in military and aerospace applications. Drivers with internal transient-suppression diodes are recommended for use with inductive loads.

Three minimum output-breakdown voltage ratings are available: 40 V (Series UHD-400), 70 V (Series UHD-400-1), and 100 V (Series UHD-500). All devices can sink 250 mA continuous, or 500 mA peak.

The inputs are compatible with standard TTL and CMOS logic levels. Four of eight available logic/output configurations are shown at right.

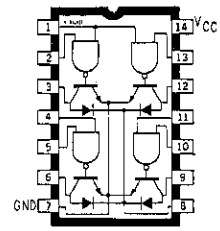
These devices are supplied in ceramic/metal side-brazed 14-pin hermetic packages. The package conforms to the dimensional requirements of MIL-M-38510 and is rated for operation over the full military temperature range of −55°C to +125°C. Power and relay drivers in flat-pack packages, Series UHC-400, UHC-400-1, and UHC-500, continue to be available on special order.

Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, is standard for all devices.



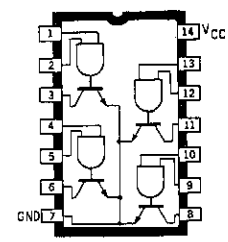
Dwg. No. A-9130B

UHD-403
UHD-403-1
UHD-503



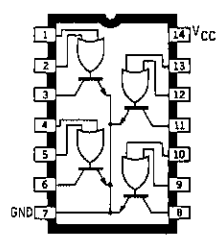
Dwg. No. A-7880B

UHD-406
UHD-406-1
UHD-506



Dwg. No. A-12,388

UHD-408
UHD-408-1
UHD-508



Dwg. No. A-12,389

UHD-432
UHD-432-1
UHD-532

Device Part Number Designation

Part Numbers*			Function
400	400-1	500	Quad 2-Input AND
402	402-1	502	Quad 2-Input OR
403	403-1	503	Quad OR for Inductive Loads
406	406-1	506	Quad AND for Inductive Loads
407	407-1	507	Quad NAND for Inductive Loads
408	408-1	508	Quad 2-Input NAND
432	432-1	532	Quad 2-Input NOR
433	433-1	533	Quad NOR for Inductive Loads

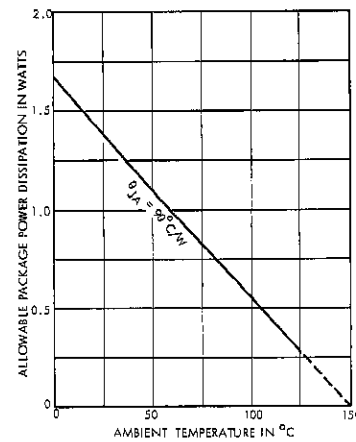
*Complete part number includes the prefix UHD.

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7 V
Output Voltage, V_{IN} . . . . . 5.5 V
Output Off-State Voltage, V_{OFF}
  Series UHD-400 . . . . . 40 V
  Series UHD-400-1 . . . . . 70 V
  Series UHD-500 . . . . . 100 V
Output On-State Sink Current, I_{ON}
  (one driver) . . . . . 500 mA
  (total package) . . . . . 1 A
Suppression Diode Off-State Voltage, V_R
  Series UHD-400 . . . . . 40 V
  Series UHD-400-1 . . . . . 70 V
  Series UHD-500 . . . . . 100 V
Suppression Diode On-State Current, I_F . . . . . 500 mA
Operating Free-Air Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,884B

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into Any Output (ON State)	—	—	250	mA

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

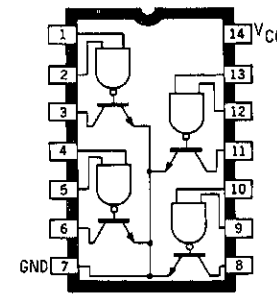
Characteristic	Series	Test Conditions (Note 3)	Limits			
			Min.	Typ.	Max.	Units
Turn-On Delay Time (t_{pdO})	UHD-400	V_S = 40 V, R_L = 265Ω (6 W)	—	200	500	ns
	UHD-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	200	500	ns
	UHD-500	V_S = 100 V, R_L = 670Ω (15 W)	—	200	500	ns
Turn-Off Delay Time (t_{pdf})	UHD-400	V_S = 40 V, R_L = 265Ω (6 W)	—	300	750	ns
	UHD-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	300	750	ns
	UHD-500	V_S = 100 V, R_L = 670Ω (15 W)	—	300	750	ns

NOTES:
1. Each input tested separately.
2. Voltage values shown in the test-circuit waveforms are with respect to network ground terminal.
3. C_L = 15 pF. Capacitance value specified includes probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0 V	$t_f \leq$ 7.0 ns	t_p = 1.0 µs
$V_{in(1)}$ = 3.5 V	$t_r \leq$ 14 ns	PRR = 500 kHz

UHD-400, UHD-400-1, UHD-500
Quad 2-Input AND Power Drivers

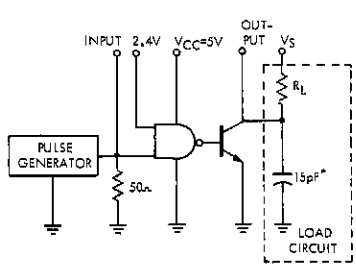


Dwg. No. A-7606

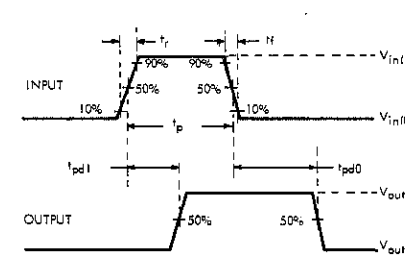
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-400	4.5 V	2.0 V	2.0 V	40 V	—	—	100	µA
			UHD-400-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	µA
			UHD-500	4.5 V	2.0 V	2.0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.



Dwg. No. A-7876E

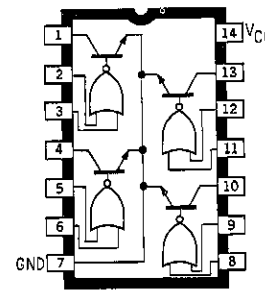


Dwg. No. A-7628C

*Includes probe and test fixture capacitance.

6

UHD-402, UHD-402-1, UHD-502
Quad 2-Input OR Power Drivers

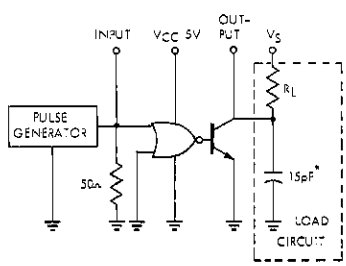


Dwg. No. A-7608

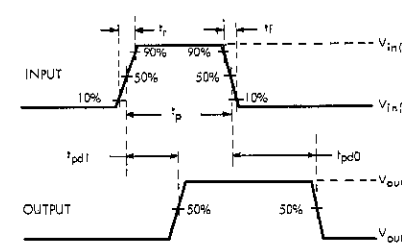
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-402	4.5 V	2.0 V	0 V	40 V	—	—	100	µA
			UHD-402-1	4.5 V	2.0 V	0 V	70 V	—	—	100	µA
			UHD-502	4.5 V	2.0 V	0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.1	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	18	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.



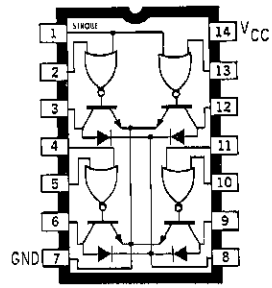
Dwg. No. A-7877C



Dwg. No. A-7828C

*Includes probe and test fixture capacitance.

UHD-403, UHD-403-1, UHD-503
Quad OR Relay Drivers

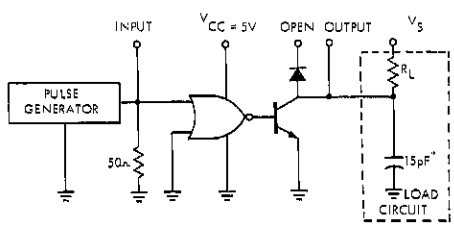


Dwg. No. A-9130B

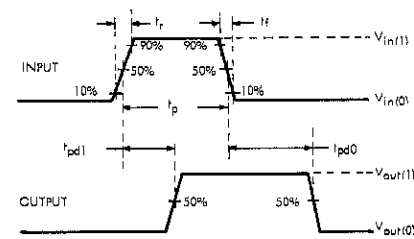
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			Units
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	
Output Reverse Current	I_{OEX}	—	UHD-403	4.5 V	2.0 V	0 V	40 V	—	—	100	µA
			UHD-403-1	4.5 V	2.0 V	0 V	70 V	—	—	100	µA
			UHD-503	4.5 V	2.0 V	0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25$°C.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



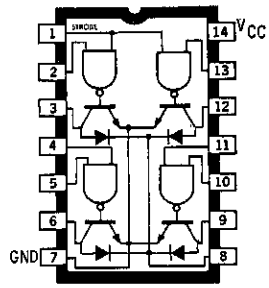
Dwg. No. A-9123C



Dwg. No. A-7828C

*Includes probe and test fixture capacitance.

UHD-406, UHD-406-1, UHD-506
Quad AND Relay Drivers

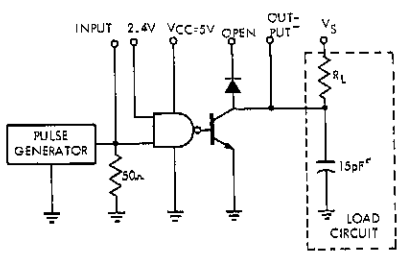


Dwg. No. A-7860B

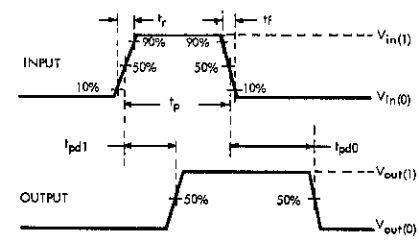
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-406	4.5 V	2.0 V	2.0 V	40 V	—	—	100	µA
			UHD-406-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	µA
			UHD-506	4.5 V	2.0 V	2.0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V*	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



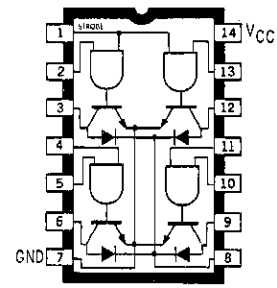
Dwg. No. A-7878C



Dwg. No. A-7628C

*Includes probe and test fixture capacitance.

UHD-407, UHD-407-1, UHD-507
Quad NAND Relay Drivers

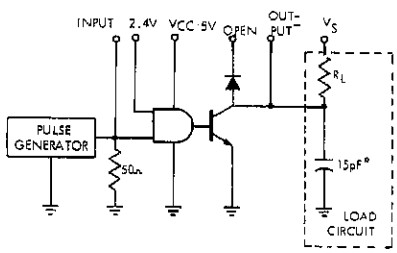


Dwg. No. A-7873B

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

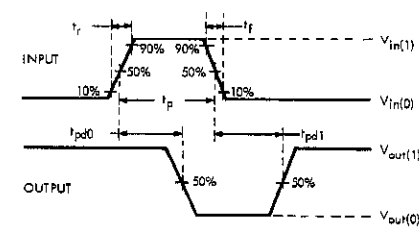
Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-407	4.5 V	0.8 V	4.5 V	40 V	—	—	100	µA
			UHD-407-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	µA
			UHD-507	4.5 V	0.8 V	4.5 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	5.0 V	5.0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	0 V	0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



Dwg. No. A-7899C

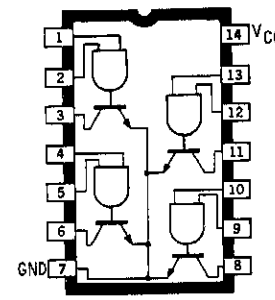
*Includes probe and text fixture capacitance.



Dwg. No. A-7900A

6

UHD-408, UHD-408-1, UHD-508
Quad 2-Input NAND Power Drivers

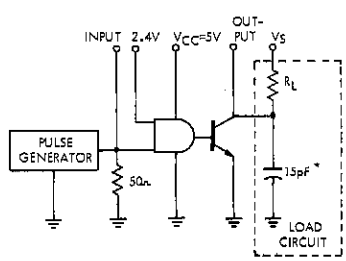


Dwg. No. 12,388

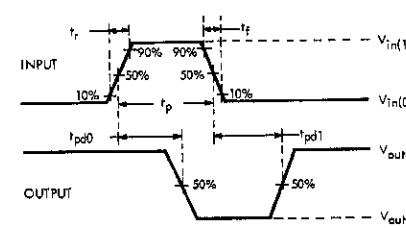
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-408	4.5 V	0.8 V	4.5 V	40 V	—	—	100	µA
			UHD-408-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	µA
			UHD-508	4.5 V	0.8 V	4.5 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Each input is tested separately.



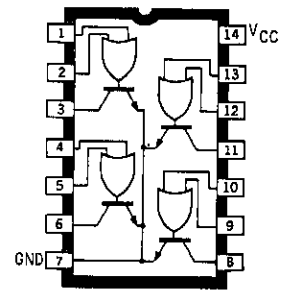
Dwg. No. A-9638A



Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

UHD-432, UHD-432-1, UHD-532
Quad 2-Input NOR Power Drivers

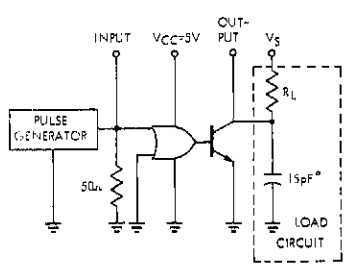


Dwg. No. A-12,389

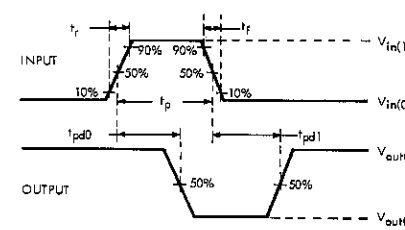
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-432	4.5 V	0.8 V	0.8 V	40 V	—	—	100	μA
			UHD-432-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	μA
			UHD-532	4.5 V	0.8 V	0.8 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Each input is tested separately.



Dwg. No. A-7902C

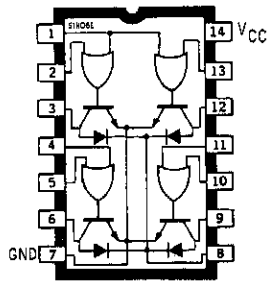


Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

6

UHD-433, UHD-433-1, UHD-533
Quad NOR Relay Drivers

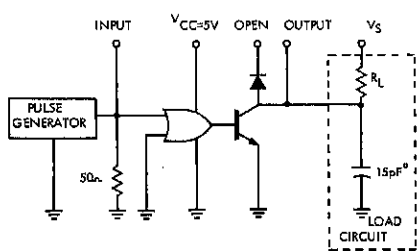


Dwg. No. A-12,390A

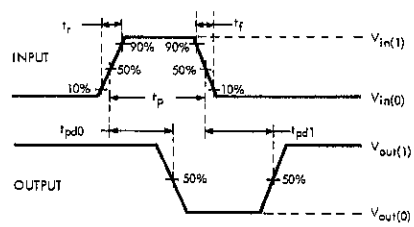
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-433	4.5 V	0.8 V	0.8 V	40 V	—	—	100	µA
			UHD-433-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	µA
			UHD-533	4.5 V	0.8 V	0.8 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	5.0 V	5.0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	0 V	0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values at are V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



Dwg. No. A-9135C



Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

SERIES ULS-2000H AND ULS-2000R
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS
MIL-STD-883 Compliant

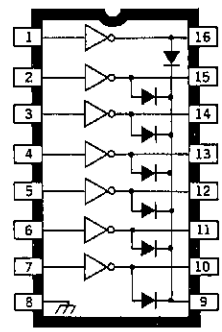
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- Side-Brazed Hermetic Package
- Cer-DIP Hermetic Package
- High-Reliability Screening to MIL-STD-883, Class B
- −55°C to +125°C Temperature Range

COMPRISED OF SEVEN silicon NPN Darlington power drivers on a common monolithic substrate, Series ULS-2000H and ULS-2000R arrays drive relays, solenoids, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A of output current per package.

These devices are screened to MIL-STD-883, Class B and are supplied in either the popular ceramic/metal side-brazed 16-pin hermetic package (suffix 'H') or ceramic/glass cer-DIP hermetic package (suffix 'R'). Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of −55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 30 integrated circuits described in this bulletin permit the circuit designer to select the optimal device for any application. In addition to the two package styles, there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.



Dwg. No. A-9594

Device Part Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Part Number		
General Purpose PMOS, CMOS	ULS-2001*	ULS-2011*	ULS-2021*
14-25 V PMOS	ULS-2002*	ULS-2012*	ULS-2022*
5 V TTL, CMOS	ULS-2003*	ULS-2013*	ULS-2023*
6-15 V CMOS, PMOS	ULS-2004*	ULS-2014*	ULS-2024*
High-Output TTL	ULS-2005*	ULS-2015*	ULS-2025*

*Complete part number includes a final letter to indicate package (H = ceramic/metal size-brazed, R = ceramic/glass cer-DIP).

6

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
- (ULS-200X*, ULS-201X*) . . . . . 50 V
- (ULS-202X*) . . . . . 95 V

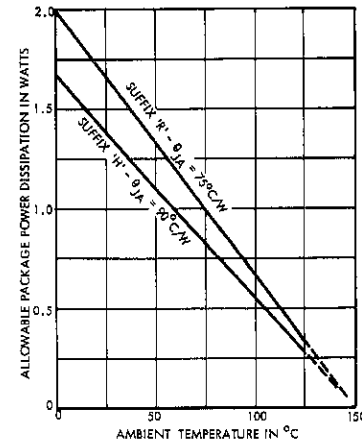
Input Voltage, V_{IN}
- (ULS-20X2, X3, X4*) . . . . . 30 V
- (ULS-20X5*) . . . . . 15 V

Peak Output Current, I_{OUT}
- (ULS-200X*, ULS-202X*) . . . . . 500 mA
- (ULS-201X*) . . . . . 600 mA

Ground Terminal Current, I_{GND} . . . . . 3.0 A
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D
- (one Darlington pair) . . . . . 1.0 W
- (total package) . . . . . See Graph

Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

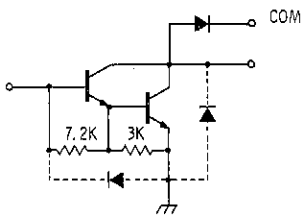
ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,884A

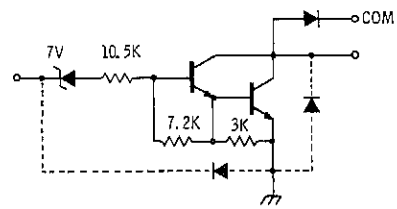
PARTIAL SCHEMATICS

ULS-20X1*
(Each Driver)



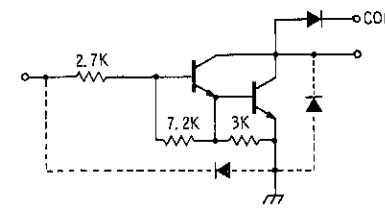
Dwg. No. A-9595

ULS-20X2*
(Each Driver)



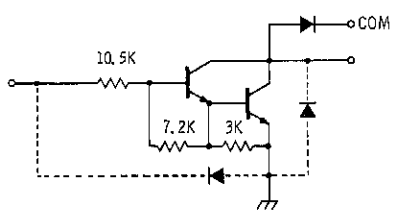
Dwg. No. A-9650

ULS-20X3*
(Each Driver)



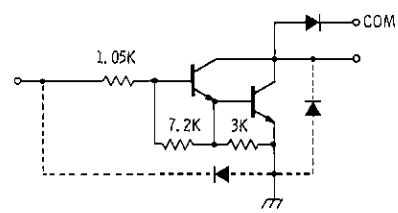
Dwg. No. A-9651

ULS-20X4*
(Each Driver)



Dwg. No. A-9898A

ULS-20X5*
(Each Driver)



Dwg. No. A-10,228

**Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP). X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.*

SERIES ULS-2000H AND ULS-2000R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{I(ON)}$	ULS-2002*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2003*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2004*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2005*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{I(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{I(ON)}$	ULS-2002*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2003*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2004*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2005*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2001*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{I(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2010H AND ULS-2010R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2012*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2013*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2014*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2015*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2012*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
		ULS-2013*	−55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V
		ULS-2014*	−55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS-2015*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2011*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2020H AND ULS-2020R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS-2022*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2024*	25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2022*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2023*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2024*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2025*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2022*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2023*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2024*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2025*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2021*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

TEST FIGURES

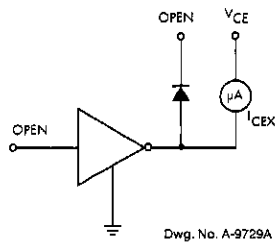


FIGURE 1A

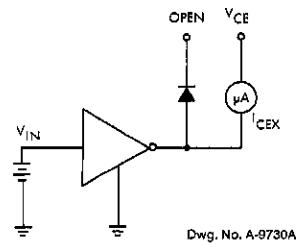


FIGURE 1B

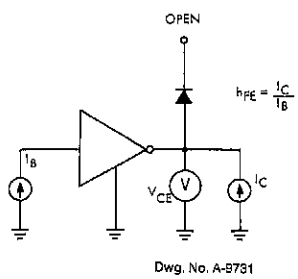


FIGURE 2

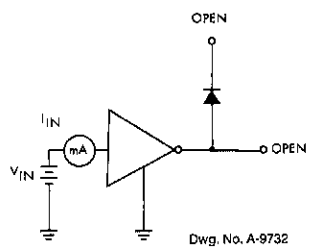


FIGURE 3

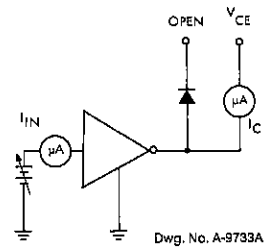


FIGURE 4

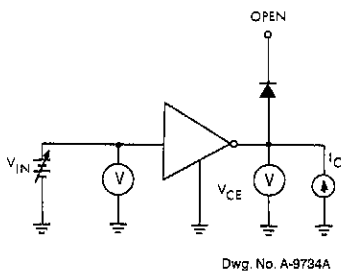


FIGURE 5

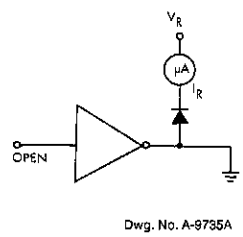


FIGURE 6

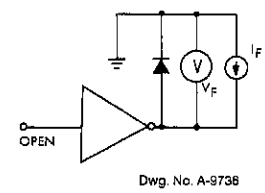
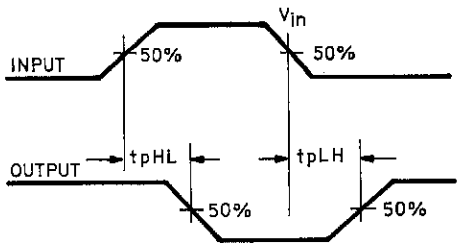
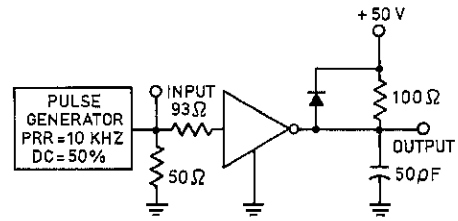


FIGURE 7

	V_{in}
ULS-20X1*	3.5 V
ULS-20X2*	13 V
ULS-20X3*	3.5 V
ULS-20X4*	12 V
ULS-20X5*	3.5 V



Dwg. No. A-13,272

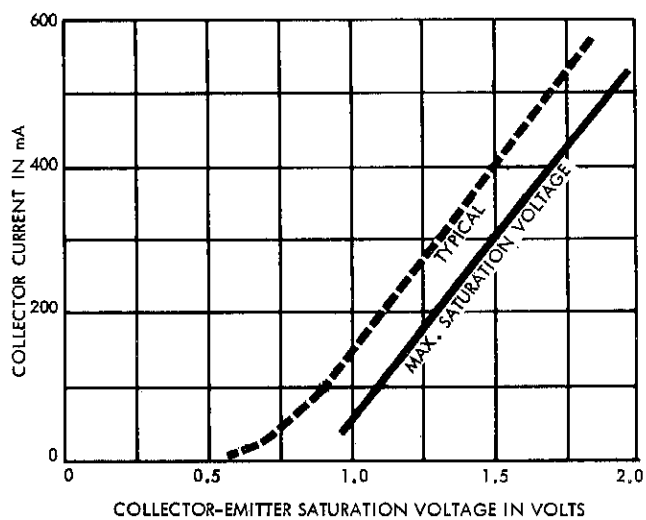


Dwg. No. A-13,273

* Complete part number includes a final letter to indicate package.
X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

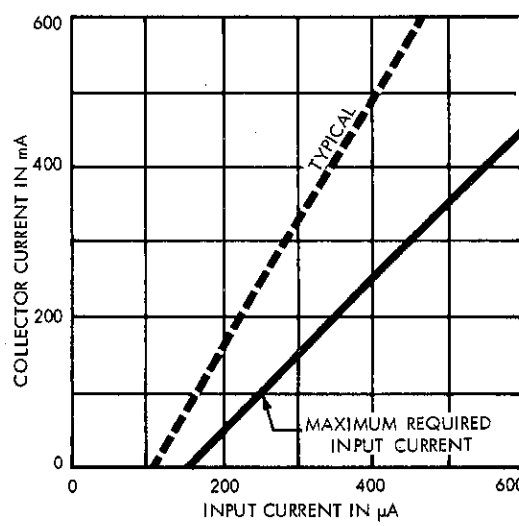
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

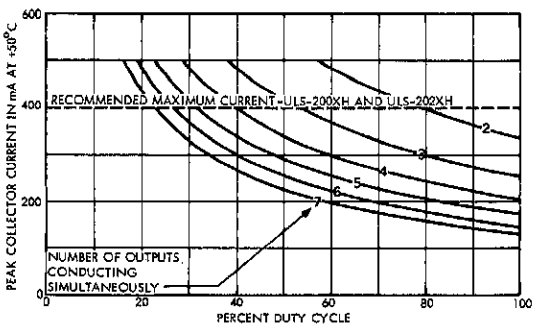


Dwg. No. A-10,872B

6

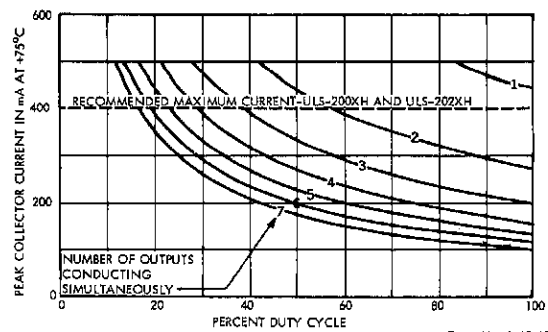
SERIES ULS-2000H

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



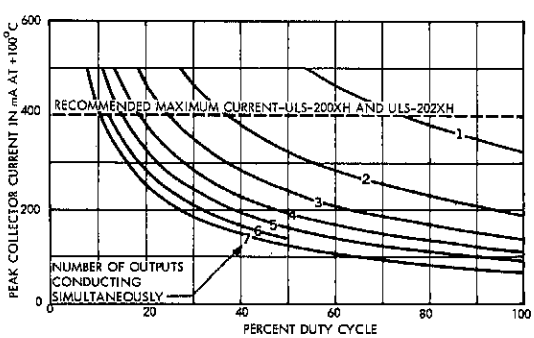
Dwg. No. A-10,197B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



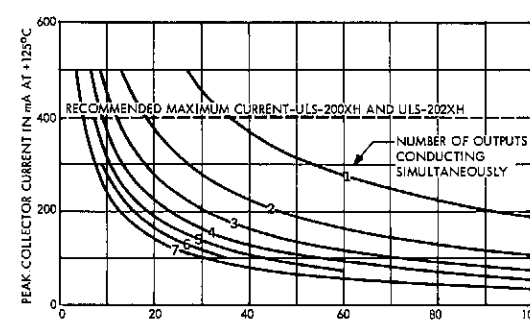
Dwg. No. A-10,199B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,200B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

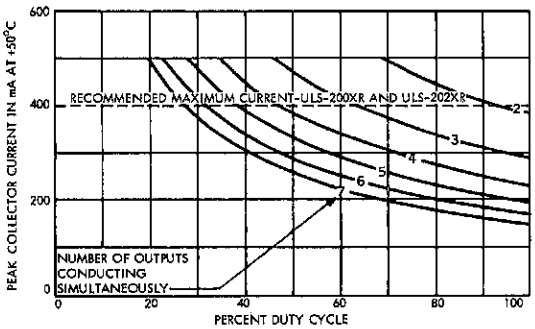


Dwg. No. A-10,201B

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

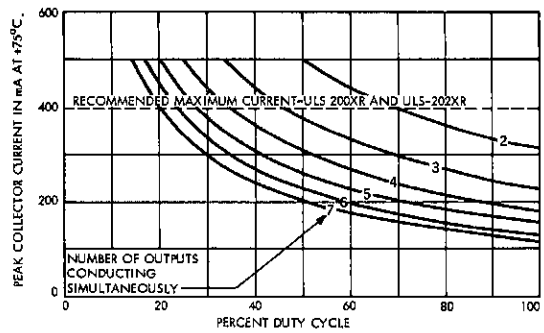
SERIES ULS-2000R

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



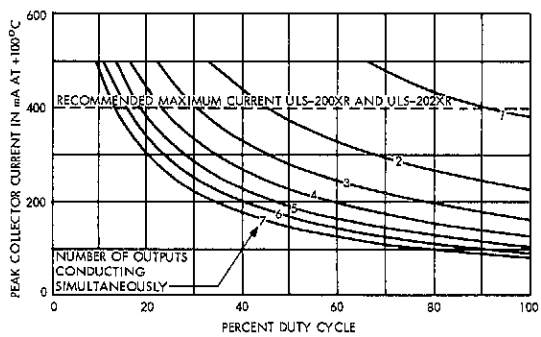
Dwg. No. A-10,883B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



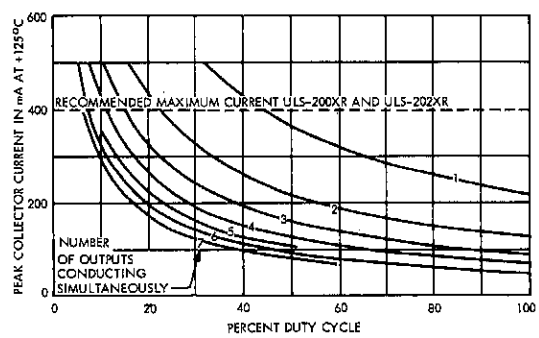
Dwg. No. A-10,887B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,434

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

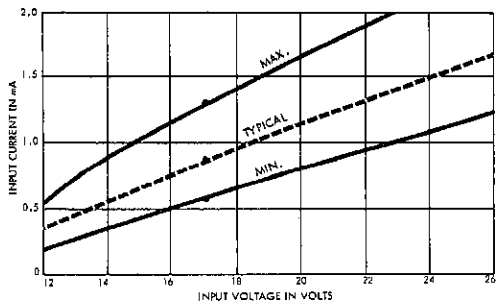


Dwg. No. A-12,435

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

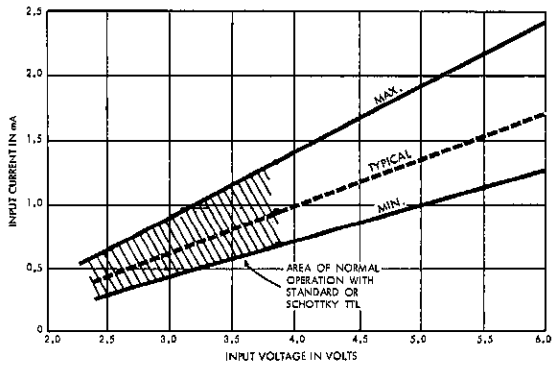
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS-20X2



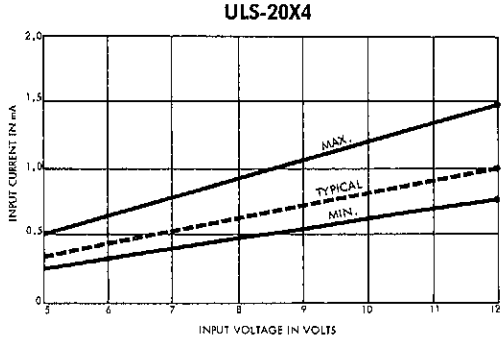
Dwg. No. A-10,225A

ULS-20X3



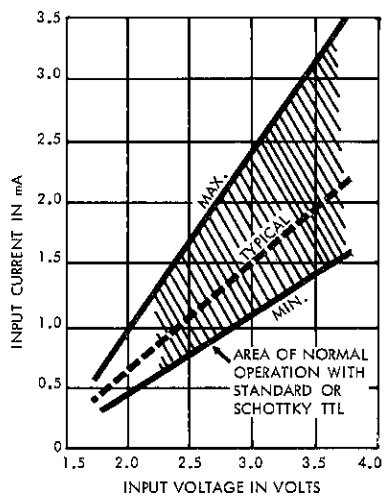
Dwg. No. A-10,224A

ULS-20X4



Dwg. No. A-10,226A

ULS-20X5



Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

ULS-2064H THROUGH ULS-2077H
1.25 A QUAD DARLINGTON SWITCHES
MIL-STD-883 Compliant

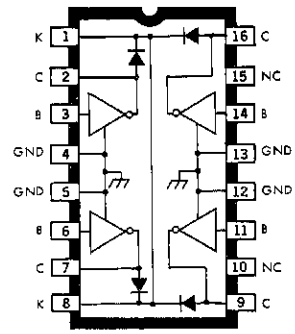
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Units
- Transient-Protected Outputs
- Hermetically Sealed Packages
- High-Reliability Screening to MIL-STD-883, Class B

INTENDED FOR MILITARY, aerospace, and related applications, ULS-2064H through ULS-2077H quad Darlington switches interface between low-level logic and a variety of peripheral power loads such as relays, solenoids, dc and stepping motors, multiplexed LED and incandescent displays, heaters, and similar loads of up to 400 watts (1.25 A per output, 80 V, 12.5% duty cycle, +50°C). The devices are specified with a minimum output breakdown of 50 volts (35 volts sustaining at 100 mA) or 80 volts (50 volts sustaining), and a saturated output current specification of 1.25 A.

The ULS-2064/65/68/69H switches are designed for use with TTL, DTL, Schottky TTL, and 5 V CMOS logic. The ULS-2066/67/70/77H are intended for use with 6 V to 15 V CMOS and PMOS logic. These devices include integral transient-suppression diodes for use with inductive loads.

Types ULS-2068H and ULS-2069H incorporate a pre-driver stage operating from a low-current, 5 V supply. The pre-driver for the ULS-2070H and ULS-2071H operates from a low-current, 12 V supply. The input drive requirements for these devices are reduced, while still allowing the outputs to switch currents up to 1.5 A.



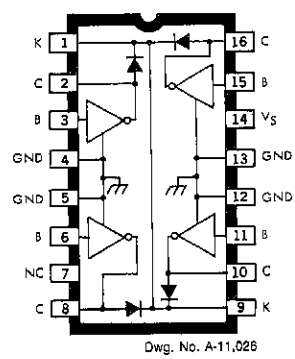
Dwg. No. A-11,025

ULS-2064H—ULS-2067H

The ULS-2074H through ULS-2077H switches are intended for use in emitter-follower applications. These circuits are identical with the ULS-2064H through ULS-2067H except for the uncommitted emitters and the omission of the suppression diodes.

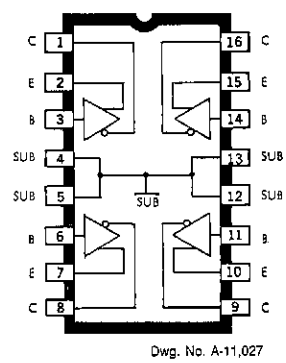
Reverse-bias burn-in and 100% high-reliability screening are standard for all side-brazed hermetic

Continued next page



Dwg. No. A-11,026

ULS-2068H—ULS-2071H



Dwg. No. A-11,027

ULS-2074H—ULS-2077H

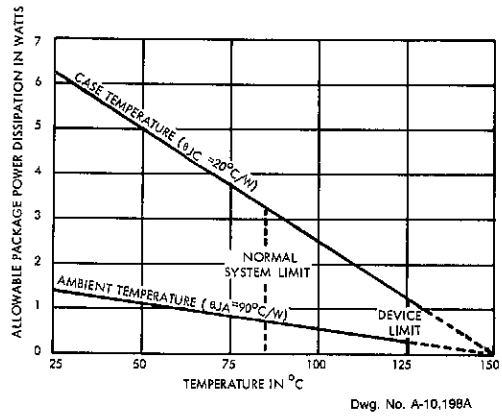
integrated circuits from Sprague Electric Company. Those devices previously manufactured as the ULS-2064H through ULS-2077H are now screened to the additional requirements of MIL-STD-883, Class B, and are so marked.

These quad Darlington switches are supplied in 16-pin ceramic/metal side-brazed hermetic packages. On special order, economical ceramic/glass cer-DIP hermetic packages can be specified by changing the part number suffix from 'H' to 'R'. Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the military temperature range of −55°C to +125°C.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature for any one driver (unless otherwise noted)

Output Voltage, V_{CEX} ..... See Below
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... See Below
Output Current, I_{OUT} (Note 1) ..... 1.5 A
Input Voltage, V_{IN} (Note 2) ..... See Below
Input Current, I_B (Note 3) ..... 25 mA
Supply Voltage, V_S (ULS-2068/69H) ..... 10 V
(ULS-2070/71H) ..... 20 V
Total Package Power Dissipation ..... See Graph
Power Dissipation, P_D/Output ..... 2.2 W
Operating Ambient Temperature Range, T_A . −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



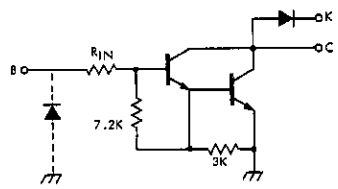
Dwg. No. A-10,198A

Type Number	V_{GEX} (Max.)	$V_{CE(SUS)}$ (Min.)	V_{IN} (Max.)	Application
ULS-2064H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS-2065H	80 V	50 V	15 V	and 5 V CMOS
ULS-2066H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2067H	80 V	50 V	30 V	and PMOS
ULS-2068H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS-2069H	80 V	50 V	15 V	and 5 V CMOS
ULS-2070H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2071H	80 V	50 V	30 V	and PMOS
ULS-2074H	50 V	35 V	30 V	General-Purpose
ULS-2075H	80 V	50 V	60 V	
ULS-2076H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2077H	80 V	50 V	60 V	and PMOS

Notes:
1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is with reference to the substrate (no connection to any other pins) for the ULS-2074/75/76/77H, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

ULS-2064H THROUGH ULS-2067H

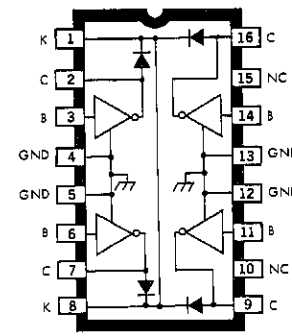
PARTIAL SCHEMATIC



Dwg. No. A-10,353

ULS-2064H
ULS-2065H $R_{IN} = 350\ \Omega$

ULS-2066H
ULS-2067H $R_{IN} = 3\ k\Omega$



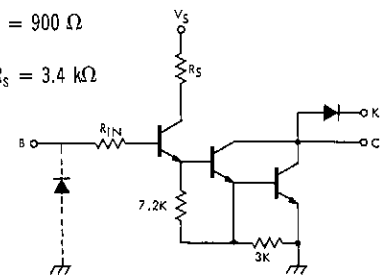
Dwg. No. A-11,025

ULS-2068H THROUGH ULS-2071H

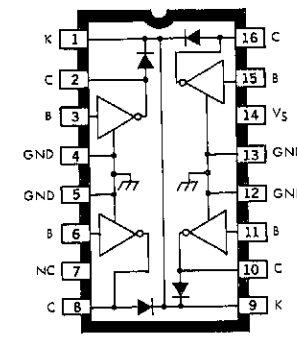
PARTIAL SCHEMATIC

ULS-2068H
ULS-2069H $R_{IN} = 2.5\ k\Omega$, $R_S = 900\ \Omega$

ULS-2070H
ULS-2071H $R_{IN} = 11.6\ k\Omega$, $R_S = 3.4\ k\Omega$



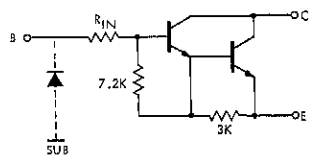
Dwg. No. A-10,354



Dwg. No. A-11,026

ULS-2074H THROUGH ULS-2077H

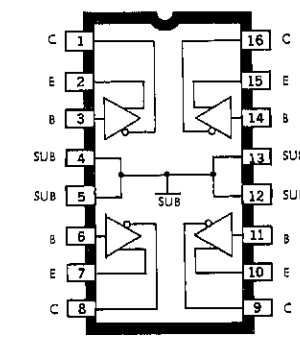
PARTIAL SCHEMATIC



Dwg. No. A-10,355

ULS-2074H
ULS-2075H $R_{IN} = 350\ \Omega$

ULS-2076H
ULS-2077H $R_{IN} = 3\ k\Omega$



Dwg. No. A-11,027

6

ULS-2064H THROUGH ULS-2067H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2064/66H		V_{CE} = 50 V	1	—	500	µA
		ULS-2065/67H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2064/66H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2065/67H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 µA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 µA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{I(ON)}$	ULS-2064/65H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS-2066/67H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{I(ON)}$	ULS-2064/65H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS-2066/67H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS-2064/66H		V_R = 50 V	6	—	100	µA
		ULS-2065/67H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 1.25 A	7	—	2.1	V

ULS-2068H THROUGH ULS-2071H

ELECTRICAL CHARACTERISTICS over operating temperature range, V_S = 5.0 V (ULS-2068/69H) or V_S = 12 V (ULS-2070/71H), (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2068/70H		V_{CE} = 50 V	1	—	500	µA
		ULS-2069/71H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2068/70H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2069/71H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ULS-2068/69H	−55°C	I_C = 500 mA, V_{IN} = 3.2 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 3.2 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 3.2 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 3.2 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 2.9 V	3	—	1.20	V
				I_C = 750 mA, V_{IN} = 2.9 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 2.9 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 2.9 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 2.8 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 2.8 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 2.8 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 2.8 V	3	—	1.95	V
		ULS-2070/71H	−55°C	I_C = 500 mA, V_{IN} = 5.5 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.5 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.5 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.5 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 5.1 V	3	—	1.20	V
				I_C = 750 mA, V_{IN} = 5.1 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 5.1 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 5.1 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.0 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.0 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.0 V	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2068/69H	−55°C	V_{IN} = 3.2 V	4	—	600	µA
			+25°C	V_{IN} = 2.75 V	4	—	550	µA
			+125°C	V_{IN} = 2.75 V	4	—	850	µA
				V_{IN} = 3.75 V	4	—	1400	µA
		ULS-2070/71H	−55°C to +25°C	V_{IN} = 5.0 V	4	—	400	µA
				V_{IN} = 12 V	4	—	1250	µA
			+125°C	V_{IN} = 5.0 V	4	—	800	µA
				V_{IN} = 12 V	4	—	1600	µA
Input Voltage	$V_{IN(ON)}$	ULS-2068/69H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.2	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.75	V
		ULS-2070/71H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
Supply Current	I_S	ULS-2068/69H		I_C = 500 mA, V_{IN} = 3.2 V	8	—	6.0	mA
		ULS-2070/71H	−55°C to +25°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	4.5	mA
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	6.0	mA
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS-2068/70H		V_R = 50 V	6	—	100	µA
		ULS-2069/71H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 1.25 A	7	—	2.1	V

6

ULS-2074H THROUGH ULS-2077H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2074/76H		V_{CE} = 50 V	1	—	500	µA
		ULS-2075/77H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2074/76H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2075/77H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 µA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 µA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2074/75H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS-2076/77H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS-2074/75H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS-2076/77H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs

TEST FIGURES

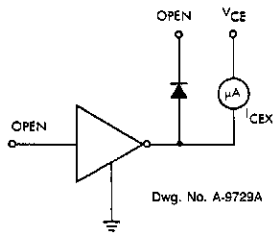


Figure 1

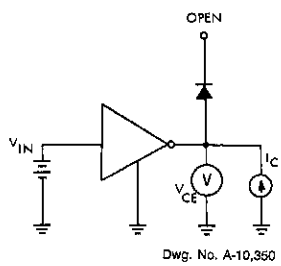


Figure 2

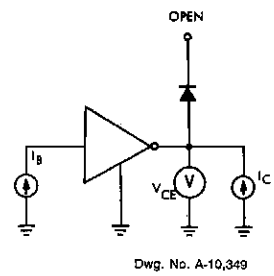


Figure 3

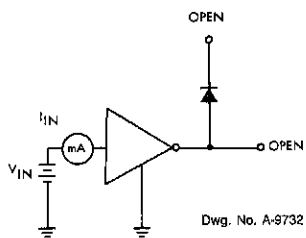


Figure 4

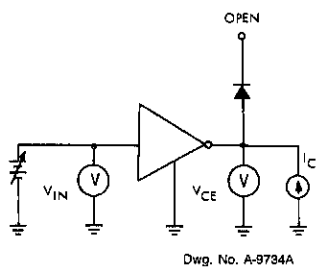


Figure 5

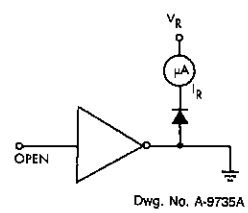


Figure 6

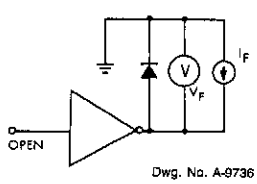


Figure 7

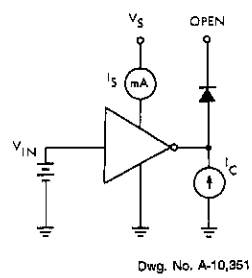
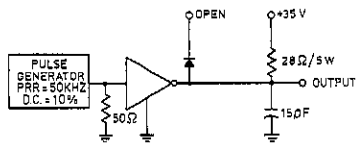


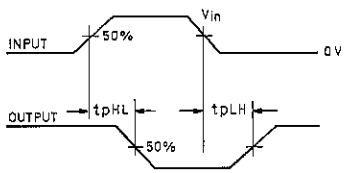
Figure 8

NOTE: Diodes not applicable to Types ULS-2074H through ULS-2077H.



Dwg. No. A-13,247

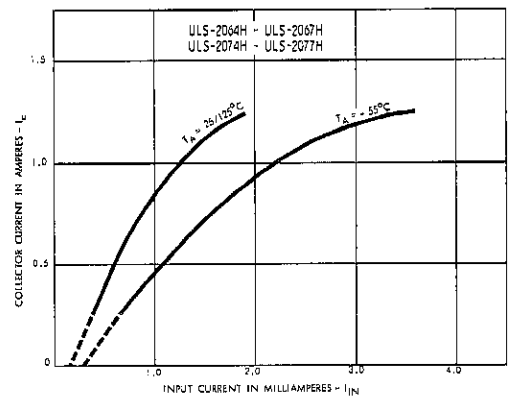
	V_{in}
ULS-2064/65/68/69/74/75H	2.4V
ULS-2066/67/70/71/76/77H	5.0V



Dwg. No. A-13,248

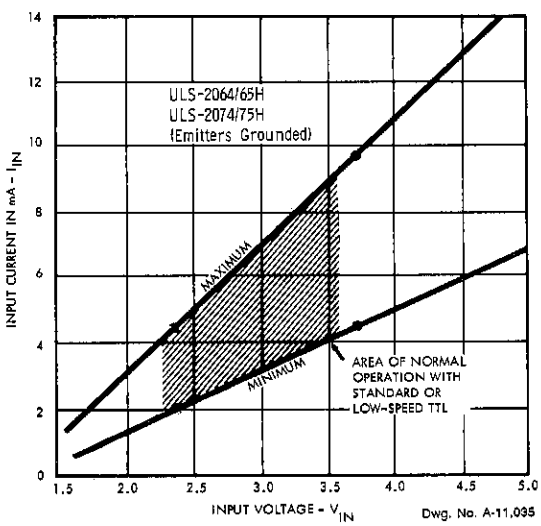
Figure 9

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

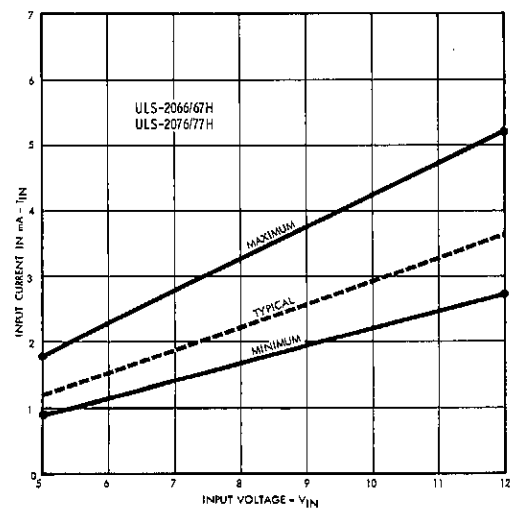


Dwg. No. A-11,030

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

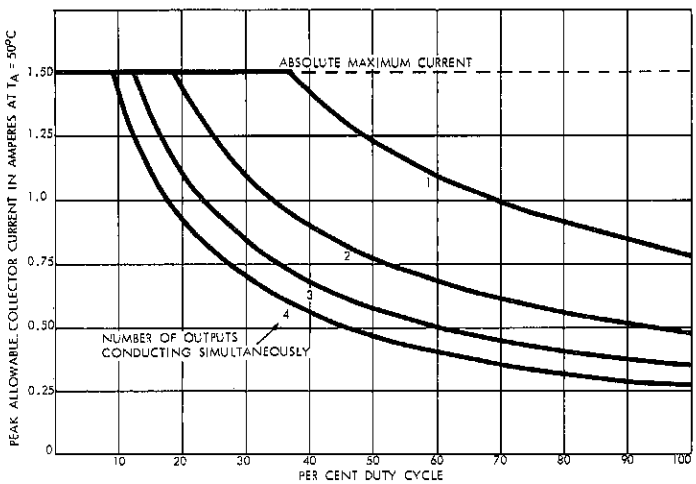


Dwg. No. A-11,035



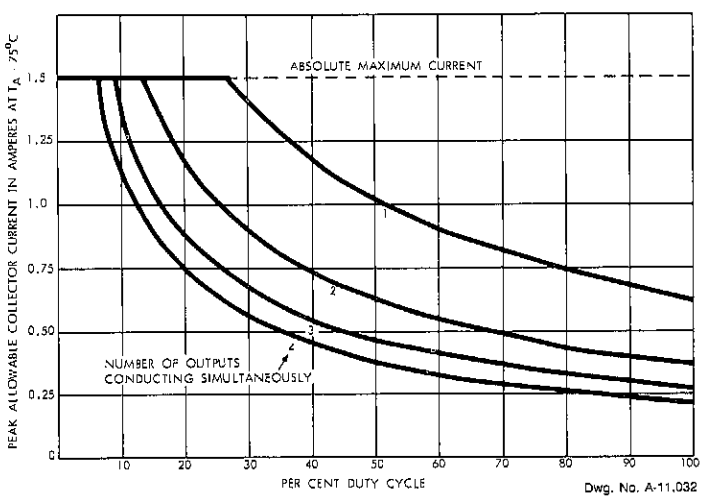
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT T_A = +50°C



Dwg. No. A-11,031

AT T_A = +75°C

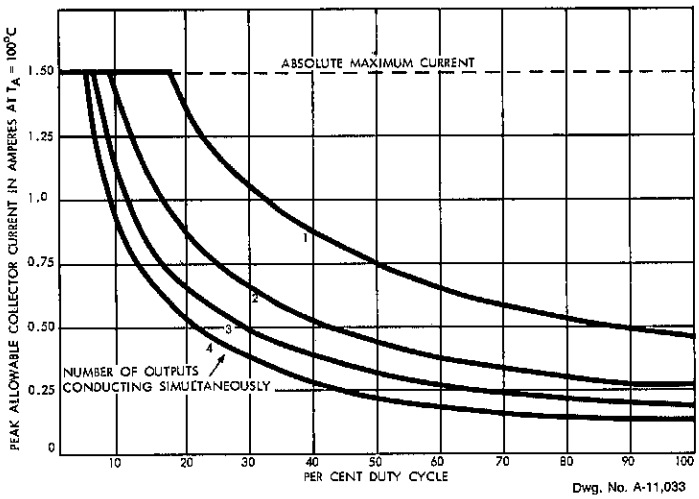


Dwg. No. A-11,032

6

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT T_A = +100°C



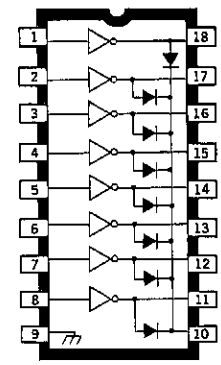
Dwg. No. A-11,033

SERIES ULS-2800H AND ULS-2800R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

MIL-STD-883 Compliant

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- Side-Brazed Hermetic Package
- Cer-DIP Hermetic Package
- High-Reliability Screening to MIL-STD-883, Class B
- −55°C to +125°C Temperature Range



Dwg. No. A-10,322

DESIGNED TO SERVE as interface between low-level logic circuitry and high-power loads, Series ULS-2800H and ULS-2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. They are ideally suited to driving relays, solenoids, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A output current per package.

These devices are screened to MIL-STD-883, Class B and are supplied in either the popular ceramic/metal side-brazed 18-pin hermetic package (suffix 'H') or ceramic/glass cer-DIP hermetic package (suffix 'R'). Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of −55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 30 integrated circuits described in this bulletin permit the circuit designer to select the optimal device for any application. In addition to the two package styles, there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.

Device Part Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Part Number		
General Purpose PMOS, CMOS	ULS-2801*	ULS-2811*	ULS-2821*
14-25 V PMOS	ULS-2802*	ULS-2812*	ULS-2822*
5 V TTL, CMOS	ULS-2803*	ULS-2813*	ULS-2823*
6-15 V CMOS, PMOS	ULS-2804*	ULS-2814*	ULS-2824*
High-Output TTL	ULS-2805*	ULS-2815*	ULS-2825*

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP)

6

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
- (ULS-280X*, ULS-281X*) . . . . . 50 V
- (ULS-282X*) . . . . . 95 V

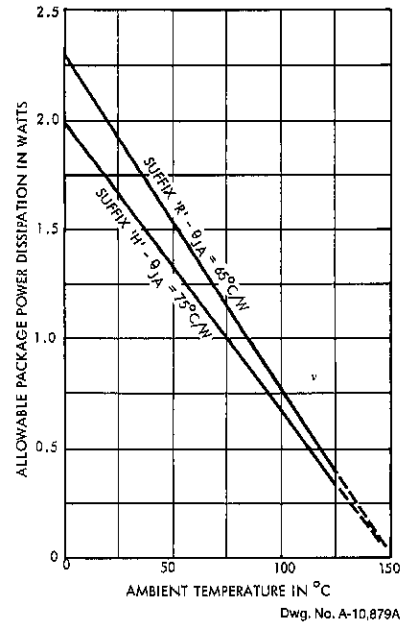
Input Voltage, V_{IN}
- (ULS-28X2, X3, X4*) . . . . . 30 V
- (ULS-28X5*) . . . . . 15 V

Peak Output Current, I_{OUT}
- (ULS-280X*, ULS-282X*) . . . . . 500 mA
- (ULS-281X*) . . . . . 600 mA

Ground Terminal Current, I_{GND} . . . . . 3.0 A
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D
- (one Darlington pair) . . . . . 1.0 W
- (total package) . . . . . See Graph

Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

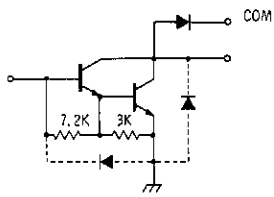
ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,879A

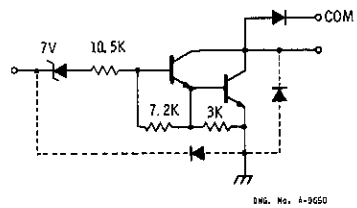
PARTIAL SCHEMATICS

ULS-28X1*
(Each Driver)



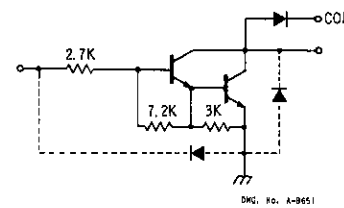
Dwg. No. A-9595

ULS-28X2*
(Each Driver)



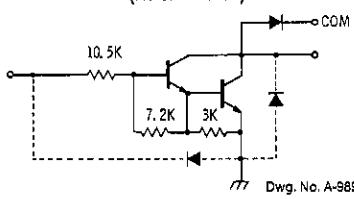
Dwg. No. A-9650

ULS-28X3*
(Each Driver)



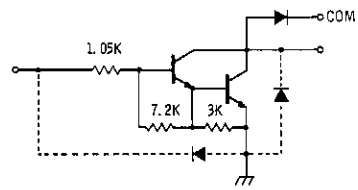
Dwg. No. A-9651

ULS-28X4*
(Each Driver)



Dwg. No. A-9898A

ULS-28X5*
(Each Driver)



Dwg. No. A-10,228

**Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP). X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.*

SERIES ULS-2800H AND ULS-2800R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2802*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2804*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{I(ON)}$	ULS-2802*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2803*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2804*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2805*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{I(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{I(ON)}$	ULS-2802*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2803*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2804*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2805*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2801*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{I(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2810H AND ULS-2810R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2812*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2814*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2812*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2813*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2814*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2815*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2812*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
		ULS-2013*	−55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V
		ULS-2814*	−55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS-2815*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2811*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2820H AND ULS-2820R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS-2822*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2824*	25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2822*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2823*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2824*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2825*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2822*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2823*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2824*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2825*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2821*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

TEST FIGURES

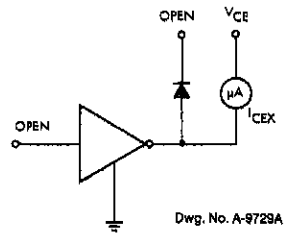


FIGURE 1A

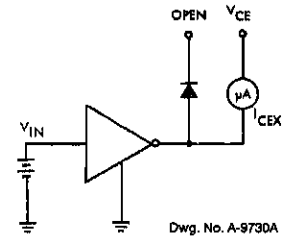


FIGURE 1B

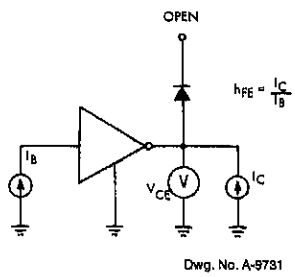


FIGURE 2

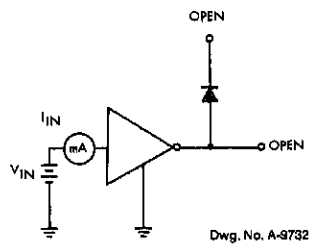


FIGURE 3

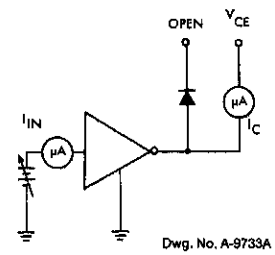


FIGURE 4

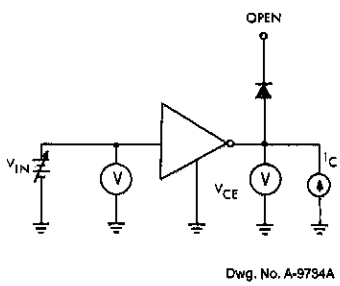


FIGURE 5

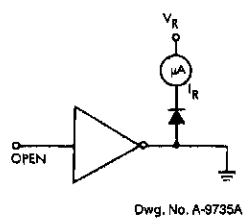


FIGURE 6

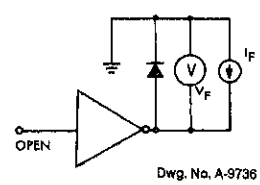
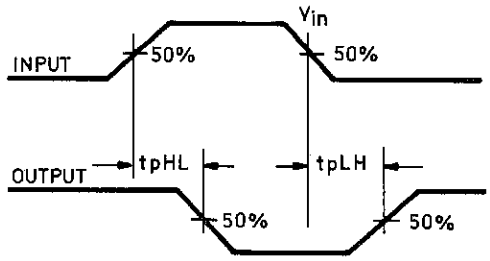
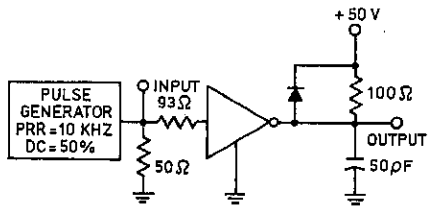


FIGURE 7

	V_{in}
ULS-28X1*	3.5 V
ULS-28X2*	13 V
ULS-28X3*	3.5 V
ULS-28X4*	12 V
ULS-28X5*	3.5 V



Dwg. No. A-13,272

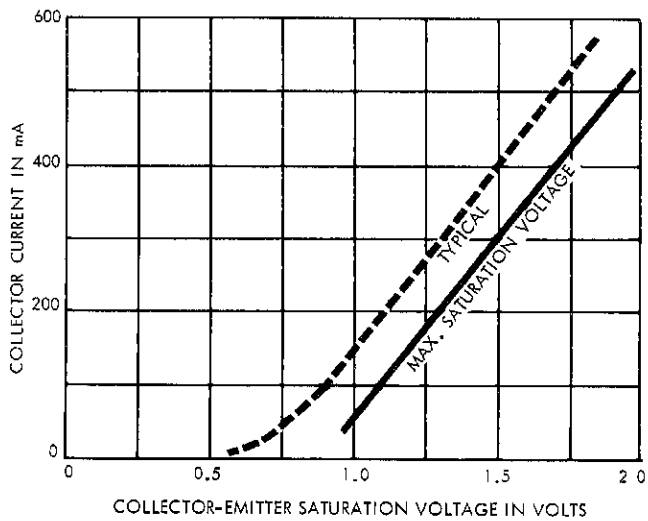


Dwg. No. A-13,273

* Complete part number includes a final letter to indicate package.
X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

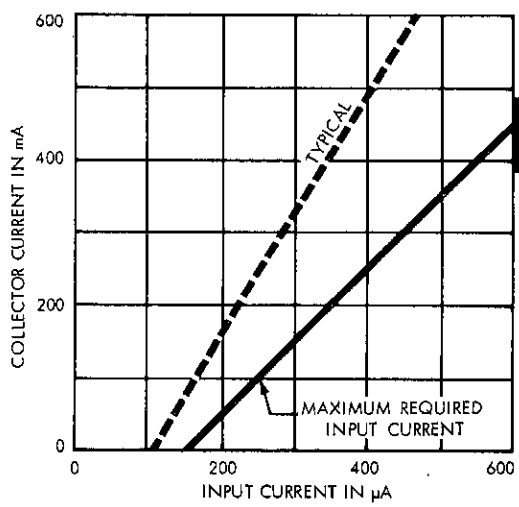
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

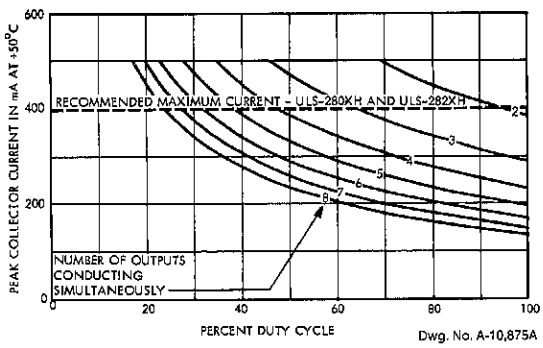


Dwg. No. A-10,872B

6

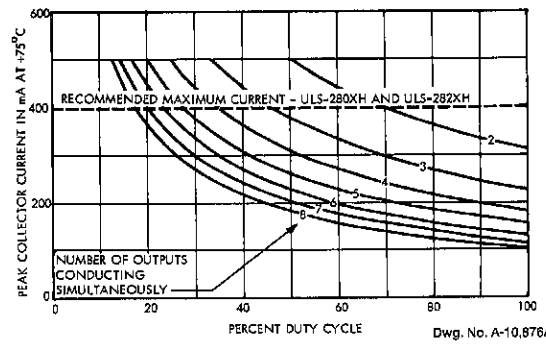
SERIES ULS-2800H

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



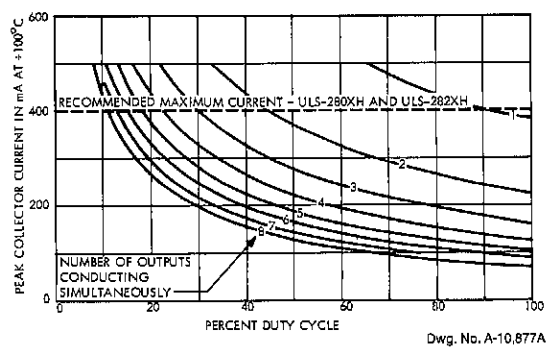
Dwg. No. A-10,875A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



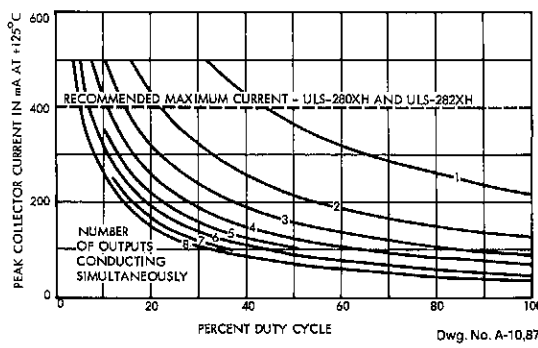
Dwg. No. A-10,876A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,877A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

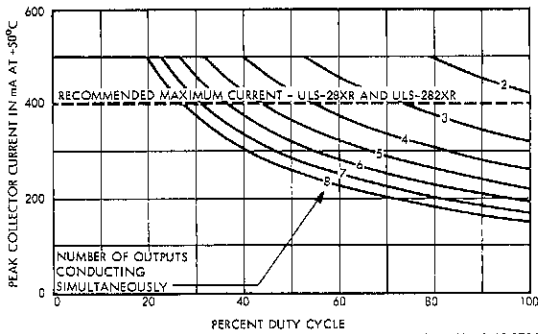


Dwg. No. A-10,878A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

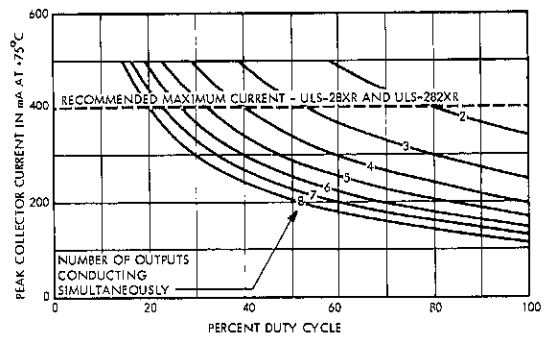
SERIES ULS-2800R

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



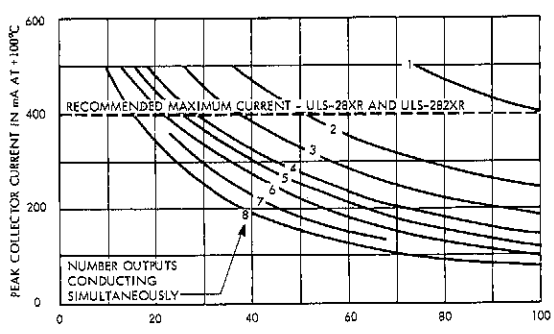
Dwg. No. A-10,870A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



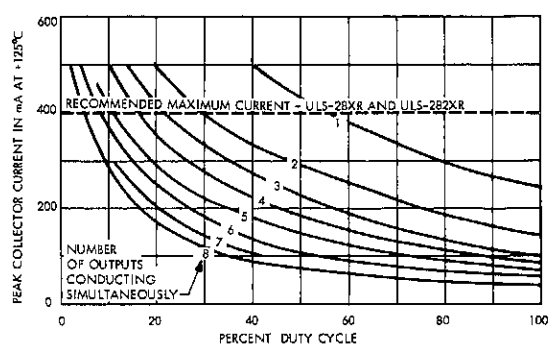
Dwg. No. A-10,871A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,466

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

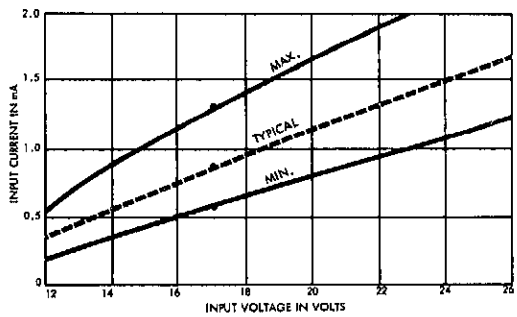


Dwg. No. A-12,467

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

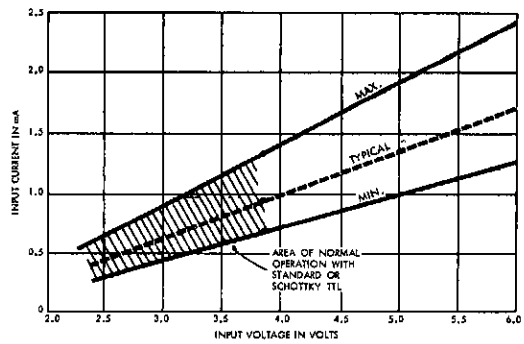
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS-28X2



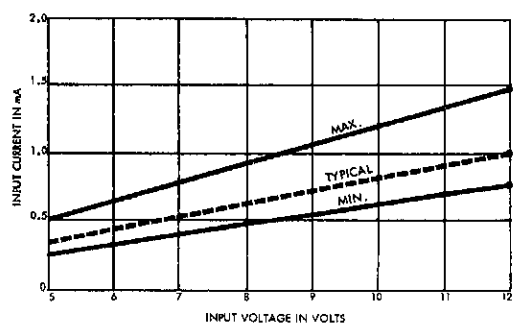
Dwg. No. A-10,225A

ULS-28X3



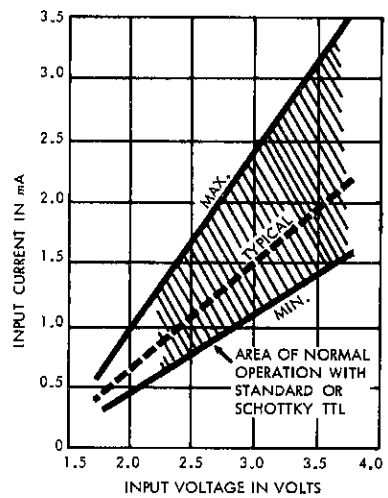
Dwg. No. A-10,224A

ULS-28X4



Dwg. No. A-10,226A

ULS-28X5



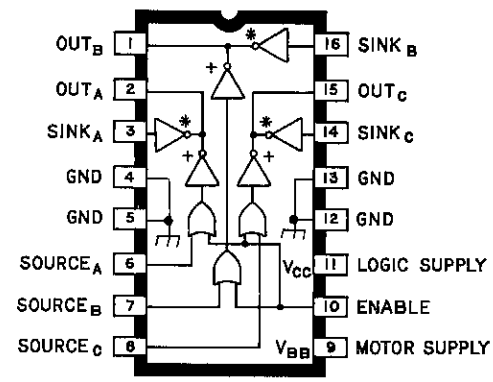
Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

UDS-2933H AND UDS-2934H
HERMETIC 3-CHANNEL HALF-BRIDGE MOTOR DRIVERS
MIL-STD-883 Compliant

FEATURES

- Output Currents to 1 A
- Output Voltage to 30 V
- Low Output-Saturation Voltage
- Transient-Protected Outputs
- Tri-State Outputs
- TTL or CMOS Compatible Inputs
- High-Reliability Screening to MIL-STD-883, Class B



Dwg. No. A-13,059

Developed for use in 3-phase brushless dc motor applications, the UDS-2933H and UDS-2934H half-bridge drivers provide output capabilities to 0.6 A and 30 V. Saturated drivers provide for low output voltage drops at maximum rated current.

The two devices differ only in input logic and supply levels: the UDS-2933H is compatible with TTL and 5 V CMOS; the UDS-2934H is used with 12 V CMOS. An ENABLE input controls the source drivers and can be used for PWM operation. The chopper drive mode is characterized by low load power dissipation levels and maximum efficiency. Both ground clamp and flyback diodes for each output are provided.

Under normal operating conditions, the UDS-2933H and UDS-2934H will drive one pair of motor windings (1 source and 1 sink ON) continuously at 250 mA and an ambient temperature of +98°C or +73°C respectively.

Both devices are supplied in glass/metal side-brazed 16-pin hermetic packages conforming to the dimensional requirements of MIL-M-38510. They are rated for operation over a temperature range of −55°C to +125°C. Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

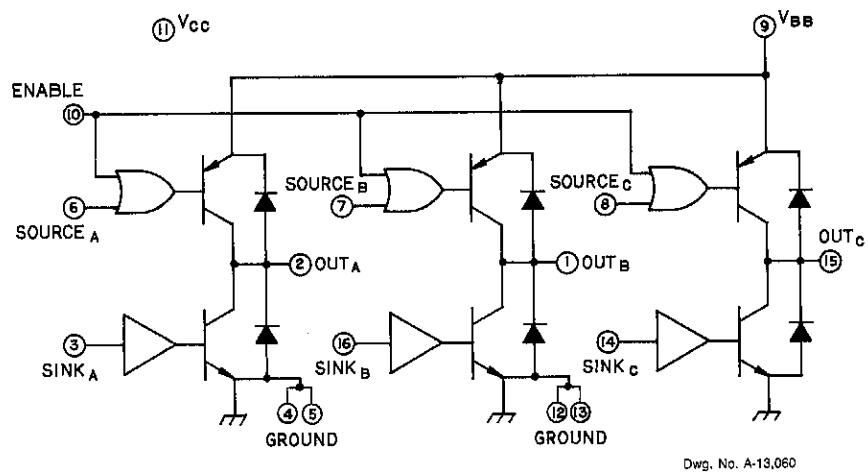
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Motor Supply Voltage Range, V_{BB} . . . . . 30 V
Logic Supply Voltage Range, V_{CC}
(UDS-2933H) . . . . . 4.5 V to 7.0 V
(UDS-2934H) . . . . . 10 V to 15 V
Logic Input Voltage, V_{IN} . . . . . V_{CC}
Output Current, I_{OUT} . . . . . ±0.6 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

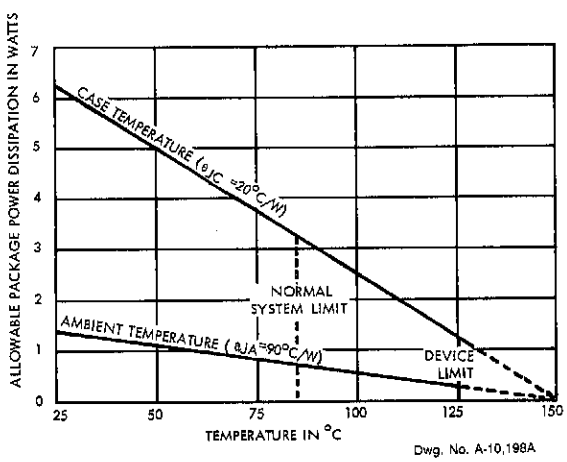
NOTE: Output current rating will be limited by ambient temperature, number of outputs conducting, duty cycle, air flow, and adjacent heat sources. Under any set of conditions, do not exceed the ±0.6 A output current rating or a junction temperature of +150°C.

6

FUNCTIONAL BLOCK DIAGRAM



ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



TRUTH TABLE

Sink Driver Input	Source Driver Input	Enable Input	Output
Low	Low	Low	High
Low	High	Low	Open
High	Low	Low	Disallowed
High	High	Any	Low
High	Any	High	Low
Low	Any	High	Open

ELECTRICAL CHARACTERISTICS at $-55°C \le T_A \le +125°C$, $V_{BB} = 30\,V$, $V_{CC} = 5\,V$ (UDS-2933H) or $V_{CC} = 12\,V$ (UDS-2934H)

Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	All Drivers OFF, $V_{OUT} = 0\,V$	—	−5.0	−500	µA
			All Drivers OFF, $V_{OUT} = 30\,V$	—	5.0	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	All	$I_{OUT} = -100\,mA$	—	—	1.1	V
			$I_{OUT} = 100\,mA$	—	—	0.2	V
			$I_{OUT} = -250\,mA$	—	—	1.2	V
			$I_{OUT} = 250\,mA$	—	—	0.3	V
			$I_{OUT} = -500\,mA$	—	—	1.5	V
			$I_{OUT} = 500\,mA$	—	—	0.6	V
Motor Supply Current	I_{BB}	All	All Drivers OFF	—	50	200	µA
			1 Source + 1 Sink ON, No Loads	—	1.0	1.3	mA
Clamp Diode Forward Voltage	V_F	All	$I_F = 500\,mA$	—	1.3	2.0	V
Logic Input Voltage	$V_{IN(1)}$	2933H		2.4	—	—	V
		2934H		8.0	—	—	V
	$V_{IN(0)}$	2933H		—	—	0.4	V
		2934H		—	—	4.0	V
Logic Input Current	$I_{IN(1)}$	2933H	$V_{IN} = 2.4\,V$	—	<1.0	10	µA
		2934H	$V_{IN} = 8.0\,V$	—	<1.0	10	µA
	$I_{IN(0)}$	All	$V_{IN} = 0.8\,V$	—	−50	−300	µA
Logic Supply Current	I_{CC}	All	All Drivers OFF	—	3.0	6.0	mA
			1 Source + 1 Sink ON	—	30	40	mA
Output Rise Time at $T_A = +25°C$	t_r	All	$I_{OUT} = -500\,mA$, $V_{BB} = 20\,V$	—	250	—	ns
			$I_{OUT} = 500\,mA$, $V_{BB} = 20\,V$	—	150	—	ns
Output Fall Time at $T_A = +25°C$	t_f	All	$I_{OUT} = -500\,mA$, $V_{BB} = 20\,V$	—	500	—	ns
			$I_{OUT} = 500\,mA$, $V_{BB} = 20\,V$	—	30	—	ns

NOTES: 1. Each driver is tested separately.
2. Positive (negative) current is defined as going into (coming out of) the specified device pin.
*Complete part number includes prefix UDS-

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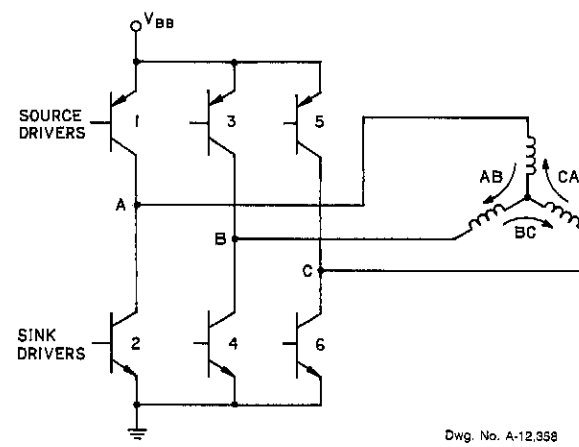
TYPICAL COMMUTATION SEQUENCE

Drivers ON*	Motor Current	Elec. Degrees
1 + 4	AB	0
1 + 6	−CA	60
3 + 6	BC	120
3 + 2	−AB	180
5 + 2	CA	240
5 + 4	−BC	300

*ENABLE input must be low; Source drivers are turned ON with a logic low, sink drivers are turned ON with a logic high.



Dwg. No. A-12,358

SERIES UDS-2980H AND UDS-2980R HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

MIL-STD-883 Compliant

FEATURES

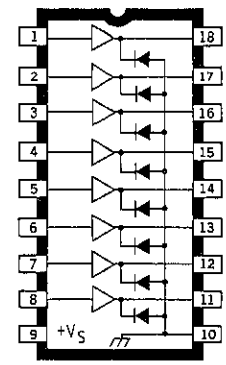
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C

SERIES UDS-2980H and UDS-2980R hermetically sealed source drivers link standard low-power digital logic and relays, solenoids, stepping motors, LEDs, and lamps in applications requiring separate logic and load grounds, load supply voltages to +80 V, and load currents to 500 mA.

Types UDS-2981H/R and UDS-2983H/R are intended for use with 5 V logic systems (TTL, Schottky TTL, DTL and 5 V CMOS). UDS-2982H/R and UDS-2984H/R integrated circuits are intended for MOS interface (PMOS and CMOS) operating from supply voltages of from 6 to 16 V.

Types UDS-2981H/R and UDS-2982H/R will withstand an output OFF voltage of 50 V. UDS-2983H/R and UDS-2984H/R drivers will withstand a maximum output OFF voltage of 80 V.

Under normal operating conditions, the devices will sustain 50 mA continuously on each of the eight outputs at an ambient temperature of +85°C and with a supply voltage of 15 V. All types include input current-limiting resistors and output transient-suppression diodes. In all cases, outputs are switched ON by an active high input level.



Dwg. No. A-10,243

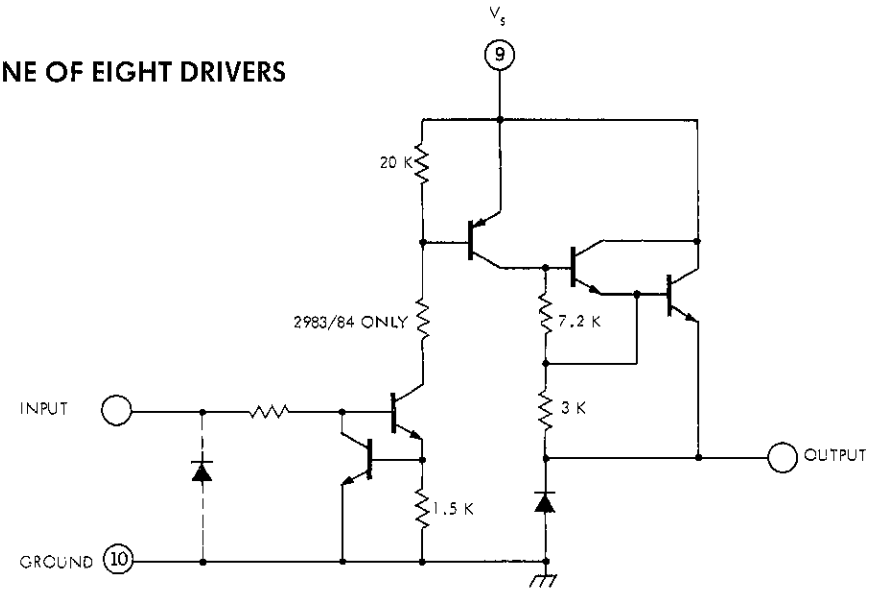
Note that the maximum current rating may not be obtained at −55°C because of reduced beta, or at +125°C because of package power limitations.

Series UDS-2980H drivers are furnished in 18-pin ceramic/metal (side-brazed) hermetic dual in-line packages. Series UDS-2980R drivers are supplied in ceramic/glass (cer-DIP) hermetic packages. Both are processed to the requirements of MIL-STD-883, Class B.

The same circuits are also available in 18-pin plastic dual in-line packages (Series UDN-2980A) for operation over a limited temperature range, or where higher package power dissipation is needed.

Device Type	$V_{CE(MAX)}$	$V_{IN(MAX)}$	Applications
UDS-2981H/R	50 V	15 V	TTL, DTL, 5 V CMOS
UDS-2982H/R	50 V	30 V	6-15 V CMOS/PMOS
UDS-2983H/R	80 V	15 V	TTL, DTL, 5 V CMOS
UDS-2984H/R	80 V	30 V	6-15 V CMOS/PMOS

ONE OF EIGHT DRIVERS



Dwg. No. A-10,242B

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

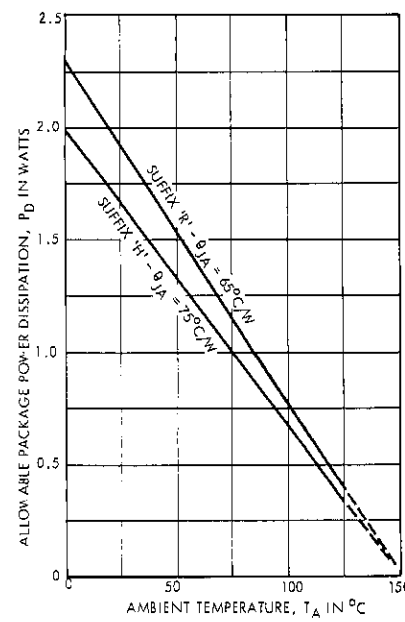
Output Voltage Range, V_{CE}
- (UDS-2981 and UDS-2982H/R) ..... +5 V to +50 V
- (UDS-2983 and UDS-2984H/R) ..... +35 V to +80 V

Input Voltage, V_{IN}
- (UDS-2981 and UDS-2983H/R) ..... −15 V
- (UDS-2982 and UDS-2984H/R) ..... −30 V

Output Current, I_{OUT} ..... −500 mA
Ground Terminal Current, I_{GND} ..... 3.0 A
Power Dissipation, P_D
- (any one driver) ..... 1.1 W
- (total package) ..... See Graph

Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,879A

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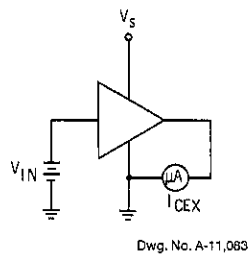
ELECTRICAL CHARACTERISTICS from −55°C to +125°C (unless otherwise specified)

Characteristic	Symbol	Applicable Devices†	Temp.	Test Conditions	Fig.	Limit
Maximum Output Leakage Current	I_{CEX}	UDS-2981/82		V_{IN} = 0.25 V*, V_S = 50 V	1	200 µA
		UDS-2983/84		V_{IN} = 0.25 V*, V_S = 80 V	1	200 µA
Maximum Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDS-2981/83	−55°C	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	2.0 V
				V_{IN} = 2.4 V, I_{OUT} = −200 mA	2	2.1 V
			+25°C	V_{IN} = 2.4 V, I_{OUT} = −350 mA	2	2.0 V
			+125°C	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	1.8 V
				V_{IN} = 2.4 V, I_{OUT} = −200 mA**	2	1.9 V
		UDS-2982/84	−55°C	V_{IN} = 5.0 V, I_{OUT} = −100 mA	2	2.0 V
				V_{IN} = 5.0 V, I_{OUT} = −200 mA	2	2.1 V
			+25°C	V_{IN} = 5.0 V, I_{OUT} = −350 mA	2	2.0 V
			+125°C	V_{IN} = 5.0 V, I_{OUT} = −100 mA	2	1.8 V
				V_{IN} = 5.0 V, I_{OUT} = −200 mA**	2	1.9 V
Maximum Input Current	$I_{IN(ON)}$	All		V_{IN} = 2.4 V	3	295 µA
				V_{IN} = 3.85 V	3	600 µA
				V_{IN} = 12 V	3	2.3 mA
	$I_{IN(OFF)}$	UDS-2981/82		V_{IN} = 0 V, V_S = 50 V	3	10 µA
		UDS-2983/84		V_{IN} = 0 V, V_S = 80 V	3	10 µA
Minimum Output Source Current	I_{OUT}	UDS-2981/83		V_{IN} = 2.4 V, V_{CE} = 2.2 V	2	−200 mA
		UDS-2982/84		V_{IN} = 5.0 V, V_{CE} = 2.2 V	2	−200 mA
Maximum Supply Current (Outputs Open)	I_S	UDS-2981	+25°C	V_{IN} = 2.4 V*, V_S = 50 V	4	10 mA
		UDS-2982		V_{IN} = 5.0 V*, V_S = 50 V	4	10 mA
		UDS-2983		V_{IN} = 2.4 V*, V_S = 80 V	4	10 mA
		UDS-2984		V_{IN} = 5.0 V*, V_S = 80 V	4	10 mA
Maximum Turn-ON Delay Time	t_{pHL}	UDS-2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	2.0 µs
		UDS-2983/84		V_S = 50 V, R_L = 250 Ω	7	2.0 µs
Maximum Turn-OFF Delay Time	t_{pLH}	UDS-2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	10 µs
		UDS-2983/84		V_S = 50 V, R_L = 250 Ω	7	10 µs
Maximum Clamp Diode Leakage Current	I_R	UDS-2981/82		V_S = 50 V (All Inputs V_{IN} = 0.25 V)	5	50 µA
		UDS-2983/84		V_S = 80 V (All Inputs V_{IN} = 0.25 V)	5	50 µA
Maximum Clamp Diode Forward Voltage	V_F	ALL		I_F = 200 mA	6	1.75 V

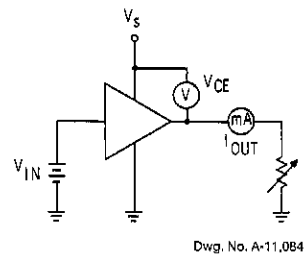
*All inputs simultaneously.
**Pulsed test.
†Complete part number includes a terminal letter that indicates package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

TEST FIGURES



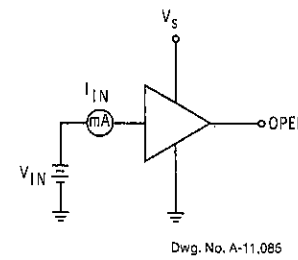
Dwg. No. A-11,083

Figure 1



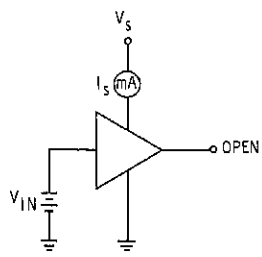
Dwg. No. A-11,084

Figure 2



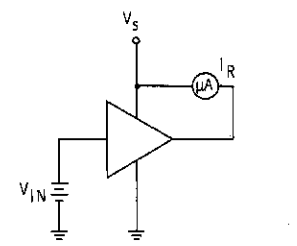
Dwg. No. A-11,085

Figure 3



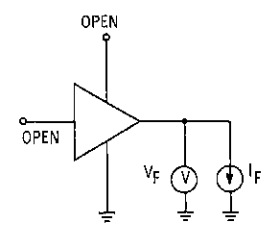
Dw.No. A-11,086

Figure 4



Dwg. No. A-11,087

Figure 5



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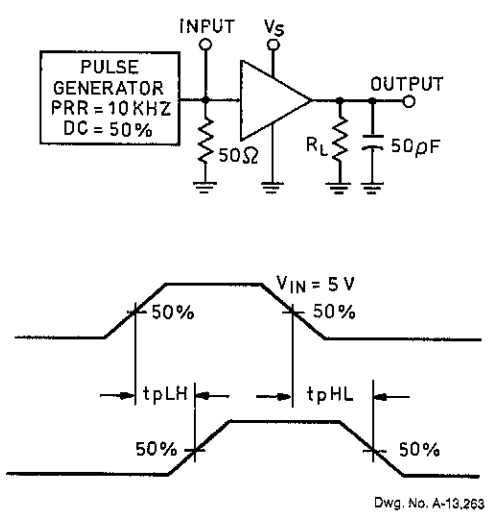
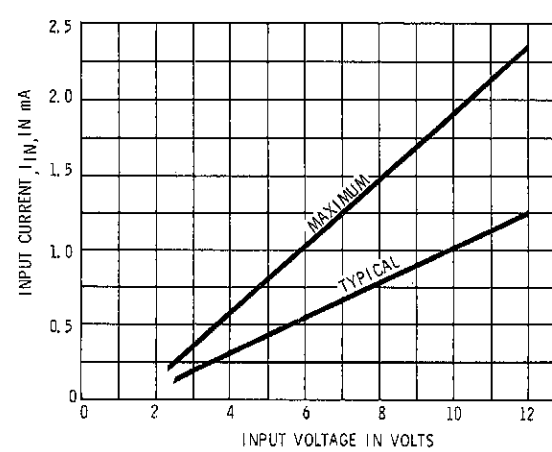


Dwg. No. A-13,263

Figure 7

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

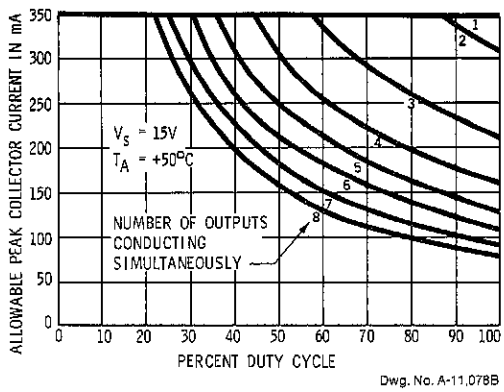


Dwg. No. A-11,115B

6

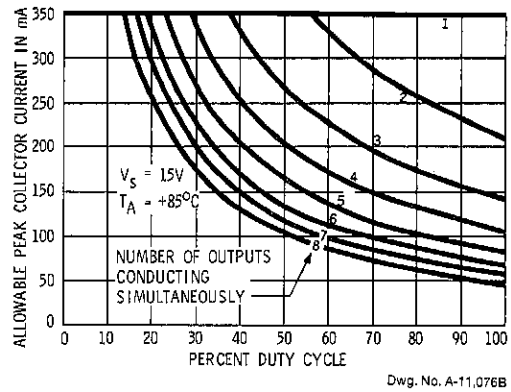
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDS-2980H

UDS-2981/82H



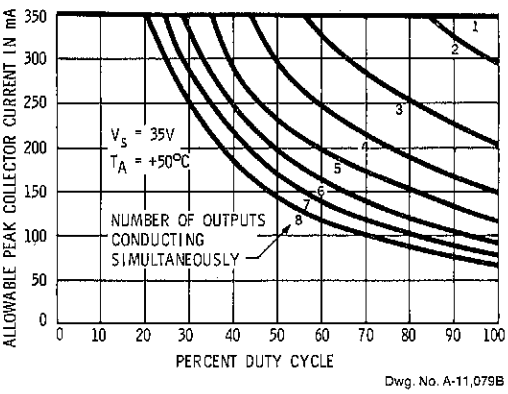
Dwg. No. A-11,078B

UDS-2981/82H



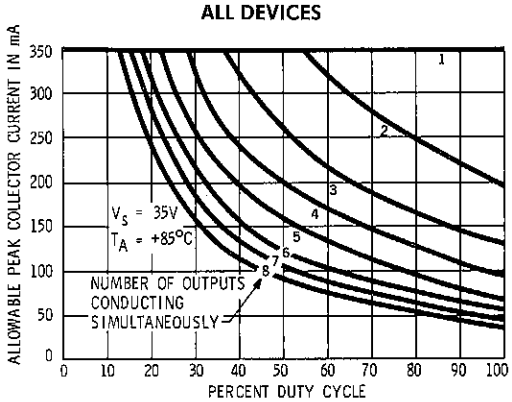
Dwg. No. A-11,076B

ALL DEVICES



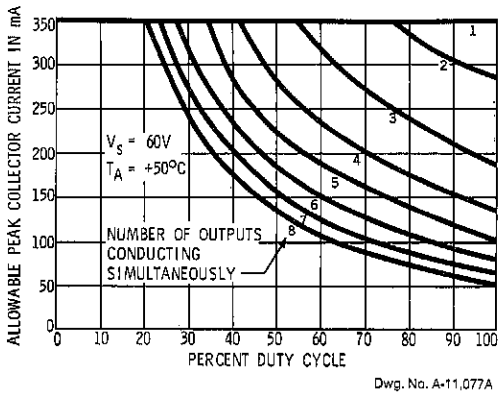
Dwg. No. A-11,079B

ALL DEVICES



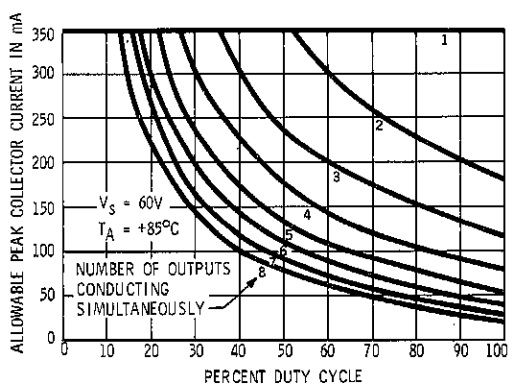
Dwg. No. A-11,080B

UDS-2983/84H



Dwg. No. A-11,077A

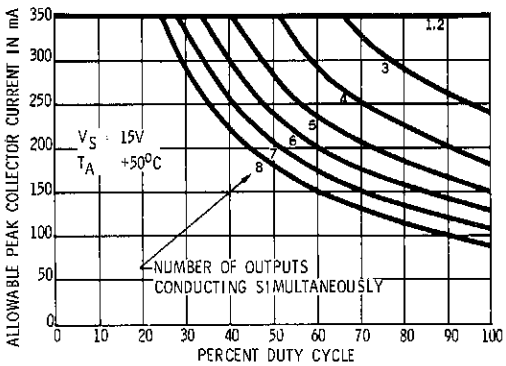
UDS-2983/84H



Dwg. No. A-11,081A

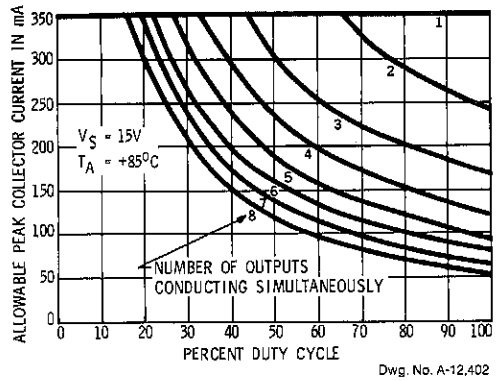
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDS-2980R

UDS-2981/82R



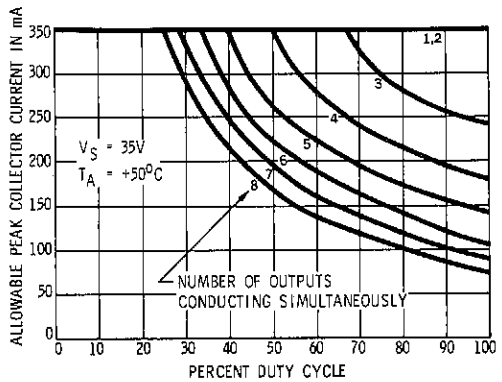
Dwg. No. A-12,401

UDS-2981/82R



Dwg. No. A-12,402

ALL DEVICES



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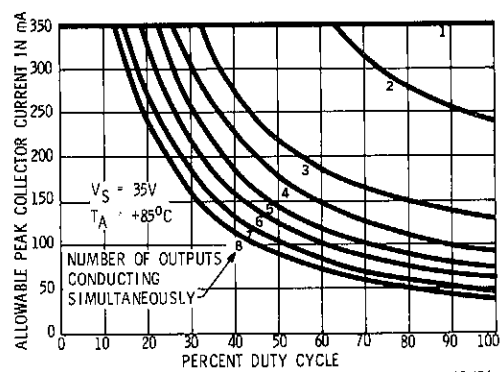
ALL DEVICES



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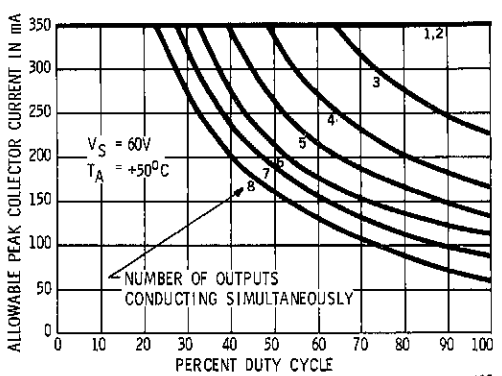
UDS-2983/84R



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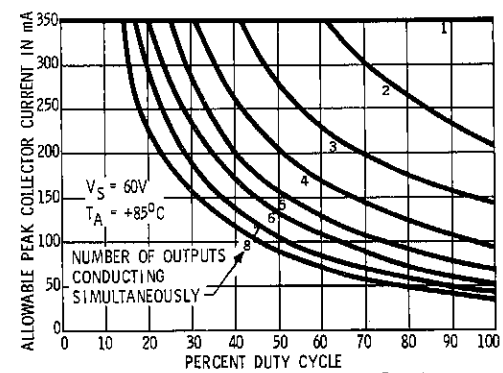


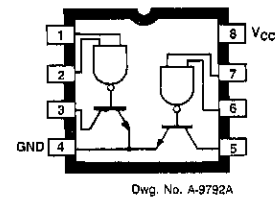
Dwg. No. A-12,406

6

SERIES UDS-3610H
DUAL 2-INPUT PERIPHERAL/POWER DRIVERS

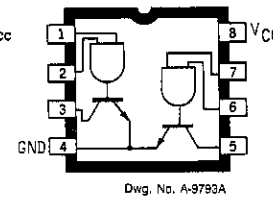
FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Hermetically Sealed Package
- High-Reliability Screening



Dwg. No. A-9792A

UDS-3611H



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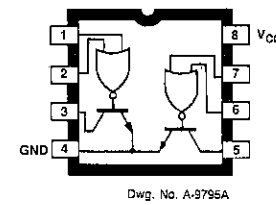
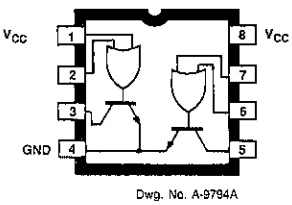
UDS-3612H



Dwg. No. A-9795A

UDS-3613H



Dwg. No. A-9794A

UDS-3614H

THESE mini-DIP dual 2-input peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 250 mA continuously at an ambient temperature of +75°C. In the OFF state, these drivers will withstand at least 80 V. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

The Series UDS-3610H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

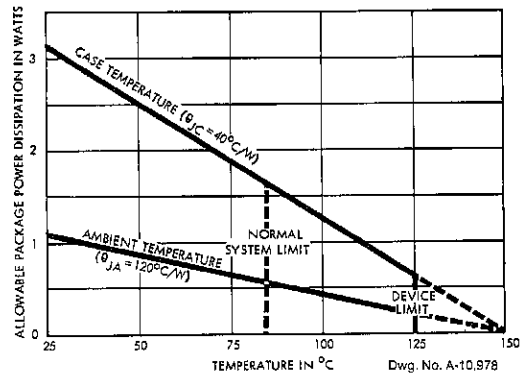
With appropriate external diode transient suppression, Series UDS-3610H drivers can also be used with inductive loads such as relays, solenoids, and stepping motors. Similar devices with integral transient suppression are in Series UDS-5710H.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{In}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Power Dissipation, P_D (One Output)	1.0 W
(Total Package)	See Graph
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

These devices are NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.

ALLOWABLE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE



RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions			Limits				Notes
		V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	Min.	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"1" Input Current	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
Input Clamp Voltage	V_I	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 W) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 W) C_L = 15 pF	—	300	750	ns	3

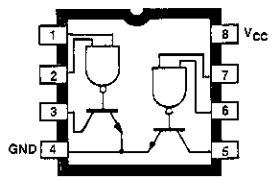
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_r \leq$ 7 ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	$t_f \leq$ 14 ns	PRR = 500 kHz

6

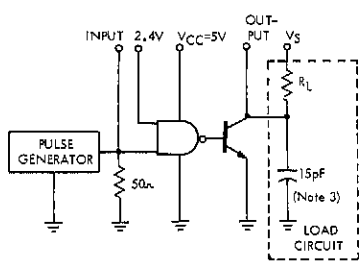
UDS-3611H
Dual AND Driver



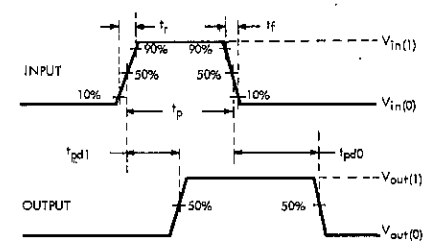
Dwg. No. A-9792A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	35	49	mA	1, 2



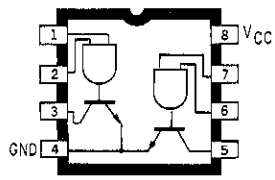
Dwg. No. A-7878D



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

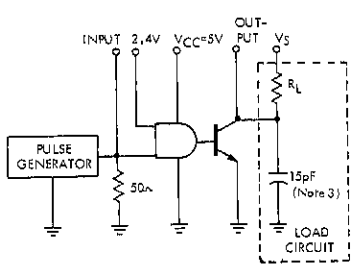
UDS-3612H
Dual NAND Driver



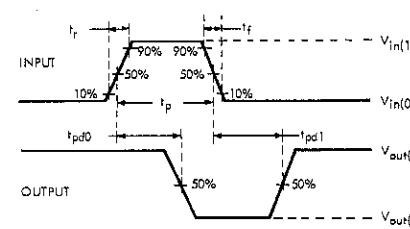
Dwg. No. A-9793A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	µA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	53	mA	1, 2



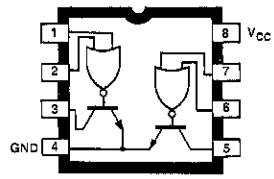
Dwg. No. A-9638



Dwg. No. A-7900A

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

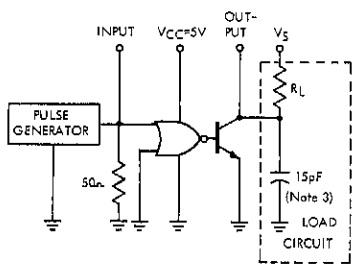
UDS-3613H
Dual OR Driver



Dwg. No. A-9795A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	36	50	mA	1, 2



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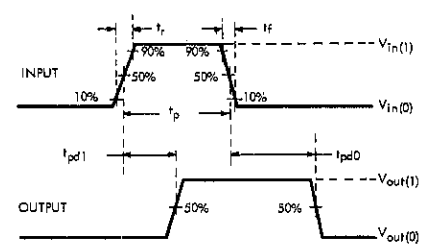
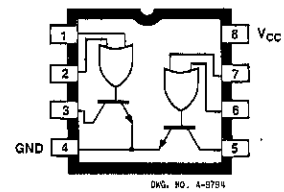


Dwg. No. A-7628C

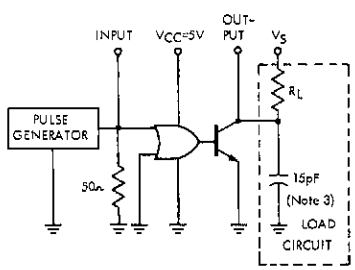
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

UDS-3614H
Dual NOR Driver



ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	µA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	50	mA	1, 2



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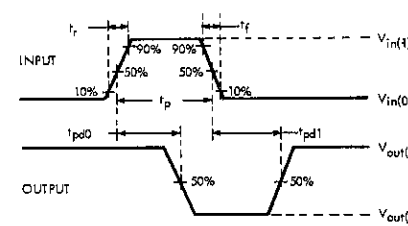


Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

6

UCS-4401H AND UCS-4801H
HERMETIC BiMOS LATCHED DRIVERS
MIL-STD-883 Compliant

FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- High-Reliability Screening to MIL-STD-883, Class B

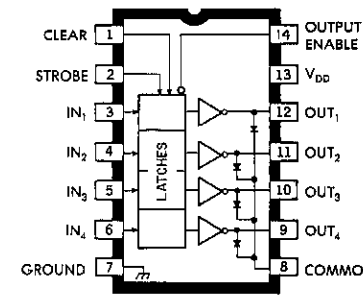
HIGH-VOLTAGE, HIGH-CURRENT interface for military, aerospace and related applications is supplied by these latched drivers. Type UCS-4401H contains four pairs of latches and drivers; Type UCS-4801H has eight pairs of latches and drivers.

The integrated circuits' CMOS inputs work with standard CMOS, PMOS and NMOS logic levels and (with appropriate pull-up resistors) with TTL or DTL circuits. The bipolar open-collector outputs can be used with relays, solenoids, motors, LED or incandescent displays, and other high-power loads.

The output transistors can sink 500 mA and will withstand a V_{CE} of 50 V in the OFF state. Outputs can be paralleled for higher current capability. Because of limitations on package power dissipation, simultaneous operation of all drivers at maximum rated current can only be accomplished with a reduction of duty cycle.

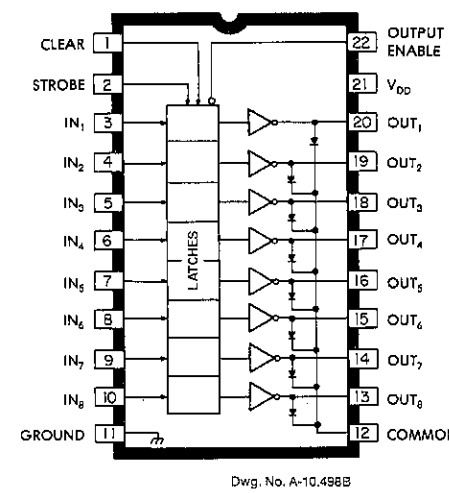
Type UCS-4401H, the four-latch device, is furnished in a standard 14-pin side-brazed hermetic package. Type UCS-4801H, the eight-latch device, is furnished in a 22-pin side-brazed hermetic package with row centers 0.400-inch (10.16 mm) apart.

Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.



Dwg. No. A-10,499B

UCS-4401H



Dwg. No. A-10,498B

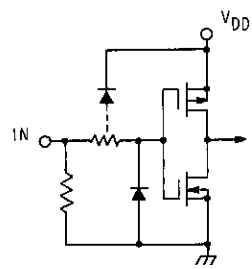
UCS-4801H

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 18 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . . $-55°C$ to $+125°C$
Storage Temperature Range, T_S . . . . . $-65°C$ to $+150°C$

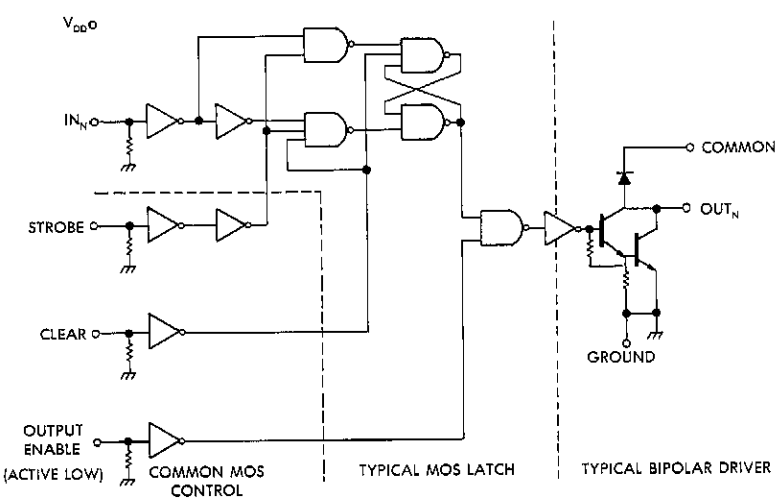
CAUTION: Sprague CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,520

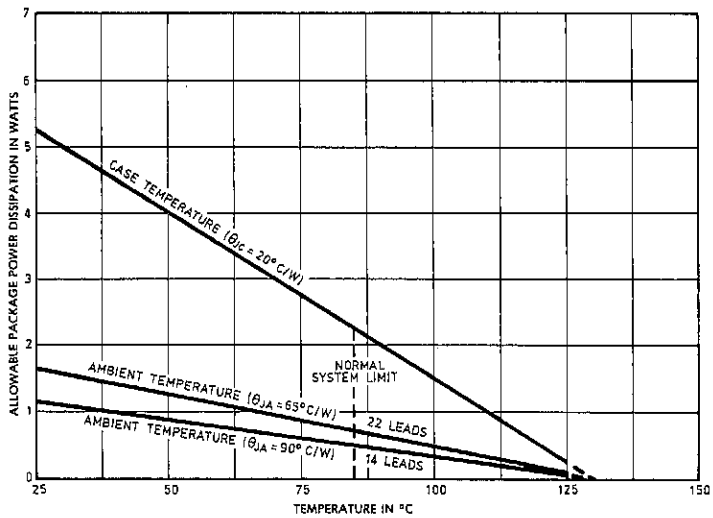
FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495B

6

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,464

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 15 V	13.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 15 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	V_{DD} = 15 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, V_{IN} = 0 V	—	50	100	µA
		All Drivers OFF, V_{IN} = 0 V, V_{DD} = 15 V	—	—	200	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	—	1.3	V
		$I_C = 200\ mA$	—	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15\ V$	14	—	—	V
		$V_{DD} = 10\ V$	9.0	—	—	V
		$V_{DD} = 5.0\ V$ (See note)	3.6	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15\ V$	35	—	—	kΩ
		$V_{DD} = 10\ V$	35	—	—	kΩ
		$V_{DD} = 5.0\ V$	35	—	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	$V_{DD} = 15\ V$, Outputs Open	—	1.0	2.5	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.9	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.2	mA
	$I_{DD(OFF)}$	All Drivers OFF, $V_{IN} = 0\ V$	—	50	100	μA
		All Drivers OFF, $V_{IN} = 0\ V$, $V_{DD} = 15\ V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	—	2.1	V

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

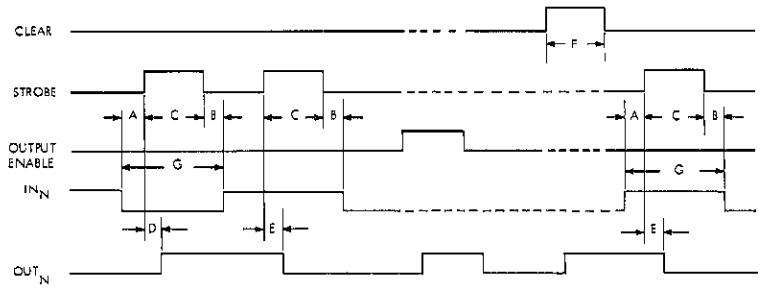
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$*	—	—	1.3	V
		$I_C = 200\ mA$*	—	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$*	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15\ V$	13.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$ (See note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15\ V$	50	—	—	kΩ
		$V_{DD} = 10\ V$	50	—	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	$V_{DD} = 15\ V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, $V_{IN} = 0\ V$	—	50	100	μA
		All Drivers OFF, $V_{IN} = 0\ V$, $V_{DD} = 15\ V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	—	500	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$*	—	—	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1"
*Pulsed test.

6

TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and Ground



Dwg. No. A-10,895A

A. Minimum data active time before strobe enabled (data set-up time) . . . . . 100 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 100 ns
C. Minimum strobe pulse width . . . . . 300 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

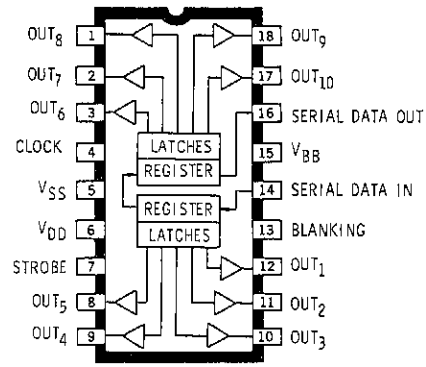
IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

UCS-4810H HERMETIC BiMOS
10-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg No A-10,988

COMBINING low-power CMOS logic with bipolar source drivers, Type UCS-4810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C at a duty cycle of 61%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications in this bulletin.

Type UCS-4810H, when combined with Type UCS-4815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. Type UCS-4801H is furnished in an 18-pin hermetic dual-in-line package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

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ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

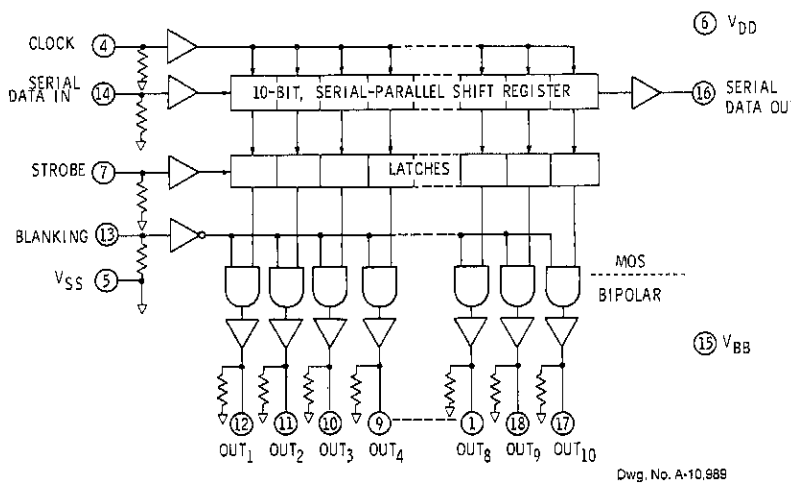
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 1.4 W*
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at 13.3 mW/°C above +25°C.

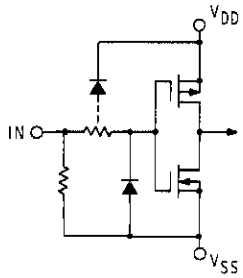
Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
10	81%	61%	34%
9	90%	68%	38%
8	98%	76%	43%
7	100%	87%	49%
6	100%	97%	57%
5	100%	100%	69%
4	100%	100%	86%
3	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM

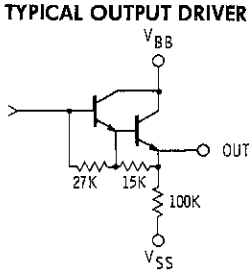


TYPICAL INPUT CIRCUIT



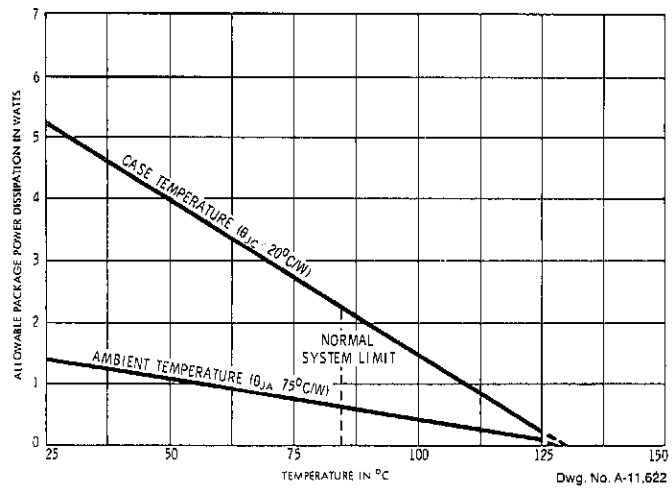
Dwg. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981B

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,622

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 15 V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 15 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 15$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	1400	μA
Output Leakage Current			—	−30	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 15 V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	27	kΩ
		V_{DD} = 15 V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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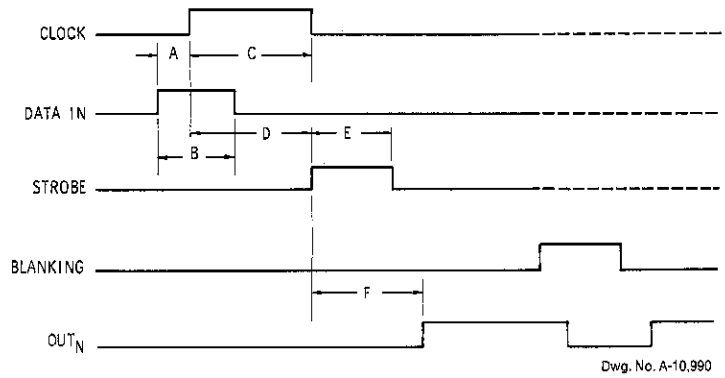


Dwg. No. A-10,990

TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and V_{SS}

	V_{DD} = 5.0 V	V_{DD} = 15 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

UCS-4810H TRUTH TABLE

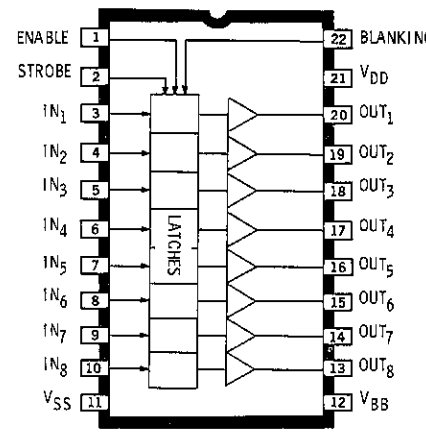
Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Blanking Input	Output Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$
H	↑	$H\ R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
L	↑	$L\ R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
X	↓	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$	R_{10}				
		X X X ..... X X X	X	L	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$		
		$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	P_{10}	H	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	L	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$
					X X X ..... X X X	H	L L L ..... L L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCS-4815H
HERMETIC BiMOS LATCH/SOURCE DRIVER
MIL-STD-883 Compliant

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCS-4815H BiMOS integrated circuit has eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply-voltage range of 5 V to 15 V. When employed with either standard TTL or low-speed TTL, UCS-4815H may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 89%. Other combinations of numbers of conducting outputs and duty cycle are shown in the specifications in this bulletin.

A minimum component display subsystem, requiring few or no discrete components, may be assembled by using a UCS-4815H BiMOS latch/source driver with a UCS-4810H serial-to-parallel latch/driver.

The UCS-4815H is furnished in 22-pin hermetic dual-in-line packages. To simplify printed wiring board layout, output pins on the package are opposite respective input pins.

Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

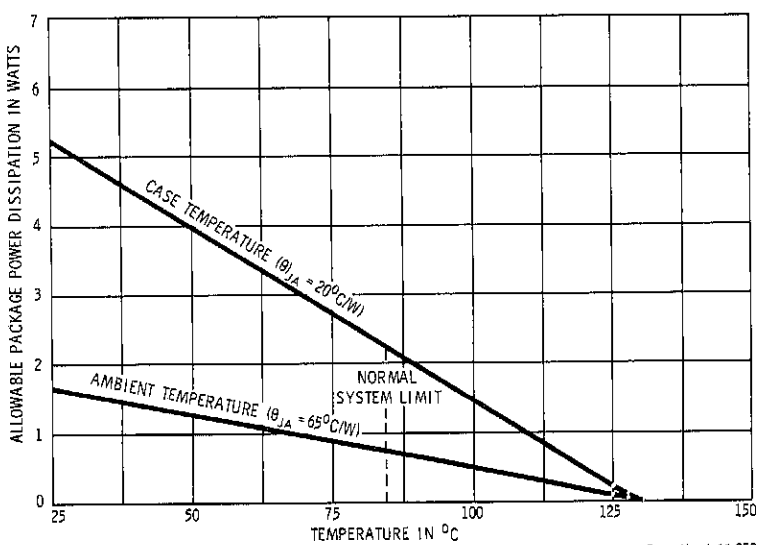
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 1.6 W*
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at 15.4 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	100%	89%	56%
7	100%	98%	57%
6	100%	100%	66%
5	100%	100%	80%
4	100%	100%	100%

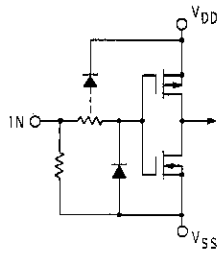
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



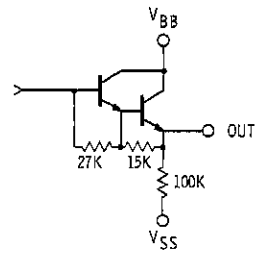
Dwg. No. A-11,652

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{BB} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

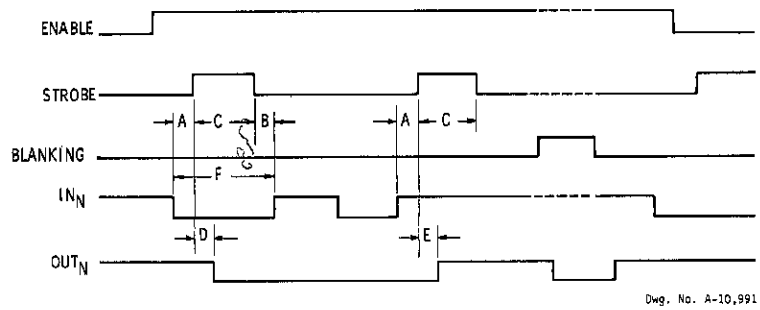
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	1400	μA
Output Leakage Current			—	−30	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 15 V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	12	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and V_{SS}

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Typical Strobe Pulse Width For Power-Up Clear Disable ..... 500 ns
Minimum Strobe Pulse Width After Power-Up Clear Disabled ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 500 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

On first applying V_{DD} to the device, all latch outputs assume a low state (Power-Up Clear) resulting in all outputs being OFF. The latches will remain in the low condition until the Clear is disabled by a STROBE high input. Data may be entered into the latches during Power-Up Clear disable if the ENABLE input is also high.

UCS-4815H TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

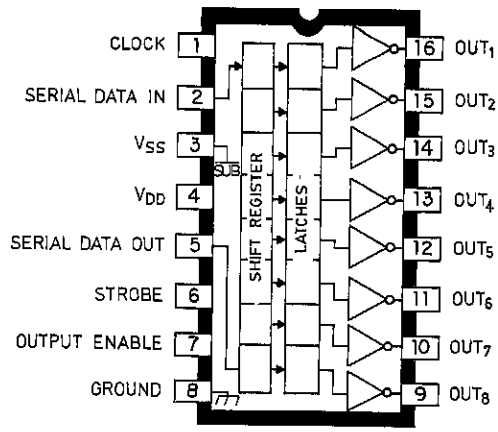
X = irrelevant
T-1 = previous output state
T = present output state

SERIES UCS-4820H HERMETIC BiMOS 8-BIT, SERIAL-INPUT, LATCHED DRIVERS

MIL-STD-883 Compliant

FEATURES

- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



Dwg. No. A-11,388B

INTENDED FOR MILITARY, aerospace, and related applications, Series UCS-4820H 8-bit, serial-input, latched drivers combine bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Except for the maximum allowable driver output-voltage ratings, Types UCS-4821H (50 V), UCS-4822H (80 V), and UCS-4823H (100 V) are identical.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output allows cascading these devices for interface applications requiring additional drive lines.

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

Series UCS-4820H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, class B are standard.

6

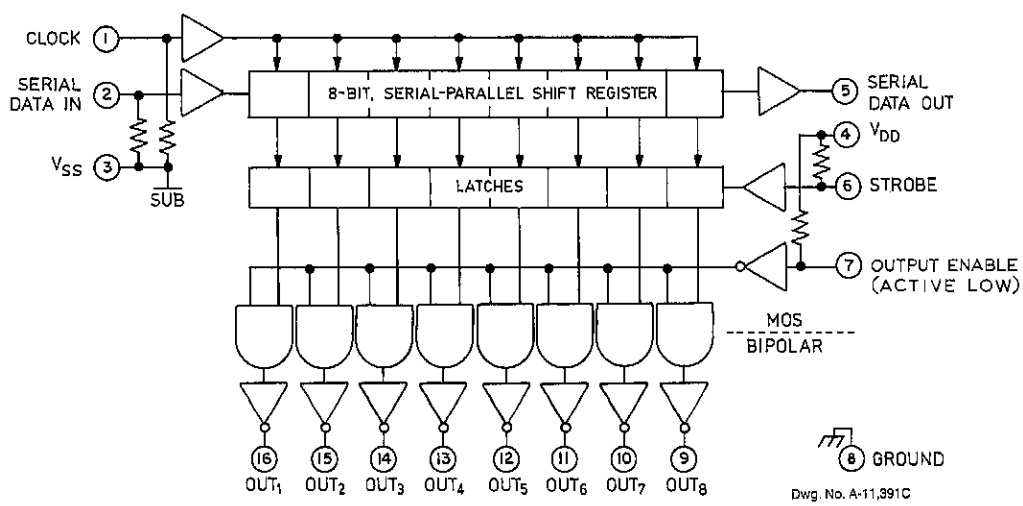
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCS-4821H) ..... 50 V
(UCS-4822H) ..... 80 V
(UCS-4823H) ..... 100 V
Logic Supply Voltage, V_{DD} ..... 18 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 500 mA
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

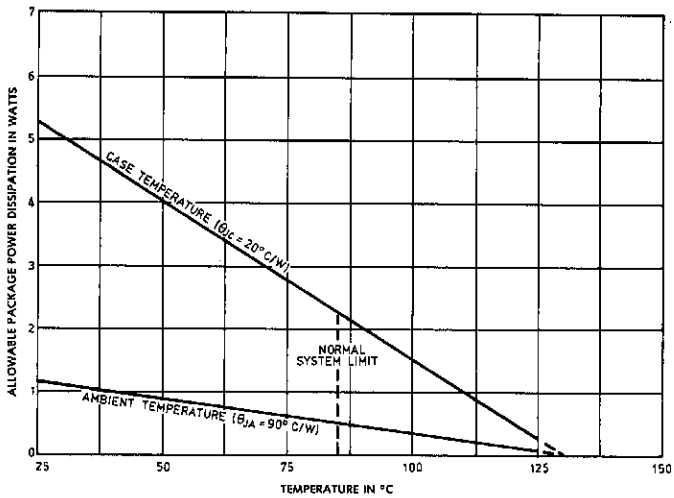
Number of Outputs ON (I_{OUT} = 200 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3	100%	100%	50%
2	100%	100%	75%
1	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,677

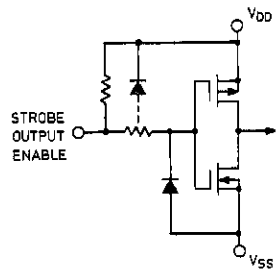
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	V_{OUT} = 50 V	—	50	µA
		UCS-4822H	V_{OUT} = 80 V	—	50	µA
		UCS-4823H	V_{OUT} = 100 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 15 V	13.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 15 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, V_{STROBE} = V_{DD} = 15 V	—	2.0	mA
			One driver ON, V_{STROBE} = V_{DD} = 10 V	—	1.7	mA
			One driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	1.0	mA
	$I_{DD(OFF)}$	ALL	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	100	µA
			V_{ENABLE} = V_{STROBE} = V_{DD} = 15 V	—	200	µA

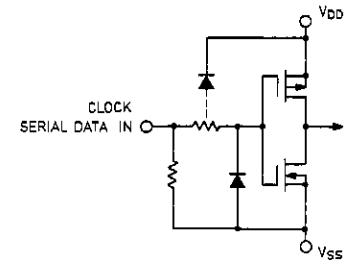
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

6

TYPICAL INPUT CIRCUITS



Dwg. No. A-12,658



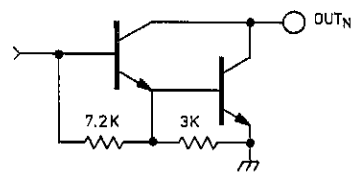
Dwg. No. A-12,659

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50\,V$	—	50	µA
		UCS-4822H	$V_{OUT} = 80\,V$	—	50	µA
		UCS-4823H	$V_{OUT} = 100\,V$	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\,mA$	—	1.3	V
			$I_{OUT} = 200\,mA$	—	1.5	V
			$I_{OUT} = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15\,V$	14	—	V
			$V_{DD} = 10\,V$	9.0	—	V
			$V_{DD} = 5.0\,V$ (See Note)	3.6	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15\,V$	35	—	kΩ
			$V_{DD} = 10\,V$	35	—	kΩ
			$V_{DD} = 5.0\,V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{STROBE} = V_{DD} = 15\,V$	—	2.5	mA
			One driver ON, $V_{STROBE} = V_{DD} = 10\,V$	—	1.9	mA
			One driver ON, $V_{STROBE} = V_{DD} = 5.0\,V$	—	1.2	mA
	$I_{DD(OFF)}$	ALL	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\,V$	—	100	µA
			$V_{ENABLE} = V_{STROBE} = V_{DD} = 15\,V$	—	200	µA

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

TYPICAL OUTPUT DRIVER



Dwg. No. A-11,390A

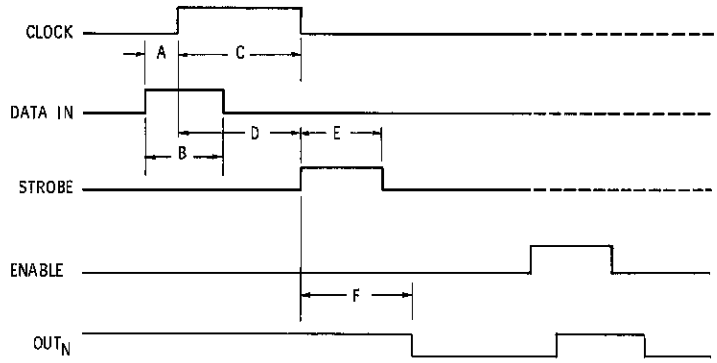
ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50\ V$	—	500	µA
		UCS-4822H	$V_{OUT} = 80\ V$	—	500	µA
		UCS-4823H	$V_{OUT} = 100\ V$	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\ mA$*	—	1.3	V
			$I_{OUT} = 200\ mA$*	—	1.5	V
			$I_{OUT} = 350\ mA$*, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15\ V$	13.5	—	V
			$V_{DD} = 10\ V$	8.5	—	V
			$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15\ V$	50	—	kΩ
			$V_{DD} = 10\ V$	50	—	kΩ
			$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{STROBE} = V_{DD} = 15\ V$	—	2.0	mA
			One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	1.7	mA
			One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	1.0	mA
	$I_{DD(OFF)}$	ALL	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	100	µA
			$V_{ENABLE} = V_{STROBE} = V_{DD} = 15\ V$	—	200	µA

*Pulsed test.

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

6



Dwg. No. A-10,990B

TIMING CONDITIONS

(T_A = +25°C; Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V	V_{DD} = 15 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCS-4820H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_8$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_8$	Output Enable	Output Contents $I_1\ I_2\ I_3 \ldots I_8$
H	↑	H R_1 R_2 ..... R_7	R_7				
L	↑	L R_1 R_2 ..... R_7	R_7				
X	↓	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

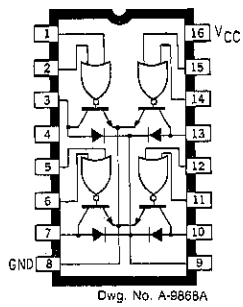
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

SERIES UDS-5700H QUAD 2-INPUT PERIPHERAL/POWER DRIVERS

MIL-STD-883 Compliant

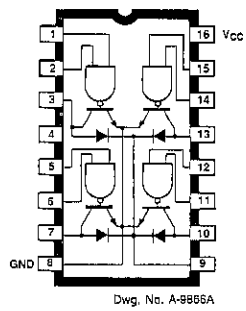
FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Hermetically Sealed Package to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



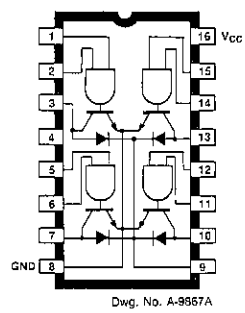
Dwg. No. A-9866A

UDS-5703H



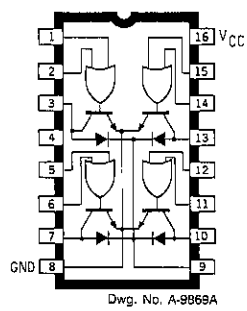
Dwg. No. A-9866A

UDS-5706H



Dwg. No. A-9867A

UDS-5707H



Dwg. No. A-9869A

UDS-5733H

THESE 16-LEAD QUAD 2-input peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, and NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 150 mA continuously at an ambient temperature of +70°C. In the OFF state, these drivers will withstand at least 80 V. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

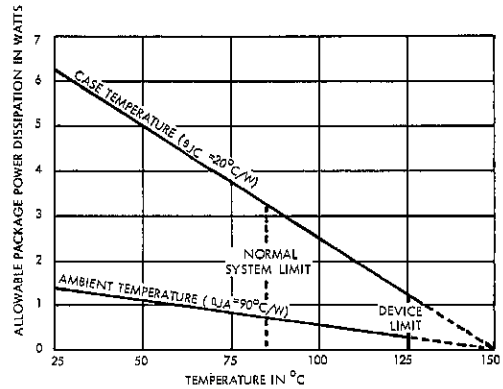
The Series UDS-5700H quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. For non-inductive loads, the diode common bus can be used as a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Suppression Diode Off-State Voltage, V_{OFF}	80 V
Suppression Diode On-State Current, I_{ON}	600 mA
Power Dissipation, P_D	1.0 W
Package Power Dissipation, P_D	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,198A

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

		Test Conditions			Limits				
Characteristic	Symbol	V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{IN(1)}$	Min.	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"1" Input Current	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
Input Clamp Voltage	V_i	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0$ V

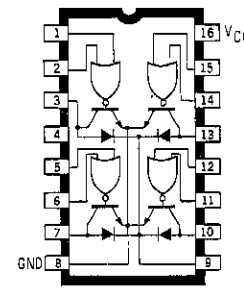
			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	$V_S = 70$ V, $R_L = 465\ \Omega$ (10 Watts) $C_L = 15$ pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	$V_S = 70$ V, $R_L = 465\ \Omega$ (10 Watts) $C_L = 15$ pF	—	300	750	ns	3

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)} = 0$ V	$t_r \leq 7$ ns	$t_p = 1\ \mu s$
$V_{IN(1)} = 3.5$ V	$t_r \leq 14$ ns	PRR = 500 kHz

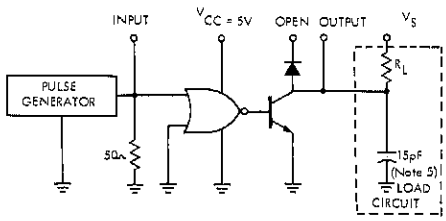
UDS-5703H QUAD OR DRIVER



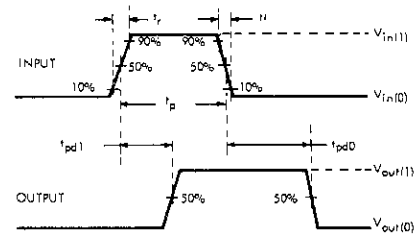
Dwg. No. A-9869A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	μA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	72	100	mA	1, 2



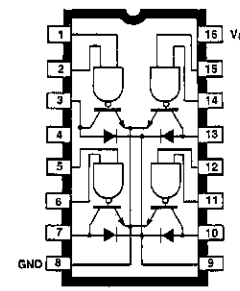
Dwg. No. A-9123A



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

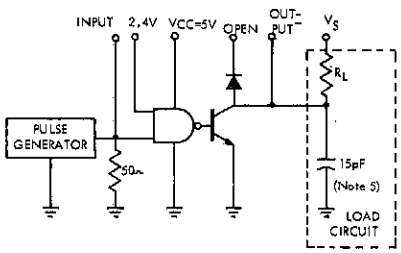
UDS-5706H QUAD AND DRIVER



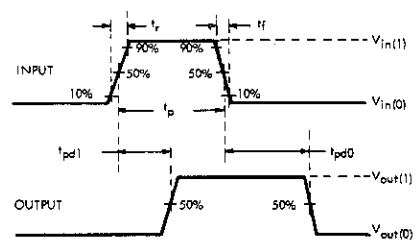
Dwg. No. A-9866A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	70	98	mA	1, 2



Dwg. No. A-7878A

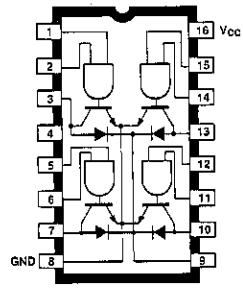


Dwg. No. A-7628C

NOTES:

1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

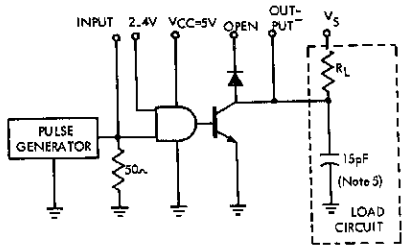
UDS-5707H QUAD NAND DRIVER



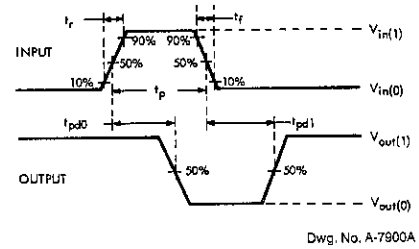
Dwg. No. A-9867A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	µA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	80	106	mA	1, 2



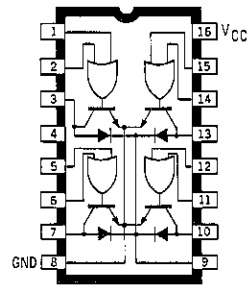
Dwg. No. A-7899A



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

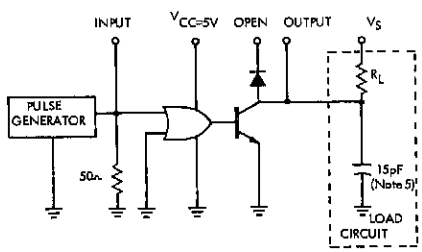
UDS-5733H QUAD NOR DRIVER



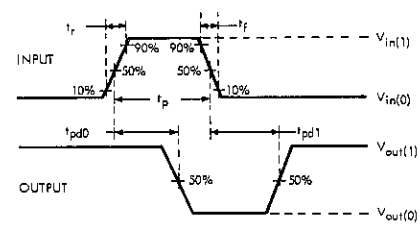
Dwg. No. A-9868A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	µA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	80	100	mA	1, 2



Dwg. No. A-9135A



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDS-5710H
DUAL PERIPHERAL/POWER DRIVERS

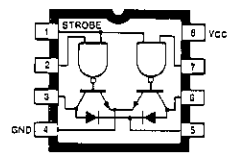
FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Transient Protected Outputs
- High-Reliability Screening

THESE DUAL peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 200 mA continuously at ambient temperatures of up to +85°C. In the OFF state, these drivers will withstand at least 80 V. Units are supplied in 8-pin hermetically-sealed mini-DIP packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883 are standard.

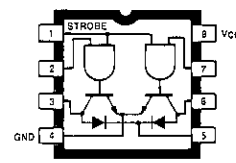
The Series UDS-5710H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to a 500 mA peak value.

The integral transient suppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function. Similar devices with four drivers per package are the Series UDS-5700H.



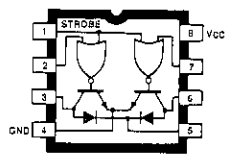
Dwg. No. A-9791B

UDS-5711H
Dual AND Driver



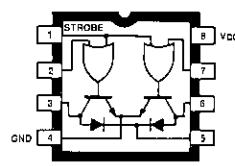
Dwg. No. A-9790B

UDS-5712H
Dual NAND Driver



Dwg. No. A-9789B

UDS-5713H
Dual OR Driver



Dwg. No. A-9788B

UDS-5714H
Dual NOR Driver

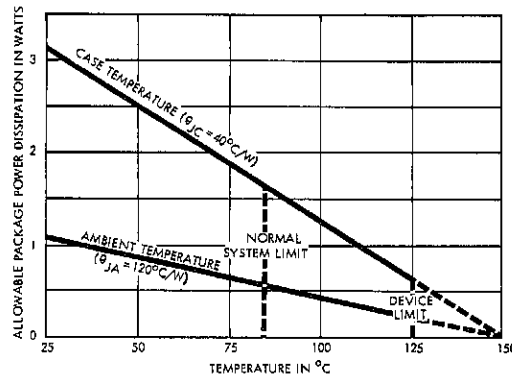
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{In}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	500 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	500 mA
Power Dissipation, P_D (one output)	1.0 W
(total package)	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

These devices are NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.

6

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,978

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions			Limits				Notes
		V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	Min.		—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.		—	—	—	0.8	V	—
"0" Input Current at all Inputs except Strobe	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"0" Input Current at Strobe	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−100	−200	μA	—
"1" Input Current at all Inputs except Strobe	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
"1" Input Current at Strobe	$I_{IN(1)}$	Max.	30 V	0 V	—	—	20	μA	2
Input Clamp Voltage	V_I	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

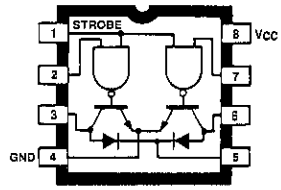
Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	T_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_r \leq$ 7 ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	$t_r \leq$ 14 ns	PRR = 500 kHz

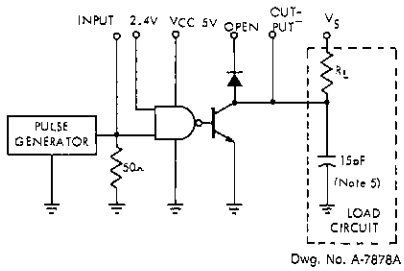
UDS-5711H DUAL AND DRIVER



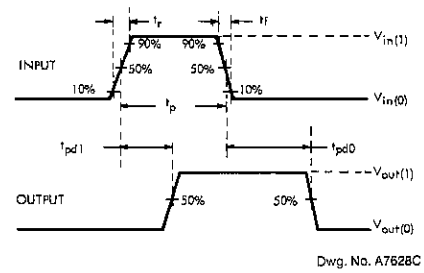
Dwg. No. A-9791B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	μA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	35	49	mA	1, 2



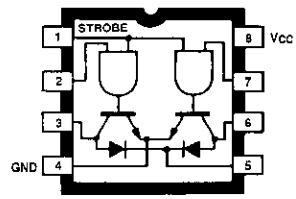
Dwg. No. A-7878A



Dwg. No. A7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

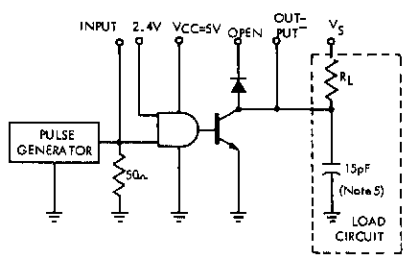
UDS-5712H DUAL NAND DRIVER



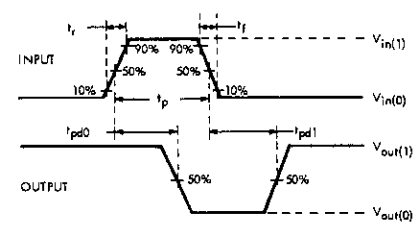
Dwg. No. A-9790B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	µA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	53	mA	1, 2



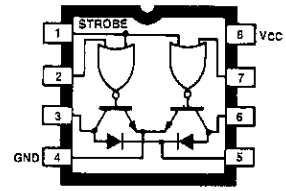
Dwg. No. A-7809A



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

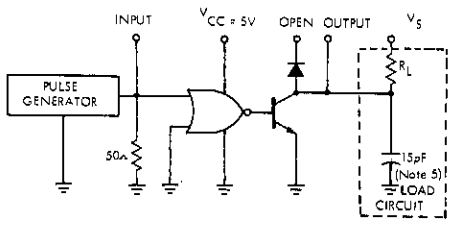
UDS-5713H DUAL OR DRIVER



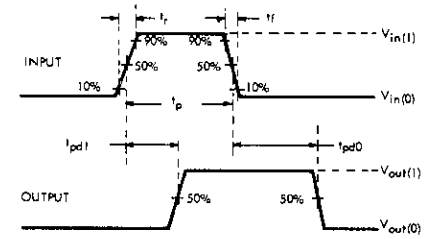
Dwg. No. A-9789B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	36	50	mA	1, 2



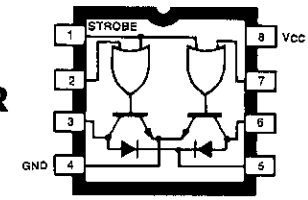
Dwg. No. A-9123A



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

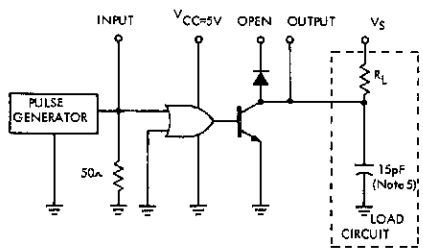
UDS-5714H DUAL NOR DRIVER



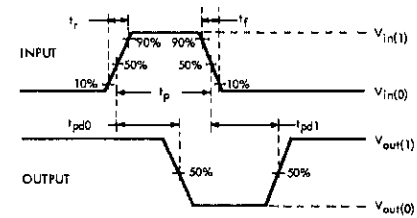
Dwg. No. A-9788B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	µA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	50	mA	1, 2



Dwg. No. A-9135A



Dwg. No. A-7900A

NOTES:

1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5791H
QUAD PIN DIODE POWER DRIVER
MIL-STD-883 Compliant

FEATURES

- Low Input Current
- TTL, DTL, MOS Compatible
- Wide Operating Voltage Range
- High Output Breakdown Voltage
- High-Reliability Screening to MIL-STD-883, Class B

CONSISTING of four high-voltage NPN output stages and associated logic and level shifting, this monolithic, planar integrated circuit offers an easy solution to many PIN diode driving applications.

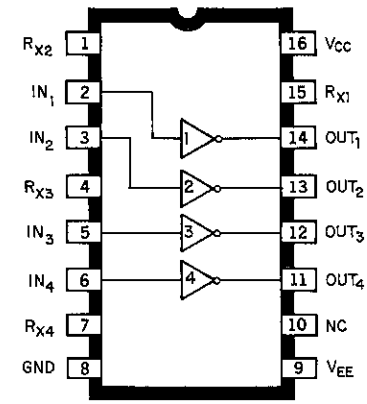
The UDS-5791H quad power driver is designed to replace discrete or hybrid PIN diode drivers. It provides significant reductions in cost and space with improved reliability. The device is capable of sustaining OFF voltages of 120 V and will switch currents to 500 mA.

The input buffer circuitry has been designed to utilize external discrete resistors. The one-resistor-per-driver effectively reduces total package power dissipation and junction temperature while allowing user selection of output base drive current, power supply voltages, and output current.

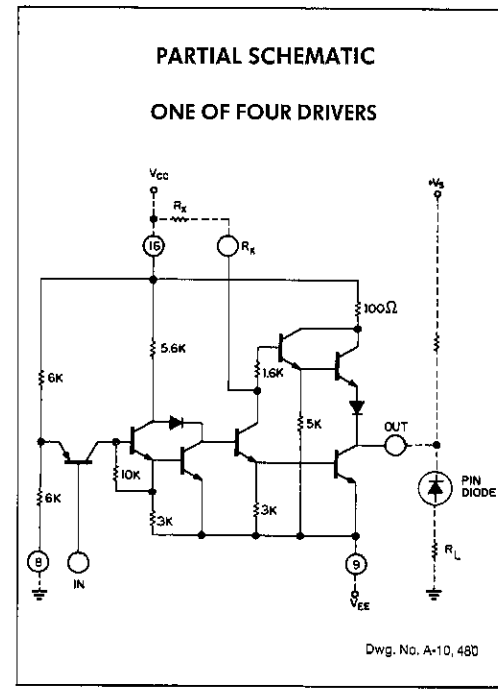
All devices are rated for operation over an extended temperature range of −55°C to +125°C. It is customarily supplied in 16-pin hermetic dual in-line packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
over free-air operating temperature range

Supply Voltage, V_{CC} . . . . . +6.0 V
Supply Voltage, V_{EE} . . . . . −6.0 V
Input Voltage, V_{IN} . . . . . V_{CC}
Output OFF-State Voltage, V_{OFF} (ref. V_{EE}) . . . . . +120 V
Output ON-State Current, I_{ON} . . . . . 500 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Ambient Temperature Range, T_A . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C



Dwg. No. A-10,478



Dwg. No. A-10,480

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RECOMMENDED OPERATING CONDITIONS

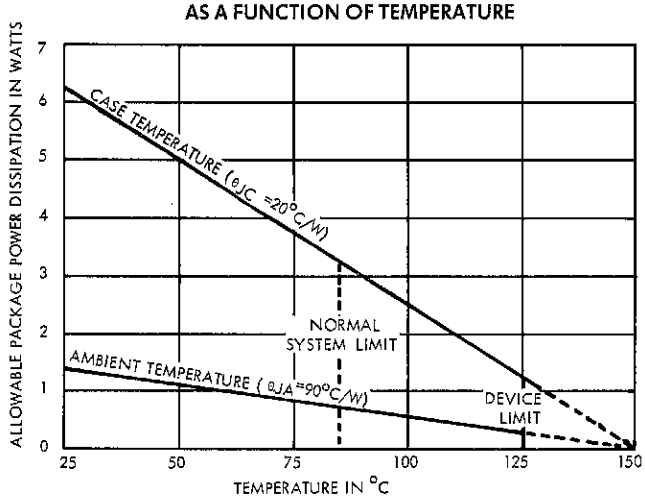
	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
Supply Voltage, V_{EE}	−1.5	−3.0	−5.5	V
Output ON-State Current, I_{ON}			300	mA
Operating Ambient Temperature Range, T_A	−55	+25	+125	°C

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp. (°C)	V_{CC} (+V)	V_{EE} (−V)	V_{IN} (+V)	V_{OFF} (+V)	or I_{ON} (mA)	R_X (Ω)	Limits Min.	Max.	Units
"1" Input Voltage	$V_{IN(1)}$	—	4.5	—	—	—	—	—	2.0	4.0	V
"0" Input Voltage	$V_{IN(0)}$	—	4.5	—	—	—	—	—	—	0.8	V
"1" Input Current	$I_{IN(1)}$	—	5.5	3.0	5.0	—	—	—	—	50	μA
"0" Input Current	$I_{IN(0)}$	—	5.5	3.0	0.4	—	—	—	—	1.0	mA
OFF-State Reverse Current	I_{OFF}	+25	4.5	3.0	0.4	115	—	—	—	50	μA
		+125	4.5	3.0	0.4	115	—	—	—	100	μA
ON-State Output Voltage* (Ref. V_{EE})	V_{ON}	−55	4.5	1.5	2.4	—	150	720	—	400	mV
						—	300	360	—	600	mV
		+25	4.5	1.5	2.4	—	150	720	—	400	mV
						—	300	360	—	700	mV
		+125	4.5	1.5	2.4	—	150	720	—	500	mV
						—	300	360	—	850	mV
Predriver Collector Voltage* (Ref. V_{EE})	V_X	—	4.5	1.5	2.4	—	150	720	—	1.3	V
						—	300	360	—	1.5	V
			5.5	3.3	2.4	—	300	270	—	1.7	V
Output Short-Circuit Current*	I_{OS}	—	4.5	3.0	0.4	−2.3	—	510	20	50	mA
OFF-State Supply Current	I_{CC}	—	5.5	5.5	0.4	—	—	—	—	4.1	mA
ON-State Supply Current	I_{CC}	—	5.5	5.5	2.4	—	—	—	—	3.4	mA
Turn-On Delay	t_{on}	+25	5.0	3.0	—	—	—	510	—	500	ns
Storage Delay	t_s	+25	5.0	3.0	—	—	—	510	—	5.0	μs
Fall Time	t_f	+25	5.0	3.0	—	—	—	510	—	100	ns

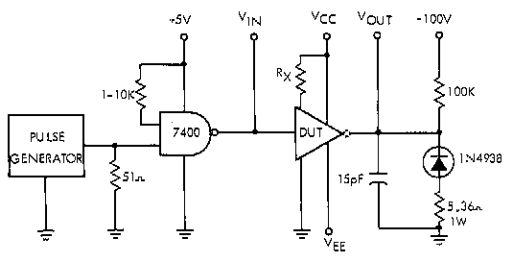
*Each output tested separately.

ALLOWABLE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

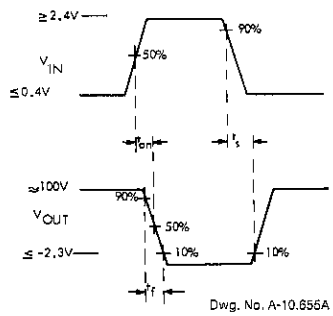


Dwg. No. A-10,198A

SWITCHING TEST CIRCUIT
AND WAVEFORMS



Dwg. No. A-10 654



Dwg. No. A-10,656A

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GENERAL DESIGN NOTES

$$I_{RX} = \frac{I_{ON}}{B} \qquad R_X = \frac{B(V_{CC} - V_{EE} - V_X)}{I_{ON}}$$

where:

B = 30, the minimum output current gain over the operating temperature range

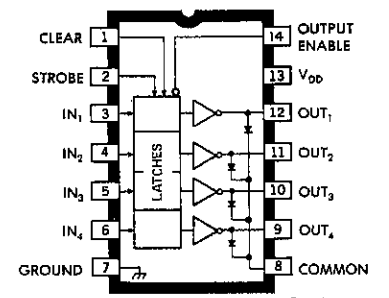
V_x = 1.5, the maximum predriver voltage

It is recommended that a minimum overdrive of 25% to be used (1.25 I_{RX} or 0.8R_X).

UCS-5800H AND UCS-5801H
HERMETIC BiMOS II LATCHED DRIVERS
MIL-STD-883 Compliant

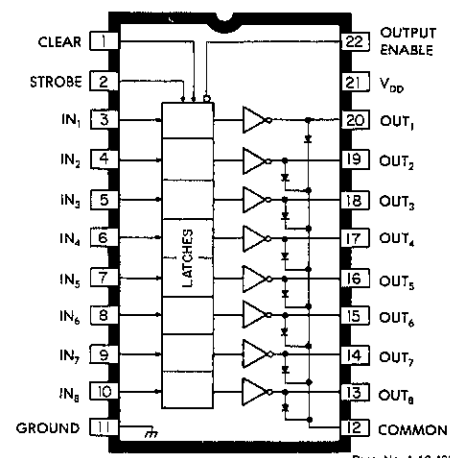
FEATURES

- 4.4 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Control and Latches
- High-Voltage, High-Current Outputs
- Transient-Protected Outputs
- Operating Temperature −55°C to +125°C
- High-Reliability Screening to MIL-STD-883, Class B



UCS-5800H

Dwg. No. A-10,499B



UCS-5801H

Dwg. No. A-10,498B

SIMPLIFYING INTERFACE between LSI and peripheral power loads, the hermetically sealed UCS-5800H (4-bit) and UCS-5801H (8-bit) latched drivers combine the advantages of CMOS logic and control and high-voltage, high-current bipolar output buffers. Typical applications include microprocessor interface to relays, solenoids, dc and stepper motors, printers, LED or incandescent displays requiring hermetic packaging and an operating temperature range of −55°C to +125°C.

BiMOS II latched drivers have data input rates faster than those of the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The Darlington open-collector outputs will drive power loads rated to 50 V and 350 mA (500 mA, maximum). Integral diodes for inductive load transient suppression are included. Because of limitations on package power dissipation, the simultaneous operation of all drivers at high current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load-current capability.

The 4-bit, UCS-5800H is furnished in a standard 14-pin side-brazed hermetic package. The 8-bit, UCS-5801H is supplied in a 22-pin side-brazed hermetic package with row spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs. Both packages conform to the dimensional requirements of MIL-M-38510. High-temperature reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

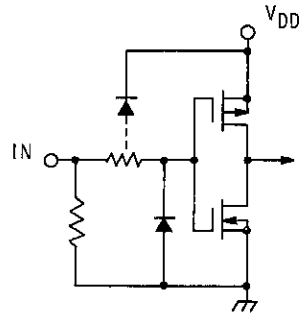
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, air flow, and number of outputs conducting. Under any set of conditions, do not exceed a maximum junction temperature of +130°C.

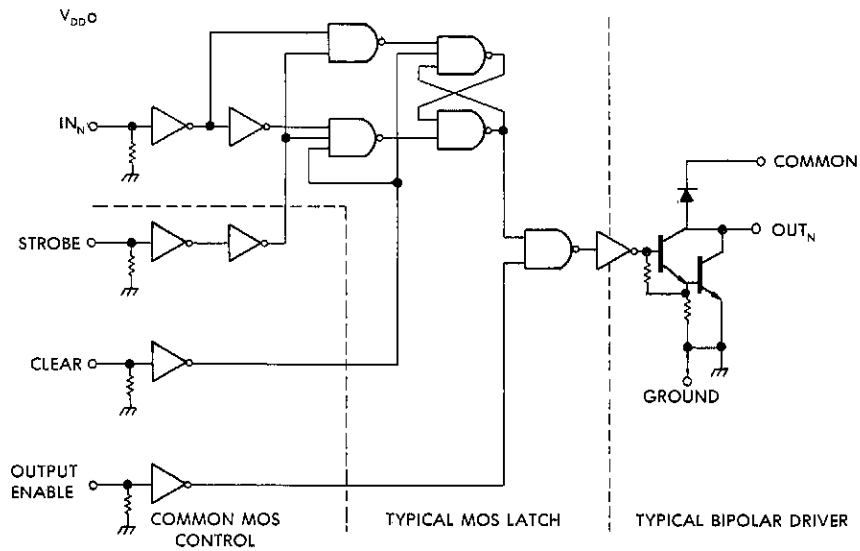
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,520

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495A

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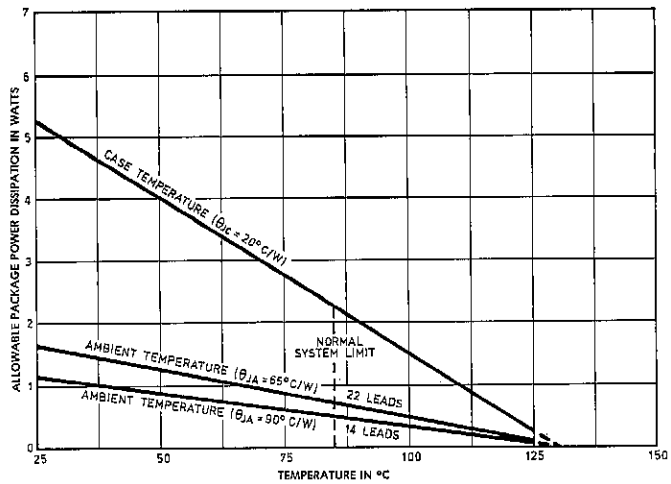
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,464

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.1	V
		I_C = 200 mA	—	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

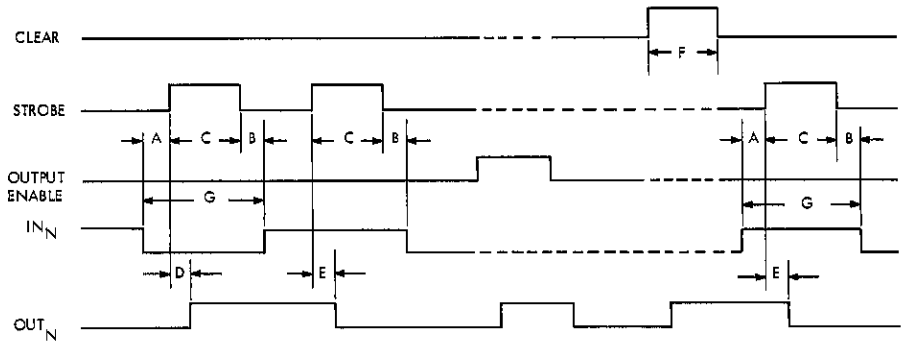
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	1.3	V
		$I_C = 200\ mA$	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	11	—	V
		$V_{DD} = 10\ V$	9.0	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.6	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	35	—	kΩ
		$V_{DD} = 10\ V$	35	—	kΩ
		$V_{DD} = 5.0\ V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	2.5	mA
		$V_{DD} = 10\ V$, Outputs Open	—	1.9	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	2.1	V

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	1.3	V
		$I_C = 200\ mA$	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 10\ V$	8.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	—	kΩ
		$V_{DD} = 10\ V$	50	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."

6



Dwg. No. A-10,895A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) . . . . . 50 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 50 ns
C. Minimum strobe pulse width . . . . . 125 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 225 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

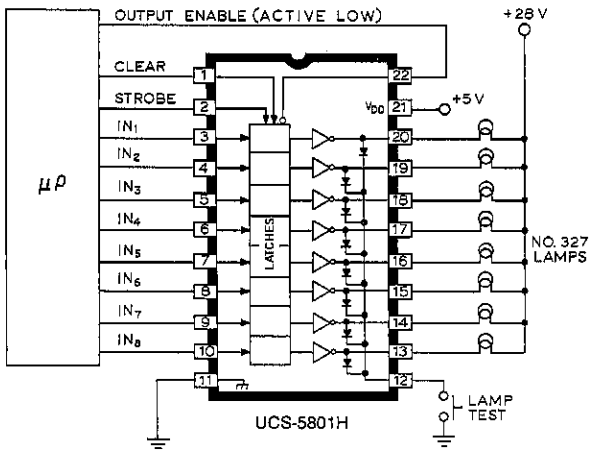
TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

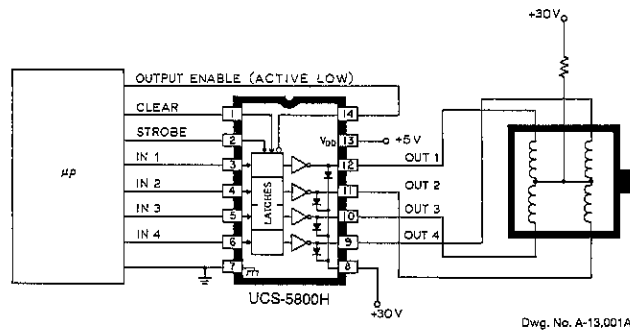
TYPICAL APPLICATIONS

INCANDESCENT LAMP DRIVER

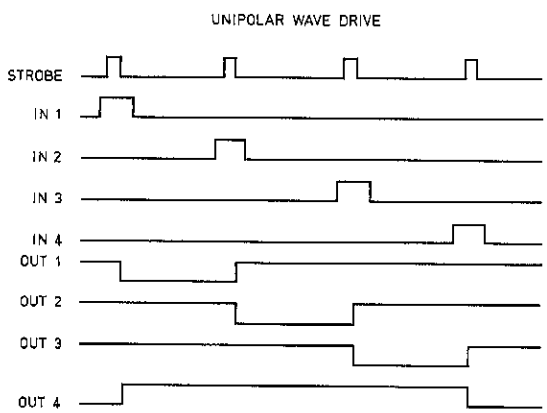


Dwg. No. A-13,000A

UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. No. A-13,001A



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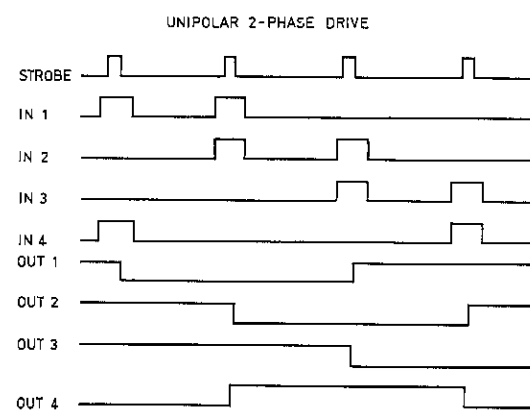


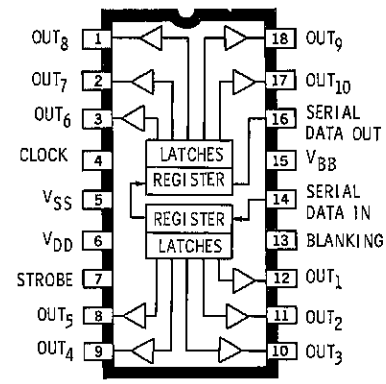
Dwg. No. A-11,447

6

UCS-5810H HERMETIC BiMOS II
10-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

FEATURES

- 5 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,888

COMBINING low-power CMOS logic with bipolar source drivers, Type UCS-5810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C at a duty cycle of 61%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications in this bulletin.

Type UCS-5810H, when combined with Type UCS-5815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. Type UCS-5810H is furnished in an 18-pin hermetic dual-in-line package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

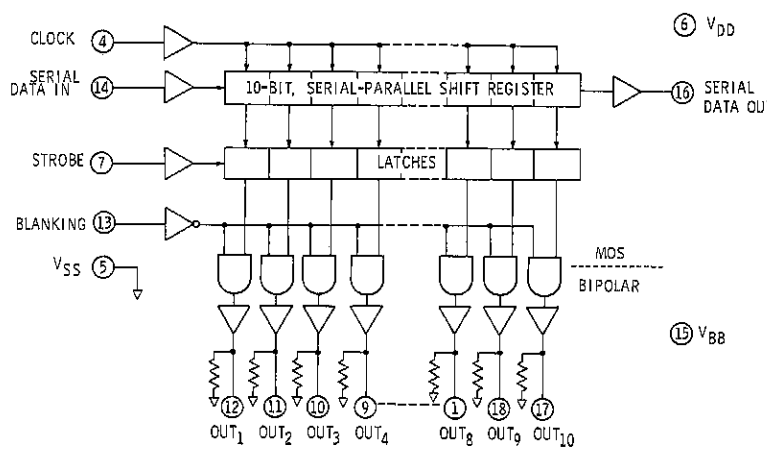
Output Voltage, V_{OUT} . . . . . 60 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Ouput Current, I_{OUT} . . . . . −40 mA
Package Power Dissipation, P_D . . . . . 1.4 W*
Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

*Derate at 13.3 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
10	81%	61%	34%
9	90%	68%	38%
8	98%	76%	43%
7	100%	87%	49%
6	100%	97%	57%
5	100%	100%	69%
4	100%	100%	86%
3	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

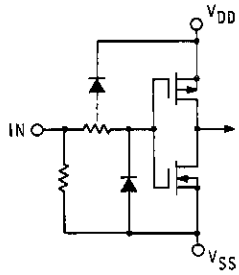
FUNCTIONAL BLOCK DIAGRAM



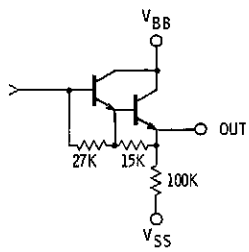
Dwg. No. A-10,989

6

TYPICAL INPUT CIRCUIT



TYPICAL OUTPUT DRIVER



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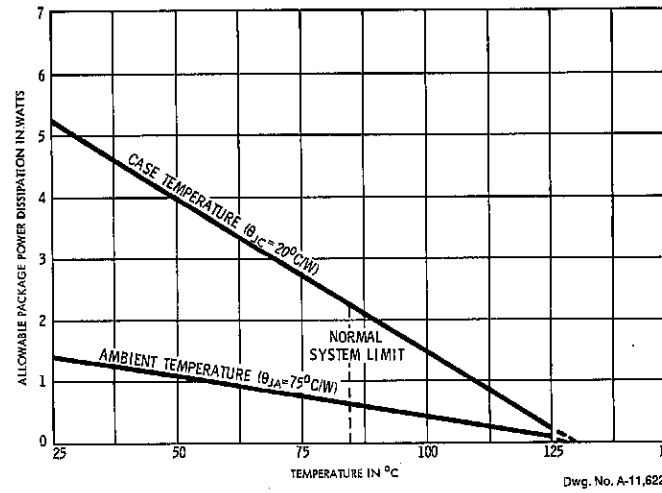
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,622

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 12$ V	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
		$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	200	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

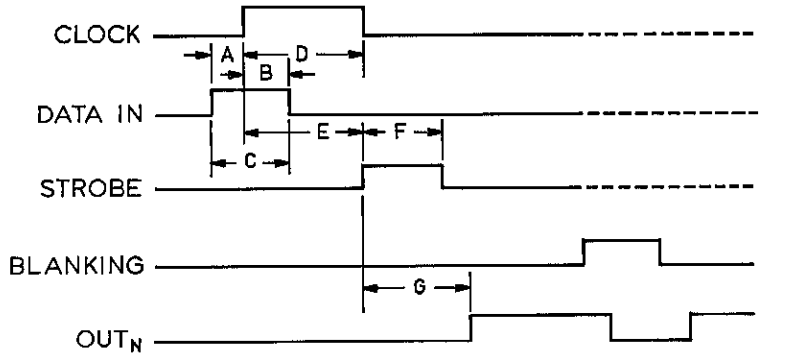
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 12$ V	11.0	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	µA
		$V_{DD} = V_{IN} = 12$ V	—	430	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	−30	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 12$ V	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
		$V_{DD} = V_{IN} = 12$ V	—	300	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	27	kΩ
		$V_{DD} = 12$ V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-12,649

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

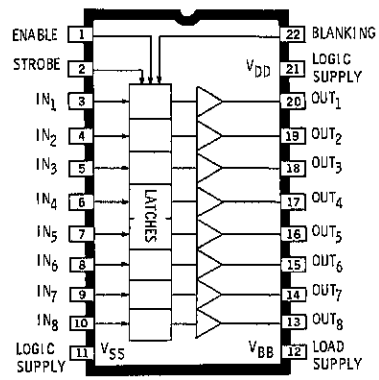
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H		$H\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L		$L\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X		$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCS-5815H
HERMETIC BiMOS II LATCH/SOURCE DRIVER
MIL-STD-883 Compliant

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,987A

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCS-5815H BiMos integrated circuit has eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 12 V. When employed with either standard TTL or low-speed TTL UCS-5815H may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 89%. Other combinations of numbers of conducting outputs and duty cycle are shown in the specifications in this bulletin.

A minimum component display subsystem, requiring few or no discrete components, may be assembled by using a UCS-5815H BiMOS latch/source driver with a UCS-5810H serial-to-parallel latch/driver.

The UCS-5815H is furnished in 22-pin hermetic dual-in-line packages. To simplify printed wiring board layout, output pins on the package are opposite respective input pins.

Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

6

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

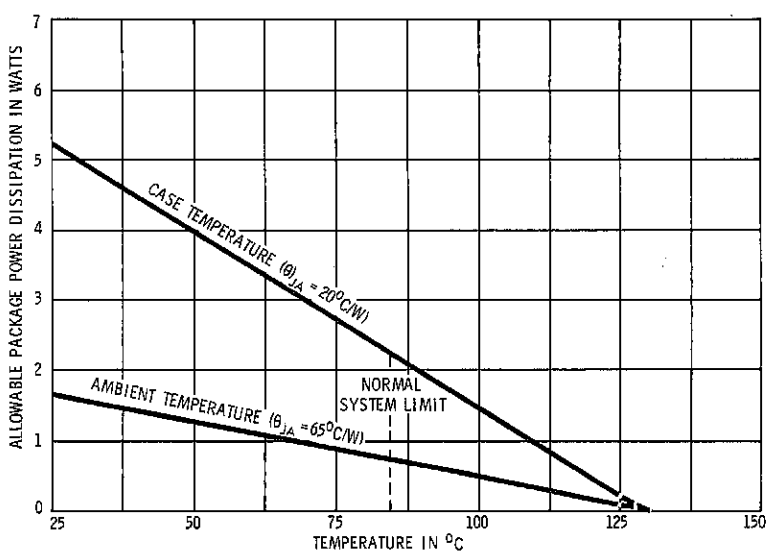
Output Voltage, V_{OUT} . . . . . 60 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} . . . . . −40 mA
Package Power Dissipation, P_D . . . . . 1.6 W*
Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

*Derate at 15.4 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	100%	89%	56%
7	100%	98%	57%
6	100%	100%	66%
5	100%	100%	80%
4	100%	100%	100%

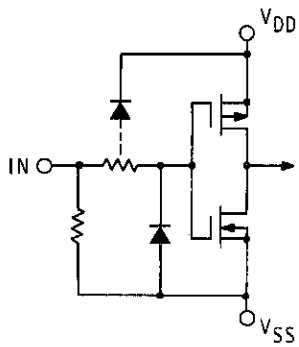
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



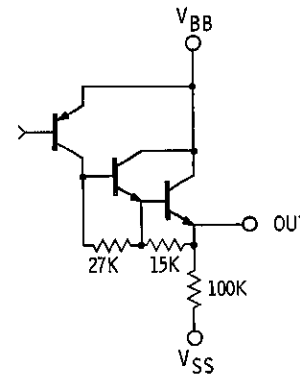
Dwg. No. A-11,652

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,546

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
		$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All Outputs open	—	10.5	mA
		All outputs OFF, All Outputs open	—	200	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

6

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60\,V$, $V_{DD} = 5\,V$ to $12\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

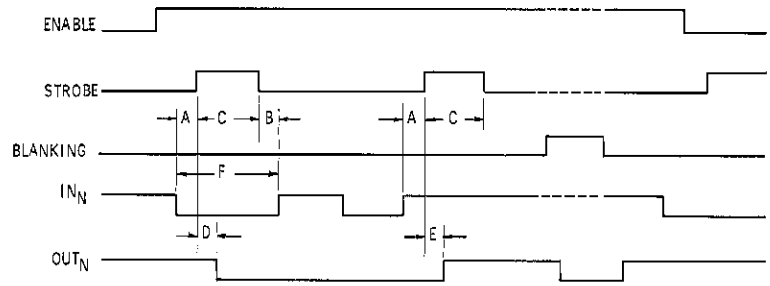
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 12$ V	11.0	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	µA
		$V_{DD} = V_{IN} = 12$ V	—	430	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60\,V$, $V_{DD} = 5\,V$ to $12\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	−30	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 12$ V	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
		$V_{DD} = V_{IN} = 12$ V	—	300	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	12	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-10,991

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active time After Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	125 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F. Minimum Data Pulse Width	225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz, minimum data input rate (50% duty cycle) with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

UCS-5815H TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

6

UCS-5822H HERMETIC BiMOS II
8-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

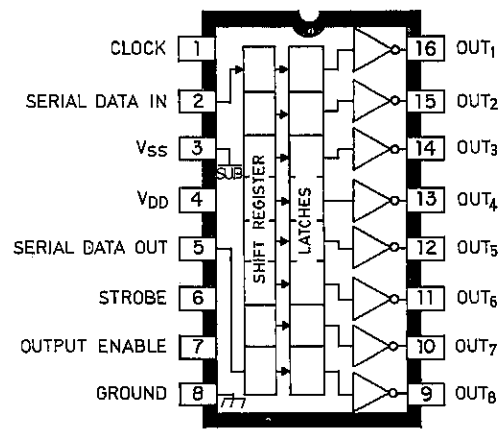
FEATURES

- 3.3 MHz Minimum Data Input Rate
- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Intended for military, aerospace, and related applications. The UCS-5822H 8-bit, serial-input, latched driver combines bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output alows cascading these devices for interface applications requiring additional drive lines.



Dwg. No. A-11,388B

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

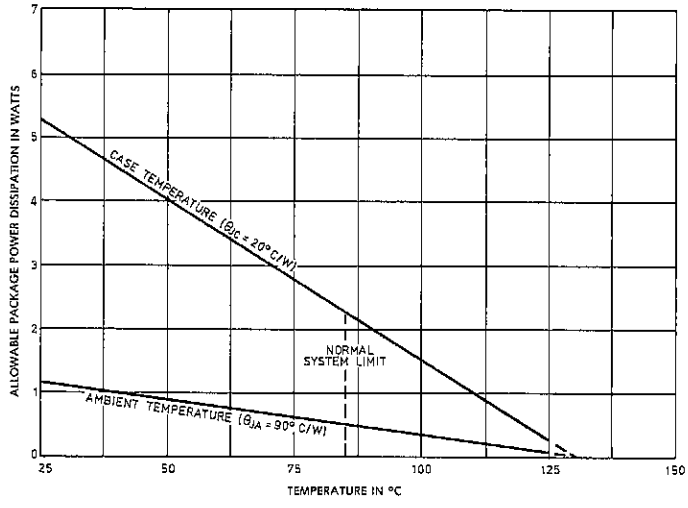
The UCS-5822H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, class B are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT}	80 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

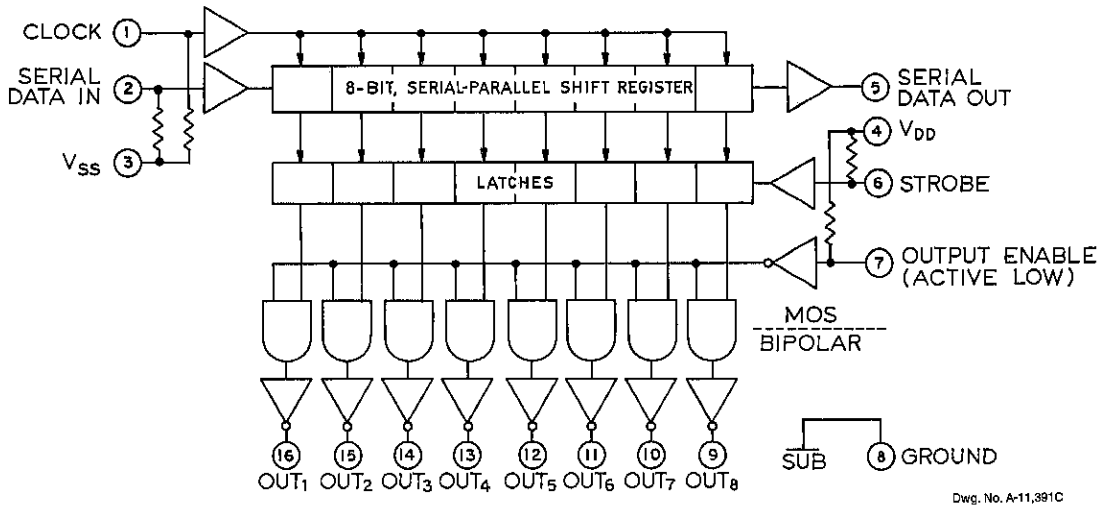
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,677

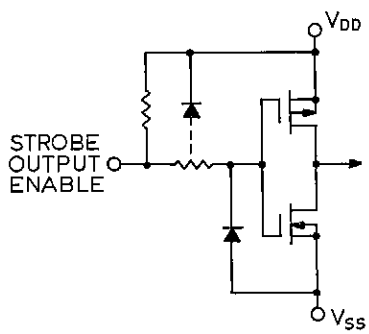
6

FUNCTIONAL BLOCK DIAGRAM

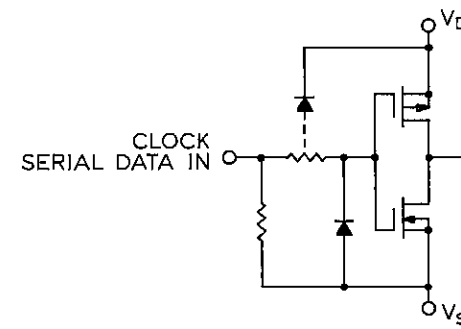


Dwg. No. A-11,391C

TYPICAL INPUT CIRCUITS

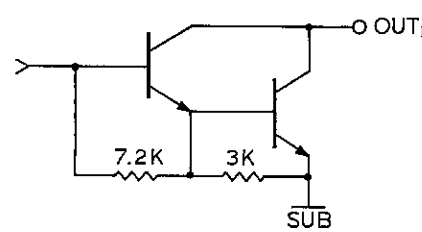


Dwg. No. A-12,658



Dwg. No. A-12,659

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,229

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\ V$	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\ mA$	—	1.1	V
		$I_{OUT} = 200\ mA$	—	1.3	V
		$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	—	kΩ
		$V_{DD} = 10\ V$	50	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\ V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	3.9	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\ V$	—	2.9	mA

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

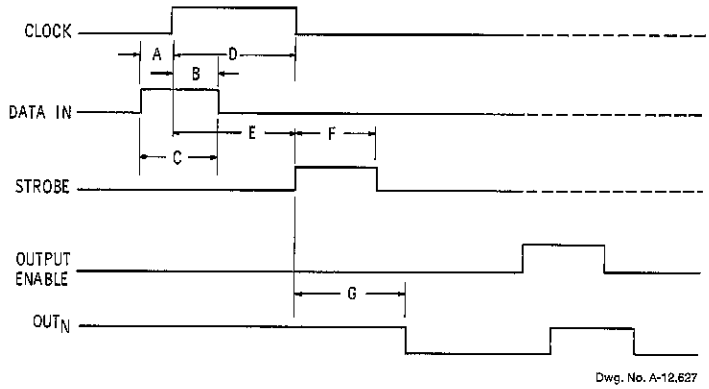
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\ V$	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\ mA$	—	1.3	V
		$I_{OUT} = 200\ mA$	—	1.5	V
		$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	35	—	kΩ
		$V_{DD} = 10\ V$	35	—	kΩ
		$V_{DD} = 5.0\ V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\ V$	—	5.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	3.0	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	2.0	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\ V$	—	3.5	mA

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA*	—	1.3	V
		I_{OUT} = 200 mA*	—	1.5	V
		I_{OUT} = 350 mA*, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, V_{STROBE} = V_{DD} = 12 V	—	4.5	mA
		One driver ON, V_{STROBE} = V_{DD} = 10 V	—	3.9	mA
		One driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	1.6	mA
		V_{ENABLE} = V_{STROBE} = V_{DD} = 12 V	—	2.9	mA

*Pulsed test.
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

Number of Outputs ON (I_{OUT} = 200 mA)	Max. Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3	100%	100%	50%
2	100%	100%	75%
1	100%	100%	100%



Dwg. No. A-12,627

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

6

UCS-5822H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H		H R_1 R_2 ..... R_7	R_7				
L		L R_1 R_2 ..... R_7	R_7				
X		R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

MIL-STD-883 CLASS B HIGH-RELIABILITY SCREENING

All full-temperature hermetic devices are produced on a production line that is JAN Class B certified and are processed to the production screen inspections and tests in accordance with the latest requirements of MIL-STD-883. Applicable devices are marked to indicate compliance to the latest revision (at time of manufacture) of MIL-STD-883. For example: UCS5822H-883.

100% Production and High Reliability Screen Tests MIL-STD-883, Method 5004, Class B

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Temperature Cycle	1010, Cond. C	—
Constant Acceleration	2001, Cond. E	30,000 Gs, Y1 Plane
Interim Electrical	5005, Gp A, Subgp. 1	25°C per Specification
Burn-In	1015, Cond. A.	125°C, 160 Hrs or 150°C, 80 Hrs
Static Electrical	5005, Gp A, Subgp. 1	25°C per Specification
	5005, Gp A, Subgp. 2 & 3	−55°C & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp. 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A_1	5×10^{-8} atm × cm³/s Max.
Gross Seal	1014, Cond. C	—
Marking	—	Sprague logo and part number, date code, lot identification, and ESD warning symbol when applicable.
External Visual	2009	—

Quality Conformance Inspection MIL-STD-883, Method 5005, Class B

Test	MIL-STD-883 Test Method	Description
Group A, Subgp. 1-4, 7 & 9	5005, Table I	Each Inspection Lot
Group B	5005, Table II	Alternate Gp. B on Weekly Basis
Group C	5005, Table III	End Points, Gp. A, Subgp. 1, as required
Group D	5005, Table IV	End Points, Gp. A, Subgp. 1, as required

NOTE: Devices using an 8-leaded side-brazed package are NON-COMPLIANT regarding MIL-STD-883. Military specification MIL-M-38510, case outline D-4, configuration 3 defines the package length as 0.405" (10.29 mm) maximum. Sprague Electric packages are 0.528" (13.41 mm) maximum. These devices (Series UDS-3610H and UDS-5710H) are therefore marked to indicate conformance only to MIL-STD-883B. For example: UDS-3611H-MIL.

BiMOS II POWER DRIVERS TO MIL-STD-883

BiMOS monolithic smart power drivers combine CMOS logic and control functions with bipolar and/or DMOS power drivers. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL, LSTTL, or DTL circuits may require appropriate pull-up resistors to ensure a logic high. The power driver outputs are used with VF, LED, and incandescent displays, dc and stepper motors, relays, solenoids, and thermal or electrosensitive print heads. With BiMOS integrated circuit, reliable, single-chip solutions are provided for a wide variety of peripheral power interface problems.

The high-current and high-voltage BiMOS drivers shown here are processed to MIL-STD-883. They furnish a higher level of interface flexibility and versatility for military, aerospace, avionics, than is provided with standard logic or discrete power drivers. They are supplied in ceramic/metal side-brazed hermetic packages (Sprague suffix letter 'H'). All devices are rated for operation over the full military temperature range of −55°C to +125°C.

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED DRIVERS

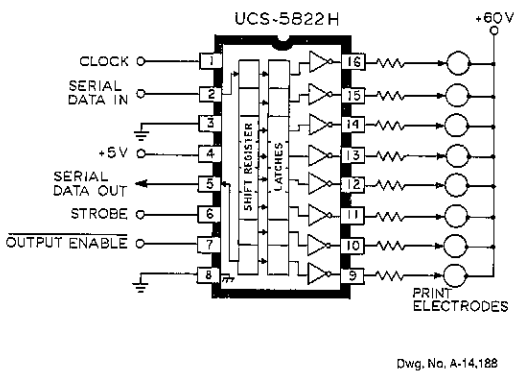
The UCS-5822H and UCS-5842H BiMOS 8-Bit Serial-In/Parallel-Out Latched Drivers augment the original UCS-4401H and UCS-4801H devices. Both of the devices contain an octal shift register, octal latch, and octal high-current, open-collector Darlington outputs. They improve systems designs through a reduced package count and a reduction in I/O line requirements. By using the serial data output, the drivers can be cascaded for interface applications requiring more than eight drive lines.

The bipolar outputs are suitable for a variety of peripheral loads, including incandescent lamps, LEDs, and thermal or electrosensitive printers. The UCS-5842H is recommended for relays, solenoids, and other high-power inductive loads.

RECOMMENDED MAX. OPERATING CONDITIONS

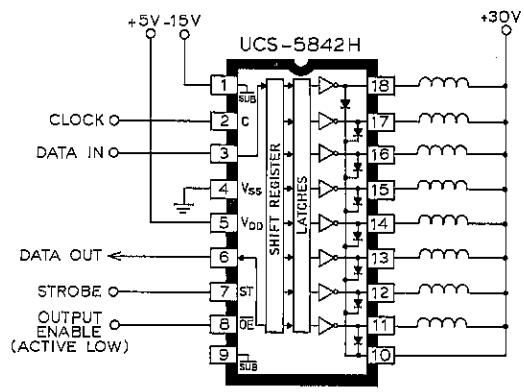
Output Sustaining Voltage (UCS-5842H)	50 V
Output Voltage	75 V
Logic Supply Voltage	12 V
Continuous Output Current	350 mA

ELECTROSENSITIVE PRINTER



Dwg. No. A-14,188

RELAY/SOLENOID DRIVER



Dwg. No. A-14,266

6

10-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED SOURCE DRIVER

The UCS-5810H BiMOS 10-Bit Serial-In/Parallel-Out Latched Source Driver is primarily designed as interface between logic circuitry and vacuum-fluorescent displays but may also be used with LED displays or thermal printers within its output limitations of 60 V and −40 mA per driver.

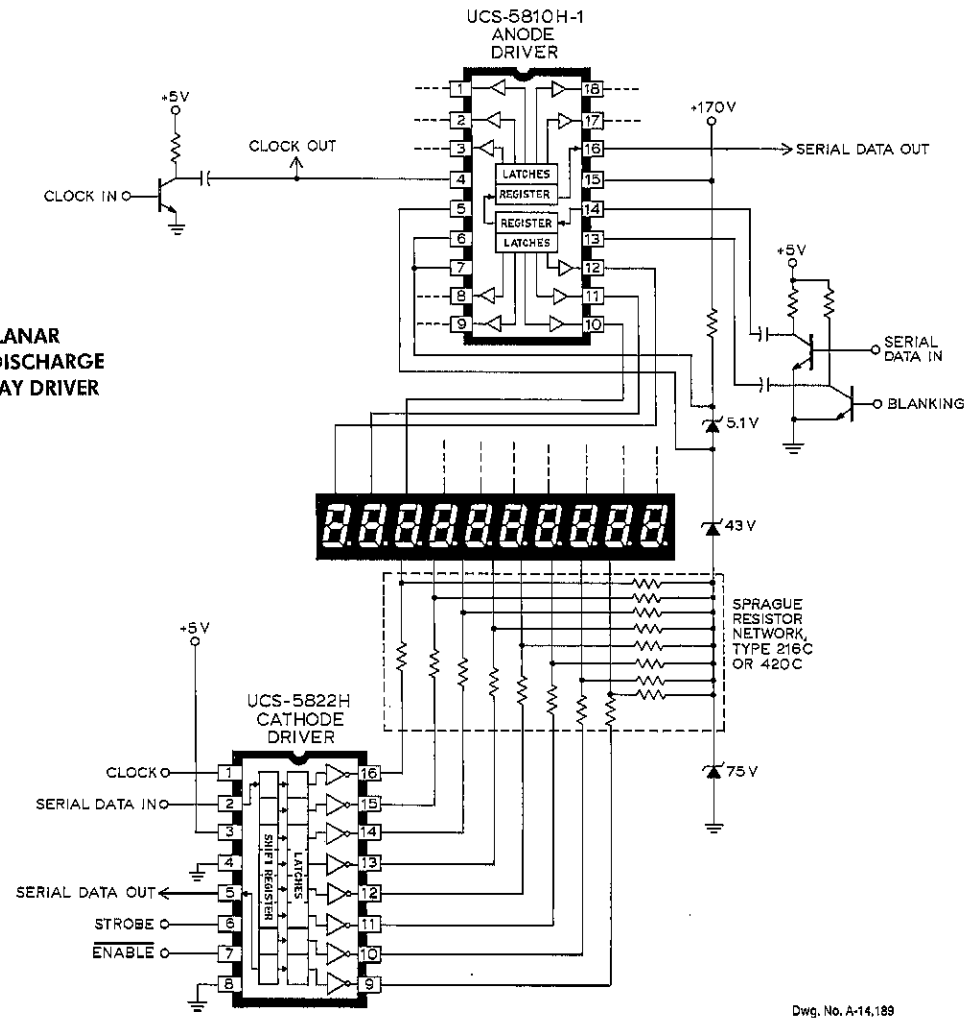
The CMOS shift register and latches will operate over a wide supply-voltage range and is compatible with standard MOS logic families. When used with TTL or low-speed TTL, pull-up resistors may be needed to ensure an input-logic high.

The 10 high-voltage outputs are used to switch the anodes (segments or dots) and/or grids (character or digit) of typical vacuum-fluorescent panels.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage ..... 55 V
Logic Supply Voltage Range..... 5.0 V to 12 V
Continuous Output Current ..... −25 mA

PLANAR GAS-DISCHARGE DISPLAY DRIVER



Dwg. No. A-14,189

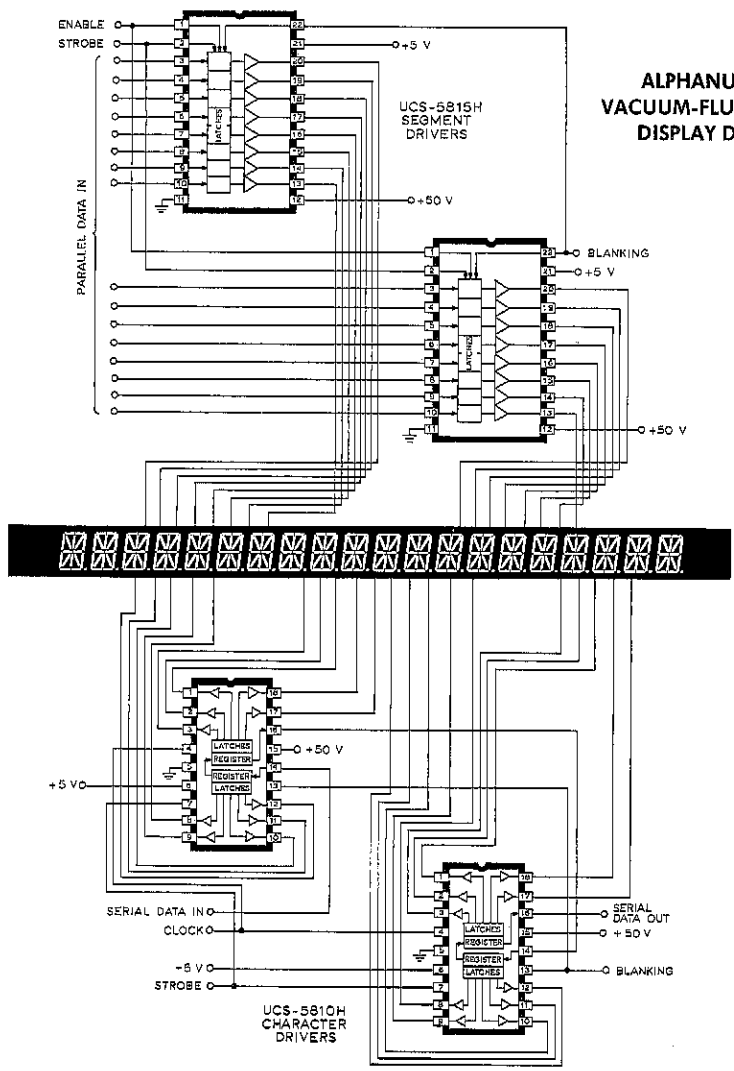
8-BIT LATCHED SOURCE DRIVER

The UCS-5815H BiMOS 8-Bit Latched Source Driver is designed primarily for use with high-voltage vacuum-fluorescent displays. It contains an 8-bit type D latch and eight source outputs with pull-down resistors, a common strobe, blanking, and enable functions.

The eight high-voltage outputs are generally used to drive the segments, dots (matrix panel), bars, or digits of vacuum-fluorescent displays. Type UCS-5815H is often used in combination with the Type UCS-5810H 10-Bit Serial Input, Latched Driver.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	55 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	−25 mA



Dwg. No. C-1272A

4- AND 8-BIT LATCHED DRIVERS

The UCS-5800H and UCS-5801H are evolutionary improvements to the original BiMOS integrated circuits. They are used successfully in many applications. These high-voltage, high-current latched drivers have four or eight MOS data latches, a bipolar driver for each latch, and MOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Type UCS-5800H contains four latched drivers while Type UCS-5801H contains eight latched drivers.

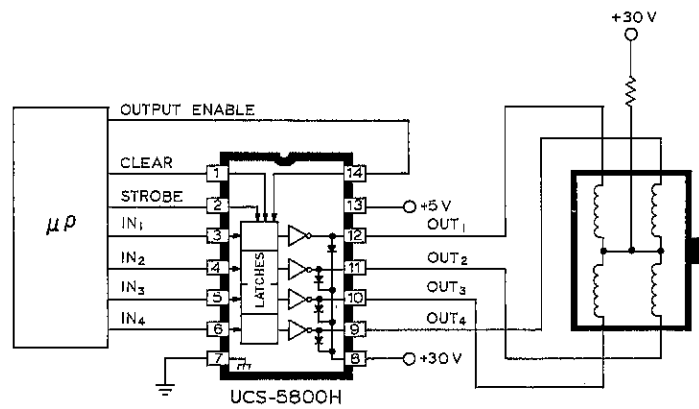
Each of the open-collector Darlington outputs can sink up to 500 mA and will sustain at least 50 V in the OFF state. Internal diodes suppress transients and allow these devices to be used with inductive loads. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current, and usually dictate either a reduction in output current or a suitable combination of duty cycle and number of active outputs.

The UCS-5800H is supplied in a standard 14-lead side-brazed hermetic package. The UCS-5801H is furnished in a 22-lead side-brazed hermetic package with lead centers on 0.400-inch spacing.

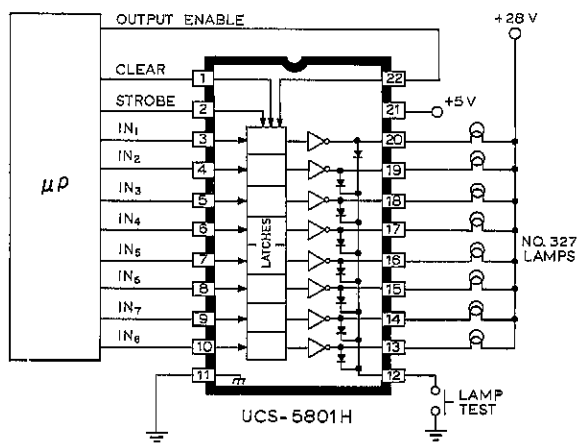
RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	45 V
Logic Supply Voltage	12 V
Continuous Output Current	350 mA

UNIPOLAR BIFILAR MOTOR DRIVE



Dwg. No. B-1491A



INCANDESCENT LAMP DRIVER

Dwg. No. A-11,743A

NOTES