AN-5013

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GTLP in BTL Applications

Abstract

Today's high performance systems require fast edge rates and smooth transitions with minimal ringing, overshoot/ undershoot, and other signal integrity issues. The Gunning Transceiver Logic Plus (GTLP) family offers a portfolio of translation devices and clock drivers that are not only capable of the fast HL/LH transitions demanded for high speed backplanes, but also feature a unique edge rate control characteristic that ensures smoother transitions. By tuning the backplane with proper termination resistors and reference voltage techniques, GTLP can act as a drop-in electrical solution for Backplane Transceiver Logic (BTL) as well as support high-speed backplane systems up to 125 MHz and beyond. GTLP's real advantages occur when the devices are operated at their recommended normal operating specifications. This application note illustrates the ability of GTLP to perform in existing BTL applications and evaluates GTLP port interface equivalence with most families.

Background

BTL and GTLP signaling can be seen as derivations of ECL/PECL signaling. Each of them addresses "open collector" or "open drain" control of a multi-drop signaling environment with the benefit of a pull-up termination for output high signal levels. The benefit of "open drain" technology is that the output is either sinking current or in high impedance state (3-STATE) but never sources current. It can also provide translation from TTL/LVTTL signaling.

The evolution from ECL to BTL to GTLP was an effort to solve power consumption problems in earlier applications while providing near-equivalent performance. ECL is a pure bipolar design and BTL designs are BiCMOS. GTLP was the first all CMOS solution and provides the most power savings of the two previous device designs.
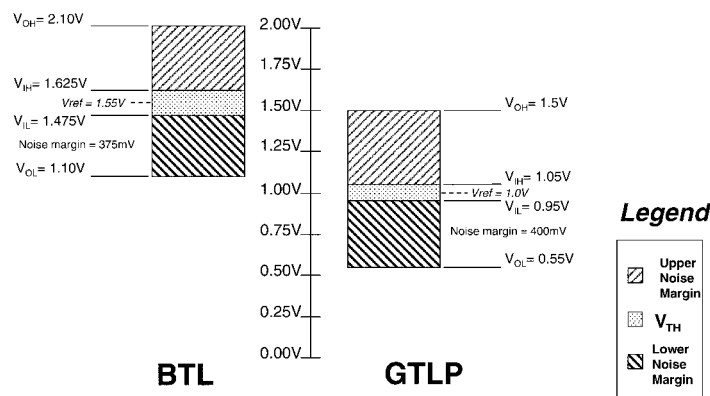
Compatibility

Because GTLP is an evolutionary step from the previous designs in BTL and ECL, it shares many of the conceptual features and performance characteristics that multi-drop applications require. Since the GTLP family provides bi-directional translation of LVTTL signal levels and GTLP signal levels, there are varied requirements when driving or receiving signals from either of its interface ports. Some of the desirable features of the GTLP port driver include high drive capability, low output impedance, controlled output edge rates and live insertion characteristics. It must also provide a completely different set of characteristics for the LVTTL driver interface such as medium drive levels, bushold and over-voltage tolerance.

Specifications

One of the noted differences between BTL and GTLP is the output and input signal. As depicted in Figure 1, BTL and GTLP differ in their drive and threshold levels. This may seem like a major design problem, when in fact GTLP can operate at the I/O levels specified by BTL. At these levels, the drive characteristics of two technologies look very compatible. The output I_{OL} characteristics of BTL and GTLP can be plotted together. The curves in Figure 2 show that GTLP has stronger drive at the critical low output voltage levels. The stronger drive will provide more noise margin for the GTLP devices.

FIGURE 1. Input/Output Signal Level Comparison
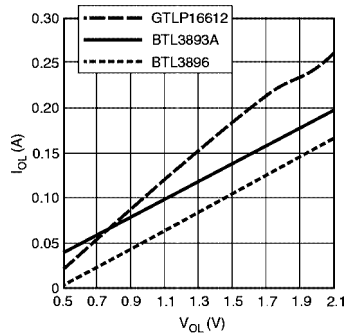
Specifications (Continued)

FIGURE 2. Output I_{OL} Characteristics

From a datasheet point of view, GTLP and BTL provide different reference from which they derive their specifications. BTL follows the standards set by various standards' bodies and its specifications are set by those. GTLP is more flexible in which standard it needs to set its specification. Initially GTLP followed an established specification set by Intel in their microprocessor interface designs. Intel set these specifications in an effort to optimize on-board signal integrity characteristics. However, off-board applications remain more "open" in nature, and the flexibility of the GTLP output allows it to interface to a number of interface signal levels.

Interface signals in today's high-speed systems often have to contend with edge rates becoming faster and refections, ringing, crosstalk, and ground bounce becoming more evident. Interface signal levels, through their noise margins, become important in ensuring system stability. GTLP devices, such as the GTLP6C816, offer comparable noise margins to its BTL predecessors. The combination of a 50mV threshold margin coupled with a wider V_{OL} noise margin means GTLP can operate within BTL signal level specifications. Figure 1 shows the lower noise margin to be 400mV for GTLP compared to 375mV for BTL.

Voltage Levels

BTL and GTLP both need a termination voltage (V_{TT}) that can be regulated directly from V_{CC}. GTLP uses a reference voltage pin (V_{REF}) which is an input threshold voltage used to reference an incoming BTL/GTLP signal. As a starting point for prototype designs, Fairchild recommends that V_{REF} be generated from V_{TT} with the use of a simple voltage-divider circuit. By tying V_{REF} to V_{TT}, at any point that a signal falls below the threshold region, incident wave switching can still be achieved by lowering the V_{TT} which consequently lowers V_{REF}. By centering the noise level between V_{REF} and V_{TT}, the maximum noise immunity can be maintained.

BTL generates V_{REF} internally and is set at 1.55V. GTLP uses an external V_{REF} pin, and it is recommended that it be set at 1.0V.

Throughput/Performance

Using GTLP at BTL voltage levels results in a maximum frequency similar to BTL of about 40 MHz. When used at the recommended voltage levels, however, GTLP's output control circuitry allows operation at frequencies exceeding 100 MHz.

By controlling the device's output edge rate, much less overshoot and undershoot characteristics are seen than with fast signal transitions in medium to high performance backplanes. The ability to set different rise and fall times compensates for various loads. Therefore the output edge rate control feature coupled with an adequate termination scheme allows the system designer to fine tune the output edge for optimum performance. Such features are found on the GTLP16T1655.

Proper termination of the system is important for optimizing performance. The backplane impedance will vary from system to system depending on stub lengths, number of slots, slot pitch, and types of connectors used. The recommended termination technique for GTLP is a Thevenin termination. This termination scheme uses two resistors in parallel, one at each end of the backplane. The resulting parallel value of the resistor equals half that of the transmission line. This type of termination reduces overshoot and improves the noise margin of the system, both of which are critical for incident wave operation.

Power Consumption

The output structure of GTLP is designed for a 50Ω termination tied at each end of the backplane. This parallel termination configuration is a 25Ω equivalent load. Single ended termination in a bi-directional backplane will result in non-incident wave switching which can cause signal integrity problems. With a 25Ω Thevenin equivalent load, the static current demand with GTLP is 34 mA. Since BTL typically has load impedances of 19.5Ω (39Ω/2 for parallel termination), the I_{OL} is 51mA. Table 1 shows the relationship between V_{OL} and I_{OL} with each technology.

TABLE 1. I_{OL} Demand

Device Technology	V_{OL} (V)	V_{TT} (V)	R_T (Ω)	I_{OL}(mA) (Note 1)
GTLP	0.65	1.5	25	34
BTL	1.10	2.1	19.5	51

Note 1: $I_{OL} = (V_{TT} - V_{OL})/R_T$

Many factors, both internal and external, affect the power consumption of a device: (1) number of outputs simultaneously switching, (2) operating frequency of the system, (3) junction temperature, and (4) capacitive load. The output power of both GTLP and BTL are supplied by an external output voltage supply (V_{TT}). When calculating the static high power consumption of the device, the device power is minimal during a static high event. This is because the output is in the high impedance state, and essentially zero current flows.

When considering static low drive current, the output power is at the worst case point. As seen in Table 2, GTLP uses less power than its predecessor BTL does. The power requirement is increased when considering that two 8-bit BTL devices are needed for one 16-bit GTLP device.

Power Consumption (Continued)

TABLE 2. Static and Dynamic Power Consumption

Device	I_{CCQ} (mA)	V_{OL} (V)	I_{OL} (mA)	P (mW) (Note 2)
GTLP16612	30	0.65	34	563
BTL3896	135	0.5	40	1737

Note 2: $P = V_{CC} * I_{CC} + n * (V_{OL} * I_{OL})$ where n = number of outputs

The dynamic power consumption comparison between BTL and GTLP can be shown graphically as a load line calculation. The I_{OL} curves in Figure 3 show this comparison. The dynamic power consumption of the two technologies are approximately the same given the same operating conditions, and when GTLP is used at its recommended operating conditions (1.0V for V_{REF}) it uses much less power. As previously discussed, GTLP offers twice the number of bits per device than the BTL technology does.
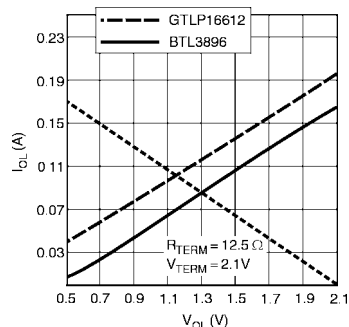
FIGURE 3. I_{OL} Characteristics with AC Load Line

Replacing BTL with GTLP

GTLP can be used in either high-speed new designs, where signal integrity and smooth edge transitions are crucial, or as an electrical drop-in solution for an existing BTL slot. The BTL family has many advantages over older CMOS and TTL logic families when designing large backplanes, and GTLP can be used in much higher performance backplanes than BTL while offering many of the same characteristics. GTLP has the capability of operating at a wide range of voltage levels without sacrificing signal integrity. GTLP can maintain adequate noise margin since V_{REF} is derived from V_{TT}. This flexibility allows GTLP to replace any equivalent BTL device.

Many BTL transceivers use a live insertion pin (LI) to support hot swapping of cards without disabling the system. This is necessary in some applications when changing or adding daughter cards to a backplane. When the LI pin is connected to V_{CC}, the output Schottky diode is reverse biased which minimizes bus loading by reducing the capacitance.

GTLP also supports live insertion applications. For instance, the GTLP16T1655 16-bit universal transceiver has a V_{CCbias} pin which forces 1V on the output pins. By pre-biasing the output pins to 1V, the device will prevent the backplane from rail-to-rail voltage swings which causes system problems upon live insertion of a daughter card.

Conclusion

Today's high performance systems require fast edge rates and smooth transitions with minimal ringing, overshoot/undershoot, and other signal integrity issues. The GTLP family offers a portfolio of translation devices and clock drivers that are not only capable of the fast HL/LH transitions demanded for high speed backplanes, but also feature a unique edge rate control characteristic that ensures smoother transitions.

By tuning the backplane with proper termination resistors and reference voltage techniques, GTLP can act as a drop-in electrical solution for BTL as well as support high-speed backplane systems up to 125 MHz and beyond. GTLP's real advantages occur when the devices are operated at their recommended normal operating specifications.

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