

## 2.5V Single Data Rate 1:10 Clock Buffer Terabuffer

### Features

- Optimized for 2.5V LVTTTL
- Guaranteed Low Skew < 25pS (max)
- Very low duty cycle distortion < 300pS (max)
- High speed propagation delay < 2nS. (max)
- Up to 200MHz operation
- Very low CMOS power levels
- Hot Insertable and over-voltage tolerant inputs
- 1:10 fanout buffer
- 2.5V Supply Voltage
- Available in TSSOP Package

The ASM2P5T9070A 2.5V single data rate (SDR) clock buffer is a single-ended input to ten single-ended outputs buffer built on advanced metal CMOS technology. The SDR clock buffer fanout from a single input to ten single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network.

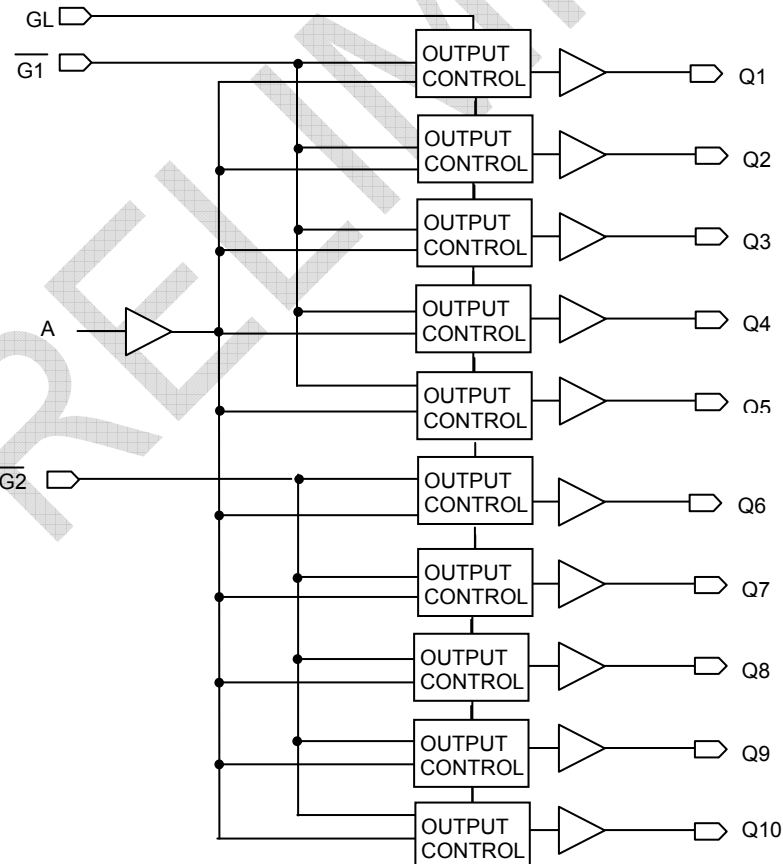
The ASM2P5T9070A has two output banks that can be asynchronously enabled/disabled. Multiple power and grounds reduce noise.

### Applications:

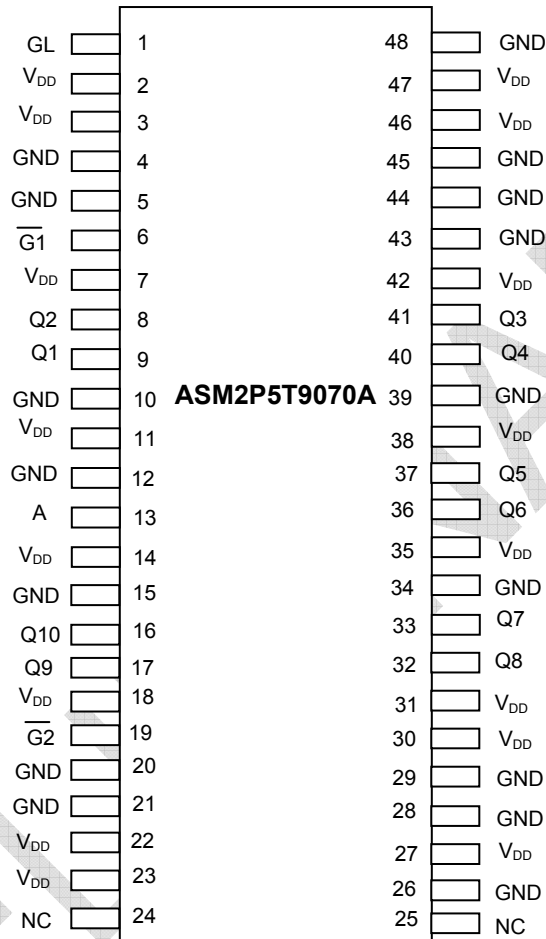
ASM2P5T9070A is targeted towards Clock and signal distribution applications.

### Functional Description

### Block Diagram



Top View – TSSOP Package



Pin Description

Symbol	I/O	Type	Description
A	I	LVTTTL	Clock input
$\overline{G1}$	I	LVTTTL	Gate for outputs Q1 through Q5. When $\overline{G1}$ is LOW, these outputs are enabled. When $\overline{G1}$ is HIGH, these outputs are asynchronously disabled to the level designated by GL <sup>1</sup> .
$\overline{G2}$	I	LVTTTL	Gate for outputs Q6 through Q10. When $\overline{G2}$ is LOW, these outputs are enabled. When $\overline{G2}$ is HIGH, these outputs are asynchronously disabled to the level designated by GL <sup>1</sup> .
GL	I	LVTTTL	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	O	LVTTTL	Clock outputs
V <sub>DD</sub>		PWR	Power supply for the device core, inputs, and outputs
GND		PWR	Power supply return for power

NOTE: Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

rev 0.2

**Absolute Maximum Ratings<sup>1</sup>**

Symbol	Description	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	-0.5 to +3.6	V
V <sub>I</sub>	Input Voltage	-0.5 to +3.6	V
V <sub>O</sub>	Output Voltage	-0.5 to V <sub>DD</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65to +165	° C
T <sub>J</sub>	Junction Temperature	150	° C

Note: 1. These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

**Capacitance<sup>1</sup>** (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ	Max	Unit
C <sub>IN</sub>	Input Capacitance		6		pF

NOTE:

1. This parameter is measured at characterization but not tested.

**Recommended Operating Range**

Symbol	Description	Min	Typ	Max	Unit
T <sub>A</sub>	Ambient Operating Temperature	-40	+25	+85	° C
V <sub>DD</sub>	Internal Power Supply Voltage	2.3	2.5	2.7	V

**DC Electrical Characteristics Over Operating Range<sup>1</sup>**

Symbol	Parameter	Test Conditions	Min	Typ <sup>4</sup>	Max	Unit
I <sub>IH</sub>	Input HIGH Current	V <sub>DD</sub> = 2.7V V <sub>I</sub> = V <sub>DD</sub> /GND			±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>DD</sub> = 2.7V V <sub>I</sub> = GND/V <sub>DD</sub>			±5	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>DD</sub> = 2.3V, I <sub>IN</sub> = -18mA		- 0.7	- 1.2	V
V <sub>IN</sub>	DC Input Voltage		-0.3		+3.6	V
V <sub>IH</sub>	DC Input HIGH <sup>2</sup>		1.7			V
V <sub>IL</sub>	DC Input LOW <sup>3</sup>		-		0.7	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -12mA	V <sub>DD</sub> - 0.4			V
		I <sub>OH</sub> = -100μA	V <sub>DD</sub> - 0.1			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 12mA			0.4	V
		I <sub>OL</sub> = 100μA			0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Voltage required to maintain a logic HIGH.

3. Voltage required to maintain a logic LOW.

4. Typical values are at V<sub>DD</sub> = 2.5V, +25°C ambient.

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Power Supply Characteristics

Symbol	Parameter	Test Conditions <sup>1</sup>	Typ	Max	Unit
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> Power Supply Current	V <sub>DD</sub> = Max., Reference Clock = LOW Outputs enabled, All outputs unloaded	1.5	2	mA
I <sub>DDD</sub>	Dynamic V <sub>DD</sub> Power Supply Current per Output	V <sub>DD</sub> = Max., V <sub>DD</sub> = Max., C <sub>L</sub> = 0pF	150	200	μA/MHz
I <sub>TOT</sub>	Total Power V <sub>DD</sub> Supply Current	V <sub>DD</sub> = 2.5V., F <sub>REFERENCE CLOCK</sub> = 100MHz, C <sub>L</sub> = 15pF	70	90	mA
		V <sub>DD</sub> = 2.5V., F <sub>REFERENCE CLOCK</sub> = 200MHz, C <sub>L</sub> = 15pF	100	150	

NOTE:

1. The termination resistors are excluded from these measurements.

Input AC Test Conditions

Symbol	Parameter	Value	Units
V <sub>IH</sub>	Input HIGH Voltage	V <sub>DD</sub>	V
V <sub>IL</sub>	Input LOW Voltage	0	V
V <sub>TH</sub>	Input Timing Measurement Reference Level <sup>1</sup>	V <sub>DD</sub> /2	V
t <sub>R</sub> , t <sub>F</sub>	Input Signal Edge Rate <sup>2</sup>	2	V/nS

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.

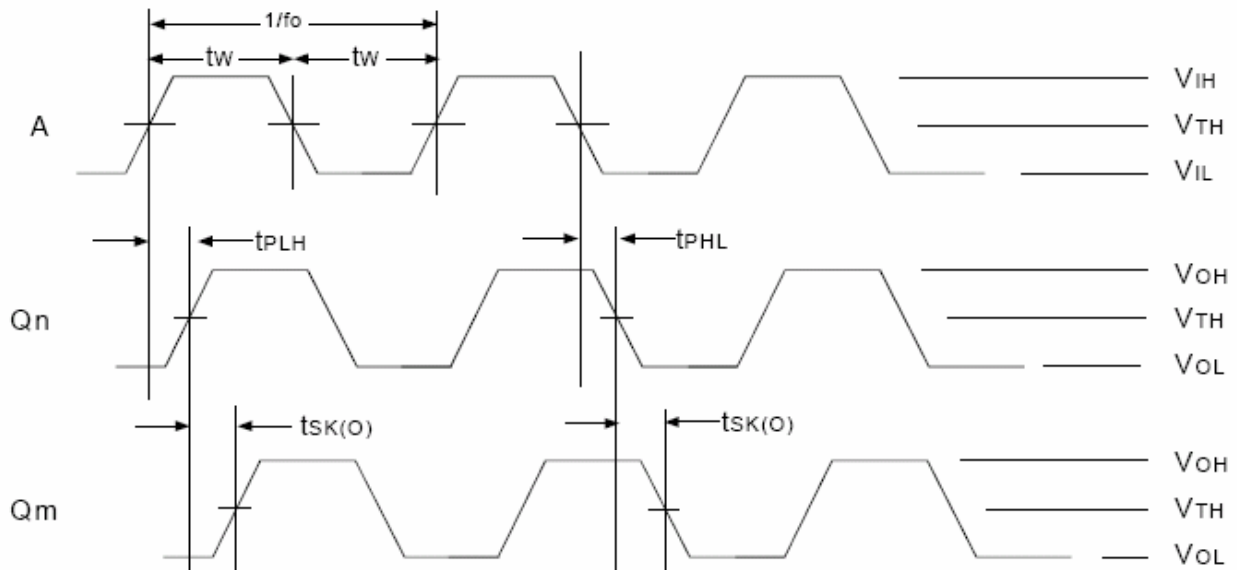
AC Electrical Characteristics Over Operating Range<sup>4</sup>

Symbol	Parameter	Min	Typ	Max	Unit
<b>Skew Parameters</b>					
t <sub>SK(O)</sub>	Same Device Output Pin-to-Pin Skew <sup>1</sup>			25	pS
t <sub>SK(P)</sub>	Pulse Skew <sup>2</sup>			300	pS
t <sub>SK(PP)</sub>	Part-to-Part Skew <sup>3</sup>			300	pS
<b>Propagation Delay</b>					
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A to Qn			2	nS
t <sub>R</sub>	Output Rise Time (20% to 80%)	350		850	pS
t <sub>F</sub>	Output Fall Time (20% to 80%)	350		850	pS
f <sub>o</sub>	Frequency Range			200	MHz
<b>Output Gate Enable/Disable Delay</b>					
t <sub>PGE</sub>	Output Gate Enable to Qn			3.5	nS
t <sub>PGD</sub>	Output Gate Enable to Qn Driven to GL Designated Level			3	nS

NOTES:

1. Skew measured between all outputs under identical input and output transitions and load conditions on any one device.
2. Skew measured is the difference between propagation delay times t<sub>PHL</sub> and t<sub>PLH</sub> of any output under identical input and output transitions and load conditions on any one device.
3. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical V<sub>DD</sub> levels and temperature.
4. Guaranteed by design.

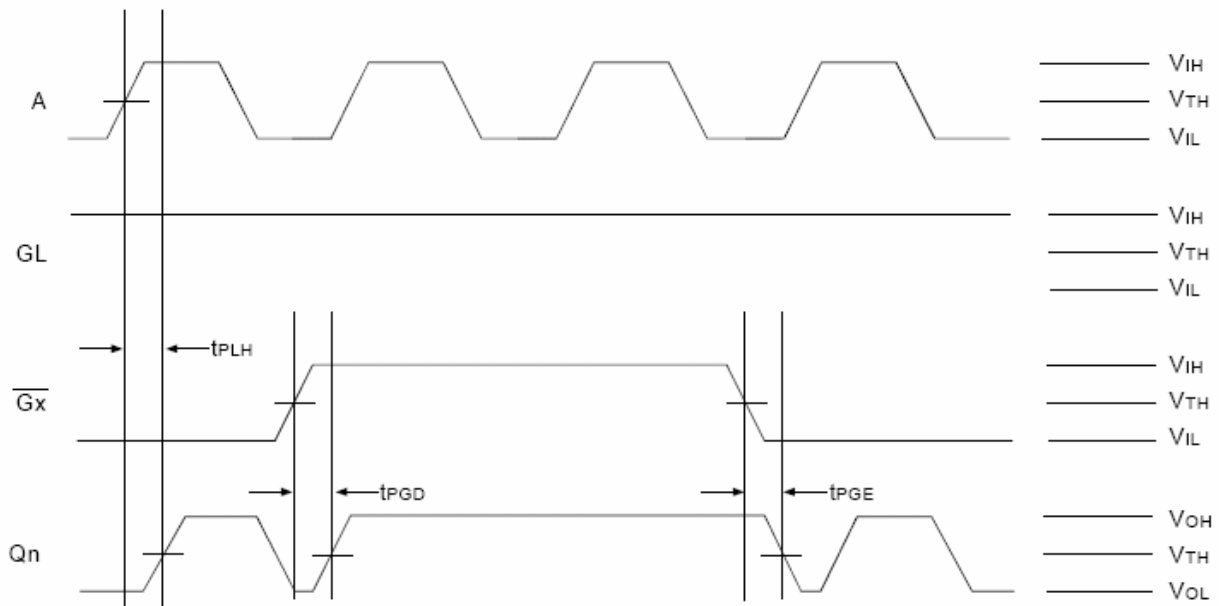
AC Timing Waveforms



Propagation and Skew Waveforms

NOTE: Pulse Skew is calculated using the following expression:

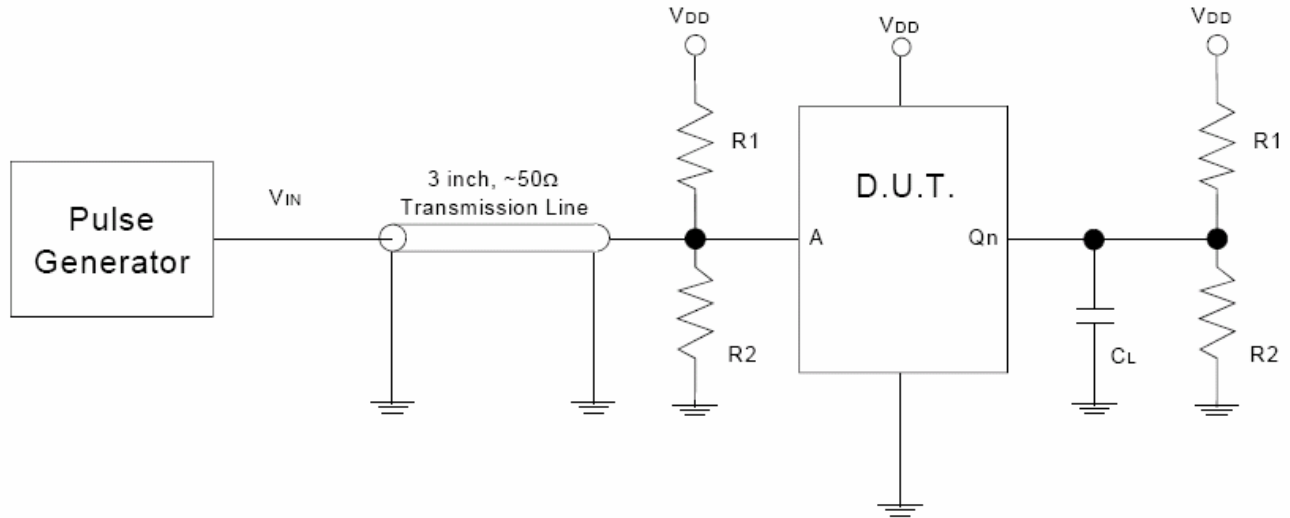
$t_{SK(P)} = |t_{PHL} - t_{PLH}|$   
 where  $t_{PHL}$  and  $t_{PLH}$  are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the  $t_{PHL}$  and  $t_{PLH}$  shown are not valid measurements for this calculation because they are not taken from the same pulse.



Gate Disable/Enable Runt Pulse Generation

NOTE: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their  $\overline{Gx}$  signals to avoid this problem.

**Test Circuit and Conditions**



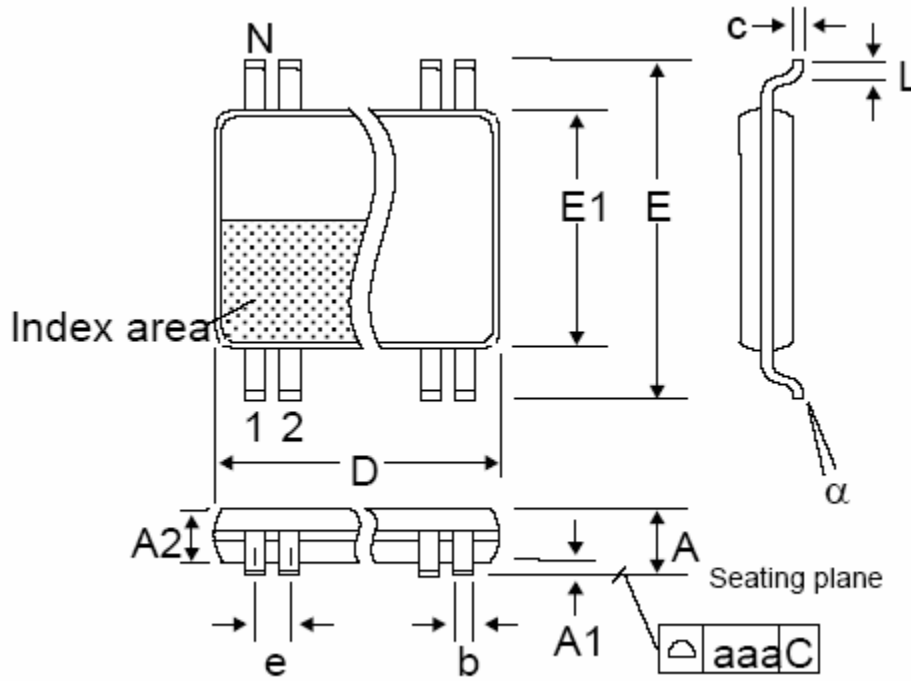
**Test Circuit for Input/Output**

**Input/Output Test Conditions**

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
$V_{TH}$	$V_{DD}/2$	V
R1	100	$\Omega$
R2	100	$\Omega$
$C_L$	15	pF

PRELIMINARY

48-lead TSSOP (6.10 mm Body, JEDEC MO-153-ED)

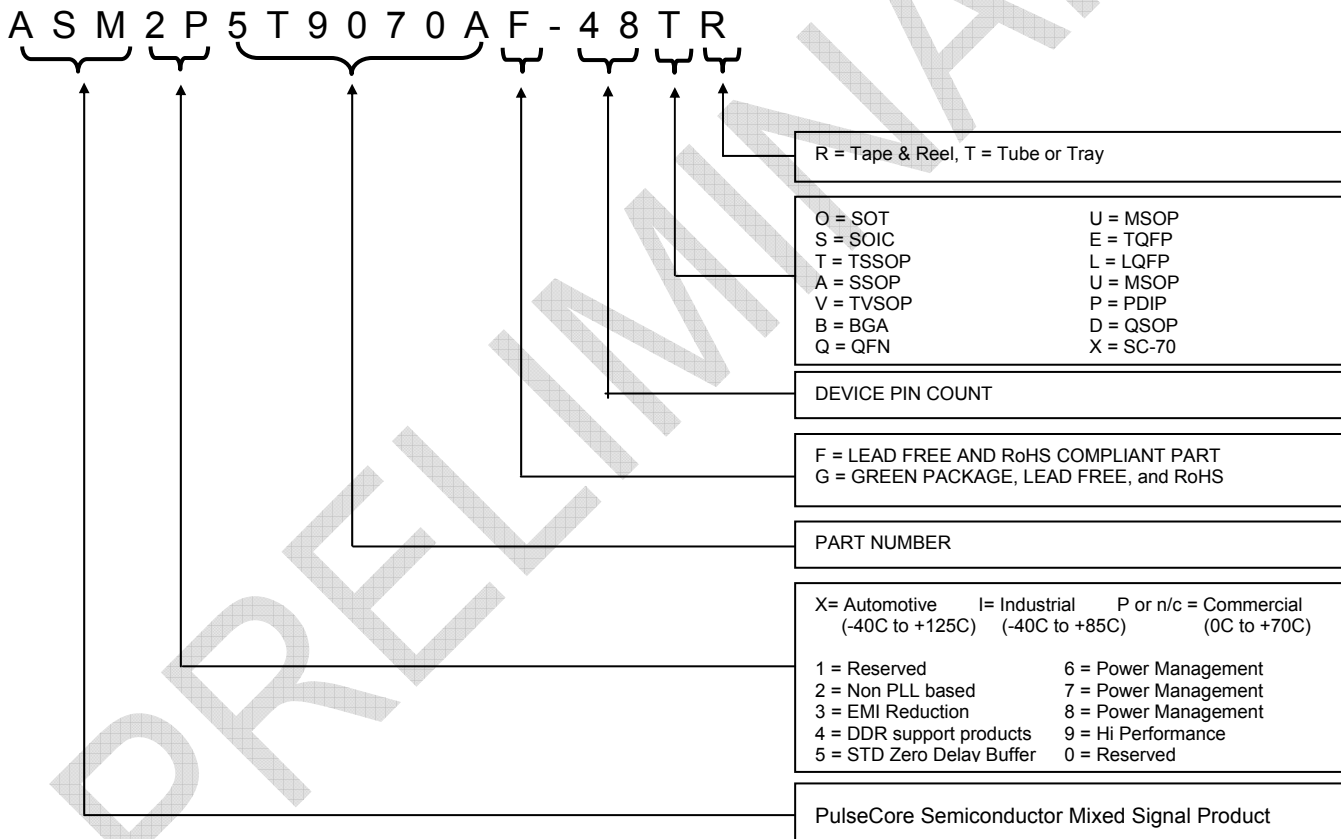


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.047	...	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.8	1.05
b	0.008 BSC		0.20 BSC	
c	0.004	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E1	0.236	0.244	6.00	6.20
E	0.319 BSC		8.10 BSC	
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
N	48			
α	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Operating Range
ASM2P5T9070AF-48TT	2P5T9070AF	48 Pin TSSOP, Tube, Pb Free	Commercial
ASM2P5T9070AF-48TR	2P5T9070AF	48 Pin TSSOP, Tape and Reel, Pb Free	Commercial
ASM2I5T9070AF-48TT	2I5T9070AF	48 Pin TSSOP, TUBE, Pb Free	Industrial
ASM2I5T9070AF-48TR	2I5T9070AF	48 Pin TSSOP, Tape and Reel, Pb Free	Industrial
ASM2P5T9070AG-48TT	2P5T9070AG	48 Pin TSSOP, Tube, Green	Commercial
ASM2P5T9070AG-48TR	2P5T9070AG	48 Pin TSSOP, Tape and Reel, Green	Commercial
ASM2I5T9070AG-48TT	2I5T9070AG	48 Pin TSSOP, TUBE, Green	Industrial
ASM2I5T9070AG-48TR	2I5T9070AG	48 Pin TSSOP, Tape and Reel, Green	Industrial

Ordering Information







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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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