AWT6223R
WCDMA/GSM/GPRS/Polar EDGE Power Amplifier Module with Integrated Power Control
Data Sheet - REV 2.0

FEATURES
- InGaP HBT Technology
- Optimized for a 50 Ω System
- Internal Reference Voltage
- Integrated GSM/EDGE Power Control with Temperature Compensation
- Low Profile Surface Mount Package: 6 mm x 8 mm x 1 mm
- RoHS Compliant Package, 250 °C MSL-3

WCDMA MODE
- HSDPA Compliant
- High Efficiency:
  - 41% @ P_{OUT} = +28.5 dBm
  - 21% @ P_{OUT} = +16 dBm
- Low Quiescent Current: 12 mA
- Low Leakage Current in Shutdown Mode: <1 μA
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage
- V_{EN} = +2.4 V (+2.2 V min over Temp)

GMSK MODE
- +35 dBm GSM850/900 Output Power
- +33 dBm DCS/PCS Output Power
- 55 % GSM850/900 PAE
- 50 % DCS/PCS PAE
- Power Control Range > 50 dB
- EGPRS Capable (class 12)

EDGE MODE
- +29 dBm GSM850/900 Output Power
- +28.5 dBm DCS/PCS Output Power
- 27 % GSM850/900 PAE
- 30 % DCS/PCS PAE
- -63 dBc/30 kHz Typical ACPR (400 kHz)
- -77 dBc/30 kHz Typical ACPR (600 kHz)

APPLICATIONS
- 3G Handsets, Smartphones, Data Devices Incorporating:
  - WCDMA (IMT)
  - GSM850/GSM900/DCS/PCS Bands
  - GMSK and 8-PSK (Open Loop Polar) Modulations

PRODUCT DESCRIPTION
The AWT6223R WEDGE module supports dual, tri, or quad band operation using GMSK/GPRS and 8-PSK (open loop polar) modulations, and WCDMA operation in the IMT band. The AWT6223R module is manufactured using ANADIGICS' advanced InGaP HBT MMIC technology to provide reliability, temperature stability, and ruggedness. This penta-band module consists of three amplifier chains; one to support GSM/GPRS/EGPRS in cellular bands, one to support GSM/GPRS/EGPRS in DCS/PCS bands, and one to support WCDMA in the IMT band. In addition, the AWT6223R module includes an internal reference voltage and integrated power control with temperature compensation for use in GMSK and 8-PSK modes of operation. These features facilitate fast and easy production calibration, minimize performance variation over temperature, and reduce the number of external components required.

The WCDMA PA incorporates ANADIGICS' HELP2™ technology. Through selectable bias modes, the AWT6223R achieves optimal efficiency across different output power levels, specifically at low and mid-range power levels where the PA typically operates, thereby dramatically increasing handset talk-time and standby-time. Its built-in voltage regulator eliminates the need for an external reference voltage and switch components, reducing PCB area and BOM costs. All of the RF ports for this device are internally matched to 50 Ω. The RF inputs GSM_IN and DCS/PCS_IN both have shunt resistors to ground to maintain a good input VSWR as the V_{RAMP} power control voltage is varied. Internal DC blocks are provided at the RF outputs.

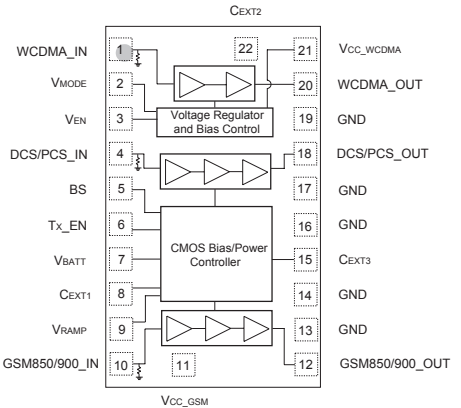


Figure 1: Block Diagram

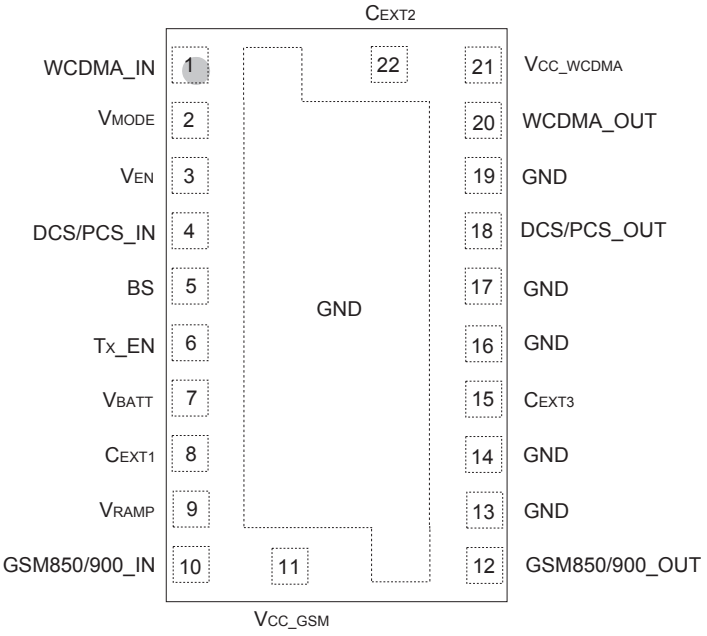


Figure 2: Pinout (X - ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	WCDMA_IN	WCDMA RF Input	12	GSM850/900_OUT	GSM850/900 RF Output
2	V_{MODE}	WCDMA Mode Control Voltage	13	GND	Ground
3	V_{EN}	WCDMA Shutdown	14	GND	Ground
4	DCS/PCS_IN	DCS/PCS RF Input	15	C_{EXT3}	Bypass for Power Control Regulator
5	BS	Band Select Logic Input	16	GND	Ground
6	T_X_EN	TX Enable Logic Input	17	GND	Ground
7	V_{BATT}	Battery Supply	18	DCS/PCS_OUT	DCS/PCS RF Output
8	C_{EXT1}	Bypass for Internal Voltage Regulator	19	GND	Ground
9	V_{RAMP}	Analog signal used to control the GSM output power	20	WCDMA_OUT	WCDMA RF Output
10	GSM850/900_IN	GSM850/900 RF Input	21	V_{CC_WCDMA}	WCDMA Supply Voltage
11	V_{CC_GSM}	V_{CC} test point for GSM secton. Do not connect. Do not ground.	22	C_{EXT2}	Bypass for WCDMA V_{CC1}

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Supply Voltage (V_{BATT})	-	+6	V
Supply Voltage (V_{CC_WCDMA})	-	+5	V
RF Input Power (RF_{IN})	-	10	dBm
GSM/EDGE Output Control Voltage (V_{RAMP})	-0.3	1.8	V
WCDMA Control Voltages (V_{MODE}, V_{EN})	0	3.5	V
Storage Temperature (T_{STG})	-55	150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

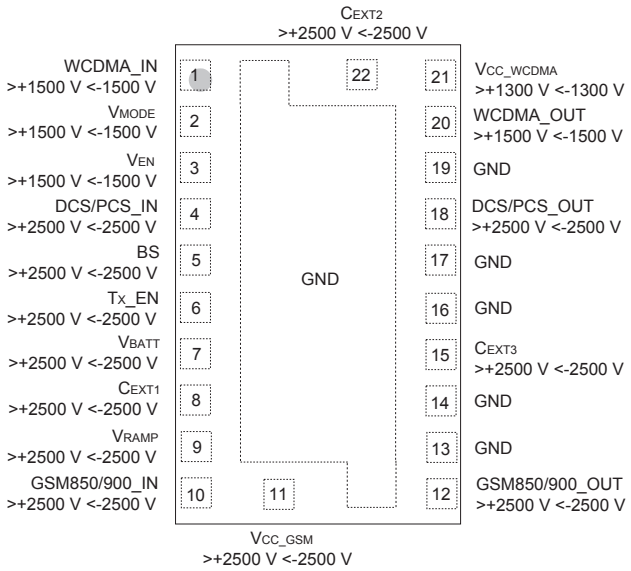


Figure 3: ESD Pin Rating

Electrostatic Discharge Sensitivity

The AWT6223R part was tested to determine the ESD sensitivity of each package pin with respect to Ground. Non-ground pins are stressed with 1 positive pulse or 1 negative pulse with respect to the Ground using the Human Body Model apparatus and waveform outlined in JESD22-A114C.01. Determination of pass or fail is made according to whether the part passes key RF tests against the datasheet limits after stress. Results of the test are presented in Figure 3:

- Rating for WCDMA_IN, V_{MODE}, V_{EN}, and WCDMA_OUT is +1500V and -1500V;
- Rating for V_{CC_WCDMA} is +1300V and -1300V;
- Rating for DCS/PCS_IN, BS, Tx_EN, V_{BATT}, C_{EXT1}, V_{RAMP}, GSM_IN, V_{CC_GSM}, GSM_OUT, C_{EXT3} and DCS/PCS_OUT is +2500V and -2500V

It is very important to take all necessary precautions, listed in Application Notes “ESD precautions for ANADIGICS GaAs MMIC,” to avoid ESD damage to

Table 3: GSM/EDGE Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
Case temperature (T_C)	-20	-	85	°C	
Supply voltage (V_{BATT})	3.0	3.5	4.8	V	
Total Power Supply Leakage Current	-	1	10	µA	V_{BATT} = V_{CC_WCDMA} = 4.8 V, V_{EN} = 0 V, V_{MODE} = 0 V, BS = 0 V, V_{RAMP} = 0 V, TX_EN = LOW, No RF applied
Control Voltage Range	0.2	-	1.6	V	
Turn On Time (T_{ON})	-	-	1	µs	V_{RAMP} = 0.2 V, TX_EN = LOW → HIGH P_{IN} = 5 dBm
Turn Off Time (T_{OFF})	-	-	1	µs	V_{RAMP} = 0.2 V, TX_EN = LOW → HIGH P_{IN} = 5 dBm
Rise Time (T_{RISE})	-	-	1	µs	P_{OUT} = -10 dBm → P_{MAX} (within 0.2 dB)
Fall Time (T_{FALL})	-	-	1	µs	P_{OUT} = P_{MAX} → -10 dBm (within 0.2 dB)
V_{RAMP} Input Capacitance	-	3	-	pF	
V_{RAMP} Input Current	-	-	10	µA	
Duty Cycle	-	-	50	%	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

1. Do not apply a DC voltage to the GSM_IN or DCS/PCS_IN RF inputs.

Table 4: GSM/EDGE Digital Inputs

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic High Voltage	V_{IH}	1.2	-	3.0	V
Logic Low Voltage	V_{IL}	-	-	0.5	V
Logic High Current	$\|I_{IH}\|$	-	-	30	µA
Logic Low Current	$\|I_{IL}\|$	-	-	30	µA

Table 5: GSM/EDGE Logic Control

OPERATIONAL MODE	BS	TX_EN
GSM850/900	LOW	HIGH
DCS/PCS	HIGH	HIGH
PA DISABLED	-	LOW

Notes:

1. V_{BATT} must be applied before taking BS and/or T_X_EN High.

Table 6: Electrical Characteristics for GSM850 GMSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 µs, Duty = 25%, Z_{IN} = Z_{OUT} = 50 Ω, T_C = 25 °C, V_{RAMP} = 1.6 V, BS = LOW, T_X_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_O)	824	-	849	MHz	
Input Power	0	3	5	dBm	
Output Power, P_{MAX}	34.5	35	-	dBm	Freq = 824 to 849 MHz
Degraded Output Power	32.0	32.5	-	dBm	V_{BATT} = 3.0 V, T_C = 85 °C P_{IN} = 0 dBm
PAE @ P_{MAX}	48	52	-	%	Freq = 824 to 849 MHz
Forward Isolation 1	-	-42	-30	dBm	T_X_EN = LOW, P_{IN} = 5 dBm
Forward Isolation 2	-	-25	-20	dBm	T_X_EN = HIGH,V_{RAMP} = 0.2V, P_{IN} = 5 dBm
Cross Isolation $2F_O$ @ DCS/PCS port $3F_O$ @ DCS/PCS port	 - -	 -36 -25	 -20 -20	dBm	V_{RAMP} =0.2V to V_{RAMP_MAX}
Second Harmonic	-	-20	-10	dBm	Over all output power levels
Third Harmonic	-	-30	-10	dBm	Over all output power levels
n x F_O (n ≥ 4), F_O ≤ 12.75 GHz	-	-30	-10	dBm	Over all output power levels
Stability	VSWR = 8:1 All Phases , P_{OUT} ≤ 34.5 dBm				
	-	-	-36	dBm	F_{OUT} < 1 GHz
	-	-	-30	dBm	F_{OUT} > 1 GHz
Ruggedness	No Permanent Degradation, VSWR 10:1, All Phase Angles				P_{OUT} ≤ 34.5 dBm
RX Noise Power	-	-86	-83	dBm	F_{TX} = 849 MHz, RBW = 100 kHz F_{RX} = 869 to 894 MHz, P_{OUT} ≤ 34.5 dBm
Input Return Loss	-	1.5:1	2.5:1	VSWR	Over all output power levels

Table 7: Electrical Characteristics for GSM900 GMSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 µs, Duty = 25%, $Z_{IN} = Z_{OUT}$ = 50 Ω, T_C = 25 °C, V_{RAMP} = 1.6 V, BS = LOW, Tx_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_O)	880	-	915	MHz	
Input Power	0	3	5	dBm	
Output Power, P_{MAX}	34.5	35	-	dBm	Freq = 880 to 915 MHz
Degraded Output Power	32.0	32.5	-	dBm	V_{BATT} = 3.0 V, T_C = 85 °C P_{IN} = 0 dBm
PAE @ P_{MAX}	50	55	-	%	Freq = 880 to 915 MHz
Forward Isolation 1	-	-40	-30	dBm	Tx_EN = LOW, P_{IN} = 5 dBm
Forward Isolation 2	-	-25	-20	dBm	Tx_EN = HIGH,V_{RAMP} = 0.2V, P_{IN} = 5 dBm
Cross Isolation $2F_O$ @ DCS/PCS port $3F_O$ @ DCS/PCS port	 - -	 -34 -22	 -20 -17	dBm	V_{RAMP} =0.2V to V_{RAMP_MAX}
Second Harmonic	-	-25	-10	dBm	Over all output power levels
Third Harmonic	-	-27	-10	dBm	Over all output power levels
n x F_O (n ≥ 4), F_O ≤ 12.75 GHz	-	-30	-10	dBm	Over all output power levels
Stability	VSWR = 8:1 All Phases , P_{OUT} ≤ 34.5 dBm				
	-	-	-36	dBm	F_{OUT} < 1 GHz
	-	-	-30	dBm	F_{OUT} > 1 GHz
Ruggedness	No Permanent Degradation, VSWR 10:1, All Phase Angles				P_{OUT} ≤ 34.5 dBm
RX Noise Power	-	-83	-77	dBm	F_{TX} = 915 MHz, RBW = 100 kHz F_{RX} = 925 to 935 MHz, P_{OUT} ≤ 34.5 dBm
	-	-86	-83	dBm	F_{TX} = 915 MHz, RBW = 100 kHz F_{RX} = 935 to 960 MHz, P_{OUT} ≤ 34.5 dBm
Input Return Loss	-	1.5:1	2.5:1	VSWR	Over all output power levels

Table 8: Electrical Characteristics for GSM850 8PSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 µs, Duty = 25%
Z_{IN} = Z_{OUT} = 50 Ω, T_C = 25 °C, BS = LOW, Tx_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_{IN})	824 880	- -	849 915	MHz	
Input Power	0	3	5	dBm	
PAE	20	27	-	%	F_{IN} = 824 to 849 MHz P_{OUT} set = +29 dBm
ACPR 200 kHz 400 kHz 600 kHz 1800 kHz	 - - - -	 -39 -63 -74 -77	 -34 -58 -64 -68	 dBc/30 kHz dBc/30 kHz dBc/30 kHz dBc/100 kHz	 All conditions under Polar operation P_{OUT} = +29 dBm
EVM	-	1	5	%	All Conditions under Polar operation P_{OUT} = +29 dBm

Table 9: Electrical Characteristics for DCS GMSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 µs, Duty = 25%, Z_{IN} = Z_{OUT} = 50 Ω, T_C = 25 °C, V_{RAMP} = 1.6 V, BS = HIGH, T_X_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1710	-	1785	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	29.5	30.5	-	dBm	V_{BATT} = 3.0 V, T_C = 85 °C P_{IN} = 0 dBm
PAE @ P_{MAX}	45	50	-	%	Freq = 1710 to 1910 MHz
Forward Isolation 1	-	-40	-33	dBm	T_X_EN = LOW, P_{IN} = 5dBm
Forward Isolation 2	-	-24	-20	dBm	T_X_EN =HIGH, V_{RAMP} = 0.2 V, P_{IN} = 5 dBm
Second Harmonic	-	-18	-10	dBm	Over all output power levels
Third Harmonic	-	-24	-10	dBm	Over all output power levels
n x F_O (n ≥ 4), F_O ≤ 12.75 GHz	-	-30	-10	dBm	Over all output power levels
Stability	VSWR = 8:1 All Phases , P_{OUT} ≤ 32 dBm				
	-	-	-36	dBm	F_{OUT} < 1 GHz
	-	-	-30	dBm	F_{OUT} > 1 GHz
Ruggedness	No Permanent Degradation, VSWR 10:1, All Phase Angles				P_{OUT} ≤ 32 dBm
RX Noise Power	-	-86	-80	dBm	F_{TX} = 1785 MHz, RBW = 100 kHz, F_{RX} =1805 to 1880 MHz, P_{OUT} ≤ 32 dBm
Input Return Loss	-	1.5:1	2.5:1	VSWR	Over all output power levels

Table 10: Electrical Characteristics for PCS GMSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 µs, Duty = 25%, Z_{IN} = Z_{OUT} = 50 Ω, T_C = 25 °C, V_{RAMP} = 1.6 V, BS = HIGH, Tx_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1850	-	1910	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	29.5	30.5	-	dBm	V_{BATT} = 3.0 V, T_C = 85 °C P_{IN} = 0 dBm
PAE @ P_{MAX}	45	50	-	%	Freq = 1710 to 1910 MHz
Forward Isolation 1	-	-37	-33	dBm	Tx_EN = LOW, P_{IN} = 5dBm
Forward Isolation 2	-	-22	-18	dBm	Tx_EN =HIGH, V_{RAMP} = 0.2 V, P_{IN} = 5 dBm
Second Harmonic	-	-28	-10	dBm	Over all output power levels
Third Harmonic	-	-24	-10	dBm	Over all output power levels
n x F_O (n ≥ 4), F_O ≤ 12.75 GHz	-	-30	-10	dBm	Over all output power levels
Stability	VSWR = 8:1 All Phases , P_{OUT} ≤ 32 dBm				
	-	-	-36	dBm	F_{OUT} < 1 GHz
	-	-	-30	dBm	F_{OUT} > 1 GHz
Ruggedness	No Permanent Degradation, VSWR 10:1, All Phase Angles				P_{OUT} ≤ 32 dBm
RX Noise Power	-	-86	-80	dBm	F_{TX} = 1910 MHz, RBW = 100 kHz, F_{RX} =1930 to 1990 MHz, P_{OUT} ≤ 32 dBm
Input Return Loss	-	1.5:1	2.5:1	VSWR	Over all output power levels

Table 11: Electrical Characteristics for DCS 8PSK Mode
(Unless Otherwise Specified: V_{BATT} = 3.5 V, P_{IN} = 3.0 dBm, Pulse Width =1154 μs, Duty = 25%, Z_{IN} = Z_{OUT} = 50 Ω, TC = 25 °C , BS =HIGH, Tx_EN = HIGH, V_{EN} = LOW)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_{IN})	1710 1850	-	1785 1910	MHz	
Input Power	0	3	5	dBm	
PAE	25	30	-	%	F_{IN} = 1710 to 1785 MHz P_{OUT} set = +28.5 dBm
ACPR 200 kHz 400 kHz 600 kHz 1800 kHz	 - - - -	 -38 -64 -77 -77	 -34 -58 -64 -68	 dBc/30 kHz dBc/30 kHz dBc/30 kHz dBc/100 kHz	 All conditions under Polar operation P_{OUT} = +28.5 dBm
EVM	-	1	5	%	All Conditions under Polar operation P_{OUT} = +28.5 dBm

Table 12: WCDMA Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
Case temperature (T_C)	-20	-	85	°C	
Supply Voltage (V_{CC})	+3.2	+3.4	+4.2	V	$P_{OUT} \leq$ +28.5 dBm
WCDMA Enable Voltage (V_{EN})	+2.2 0	+2.4 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE})	+2.2 0	+2.4 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT}) 3GPP HSDPA Case A HSDPA Case B HSDPA Case C	 +28.0 (1) +27.0 (1) +26.0 (1) +25.5 (1)	 +28.5 +27.5 +26.5 +26.0	 - - - -	dBm	 $1/15 \leq \beta_c/\beta_d \leq 12/15$ $13/15 \leq \beta_c/\beta_d \leq 15/8$ $15/7 \leq \beta_c/\beta_d \leq 15/0$

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:
(1) WCDMA operation at V_{CC} = +3.2 V, P_{OUT} is derated by 0.5 dB.
(2) Do not apply a DC voltage to the WCDMA_IN RF input.

Table 13: WCDMA Bias Control

APPLICATION	P_{OUT} LEVELS	LOGIC	V_{EN}	V_{MODE}
WCDMA - low power	$\leq$+16 dBm	Low	+2.4 V	+2.4 V
WCDMA - high power	>+16 dBm	High	+2.4 V	0 V
Shutdown	-	Shutdown	0 V	0 V

Notes:
1. For WCDMA operation set T_X_EN = LOW.

Table 14: Electrical Characteristics for WCDMA
(Unless Otherwise Specified: T_C = 25 °C, V_{BATT} = +3.4 V, Tx_EN = LOW, 50 Ω system, V_{EN} = 2.4 V)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1920	-	1980	MHz	
Gain	24.5 13.0	26.5 15.0	28.5 17.0	dB	P_{OUT} = +28.5 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
ACLR1 at 5 MHz offset (1)	- -	-40 -43	-38 -38	dBc	P_{OUT} = +28.5 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
ACLR2 at 10 MHz offset	- -	-56 -52	-48 -48	dBc	P_{OUT} = +28.5 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Power-Added Efficiency (1)	37 18	41 21	- -	%	P_{OUT} = +28.5 dBm, V_{MODE} = 0 V P_{OUT} = +16 dBm, V_{MODE} = +2.4 V
Quiescent Current (Icq)	-	12	20	mA	V_{MODE} = +2.4 V
Enable Current	-	0.2	1	mA	through V_{EN} pin
Battery Current	-	3	5	mA	through V_{BATT} pin, V_{MODE} = +2.4 V
Mode Control Current	-	0.3	1	mA	through V_{MODE} pin, V_{MODE} = +2.4 V
Noise in Receive Band	-	-138	-135	dBm/Hz	2110 MHz to 2170 MHz
Harmonics 2fo 3fo, 4fo	 - -	 -43 -50	 -35 -35	dBc	$P_{OUT} \leq$ +28.5 dBm
Input Impedance	-	-	2:1	VSWR	
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	$P_{OUT} \leq$ +28.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions
Load mismatch stress with no permanent degradation or failure	10:1	-	-	VSWR	Applies over full operating range

Notes:
(1) ACLR and Efficiency measured at 1950 MHz.

APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

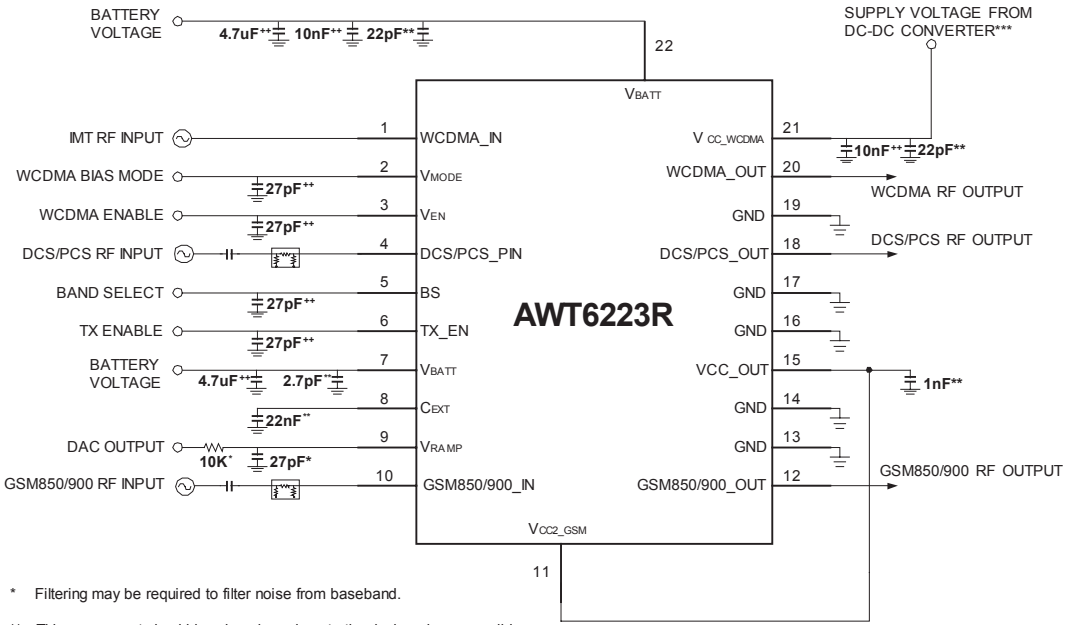
Shutdown Mode

The WCDMA power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to both the V_{EN} and V_{MODE} voltages.

Bias Modes

The WCDMA power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to the V_{MODE} voltage. The Bias Control table lists the recommended modes of operation for various applications.

Two operating modes are recommended to optimize current consumption. High Bias operating mode is for P_{OUT} levels $\geq$ 16 dBm. At or below +16 dBm, the PA should be "Mode Switched" to Low Bias Mode.



* Filtering may be required to filter noise from baseband.

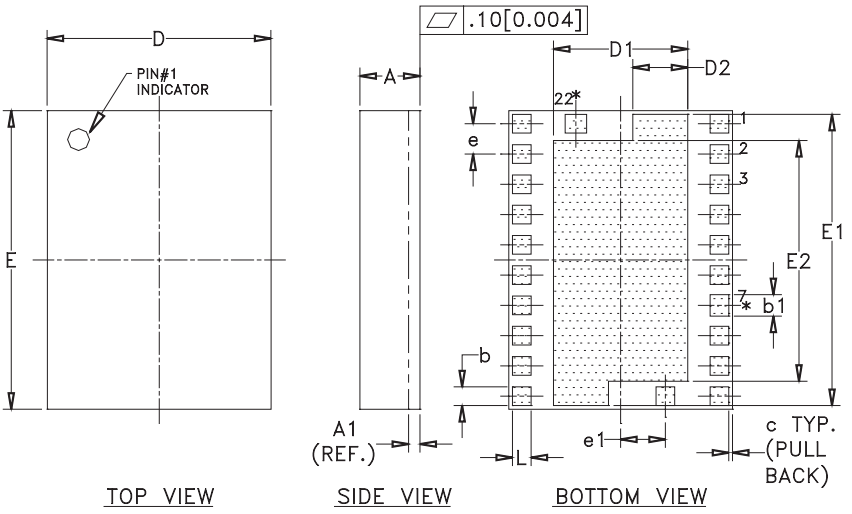
** This component should be placed as close to the device pin as possible.

*** If the final design uses a DC-DC Converter, otherwise connect Pin 21 directly to V_{BATT} Pin 22.

++ These components are recommended as good design practice for improving noise rejection characteristics. The values specified are not critical as they may not be required in the final application.

Figure 4: Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.84	0.98	1.12	0.033	0.038	0.044	–
A1	0.32 (REF.)			0.013 (REF.)			–
b	0.47	–	0.53	0.019	–	0.021	20X
b1	0.54	–	0.60	0.021	–	0.023	2X
c	–	0.10	–	–	0.004	–	–
D	5.88	6.00	6.12	0.231	0.236	0.241	–
D1	3.54	–	3.66	0.139	–	0.144	–
D2	1.41	–	1.53	0.056	–	0.060	2X
E	7.88	8.00	8.12	0.310	0.315	0.320	–
E1	7.74	–	7.86	0.305	–	0.309	–
E2	6.39	–	6.51	0.252	–	0.256	–
e		0.81			0.032		–
e1		1.20			0.047		2X
L	0.47	–	0.53	0.019	–	0.021	–

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.

Figure 5: Package Outline - 22 Pin 6 mm x 8 mm x 1 mm Surface Mount Package

TOP BRAND

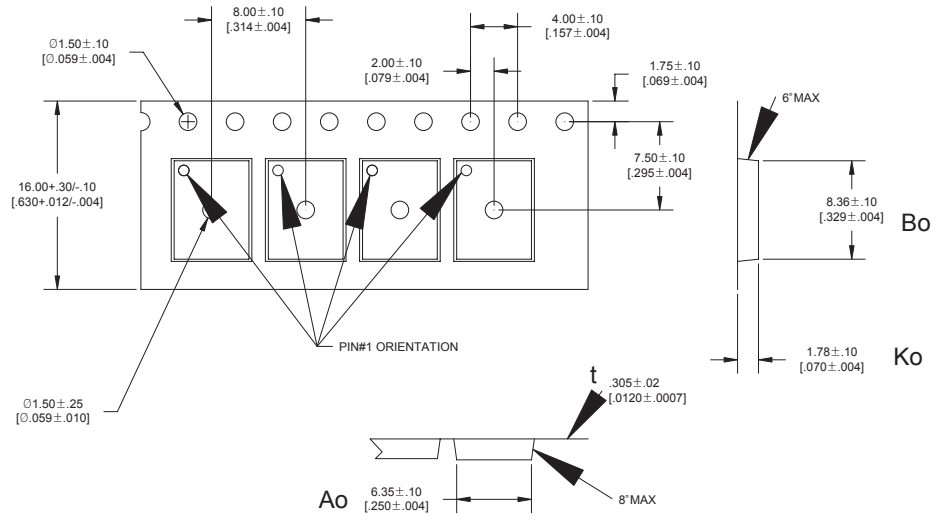
BRANDING SPECIFICATION

NOTES:

1. PIN 1 INDICATOR:	LASER MARK
2. ANADIGICS LOGO SIZE:	X=0.040±0.010 Y=0.048±0.010
3. JEDEC LEADFREE MARK:	0.040 DIA.
4. TEXT :	SIZE : AS LARGE AS POSSIBLE
5. PART #	AWT6223R = RoHS COMPLIANT
6. YEAR AND WORK WEEK:	YYWW: YY = YEAR, WW = WORK WEEK
7. WAFER LOT NUMBER:	LLLLL = WAFER LOT#, SS = WAFER ID:
8. BOM NUMBER:	069
9. COUNTRY CODE:	CC = TH –for– THAILAND, TW –for– TAIWAN, PH –for– PHILLIPPINES, CH –for– CHINA, ID –for– INDONESIA, HK –for– HONG KONG

Figure 6: Branding Specification

COMPONENT PACKAGING



NOTES:

1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

Figure 7: Tape & Reel Packaging

Table 14: Tape & Reel Dimensions

PACKAGE TYPE	TAPE WIDTH	POCKET PITCH	REEL CAPACITY	MAX REEL DIA
6 mm x 8 mm x 1 mm	16 mm	8 mm	2500	13"

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6223RM26P8	-20 °C to +85 °C	RoHS Compliant 24 Pin 6 mm x 8 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6223RM26P9	-20 °C to +85 °C	RoHS Compliant 24 Pin 6 mm x 8 mm x 1 mm Surface Mount Module	Tape and Reel, Partial Reel

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