

#### **Description**

The E737 is a precision measurement unit designed for automatic test equipment and instrumentation. Manufactured in a wide voltage CMOS process, it is a monolithic solution for a per pin PMU.

The E737 supports two modes of operation: force current/measure voltage and force voltage/measure current. The E737 can force or measure voltage in the range of -5V to +7V. In addition, the E737 can force or measure a current of up to 40 mA over four distinct ranges:  $\pm 40$  mA,  $\pm 1$  mA,  $\pm 100$   $\mu$ A and  $\pm 10$   $\mu$ A.

The E737 has an on board window comparator that provides three bits of information: DUT too high, DUT too low, and DUT fail. There is also a monitor function which provides a real time analog voltage signal proportional to either the DUT voltage or current.

On board clamps prevent large transient spikes when changing operating mode or current range. Also, the PMU will survive a direct short over the legal voltage range.

The E737 is designed to be a low power, low cost, small footprint solution to allow high pin count testers to support a PMU per pin.

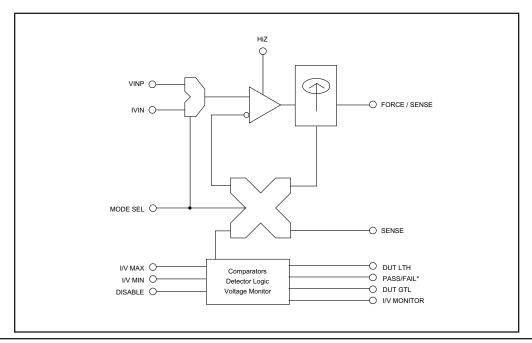
### **Features**

- FV / MI Capability
- FI / MV Capability
- 4 Current Ranges (±40 mA, ±1 mA, ±100 μA, ±10 μA)
- -5V/+7V I / O Range
- · Short Circuit Protection
- Clamps for limiting mode and range select transients

### **Applications**

- Automatic Test Equipment
  - Memory Testers
  - VLSI Testers
  - Mixed Signal Tester

### **Functional Block Diagram**





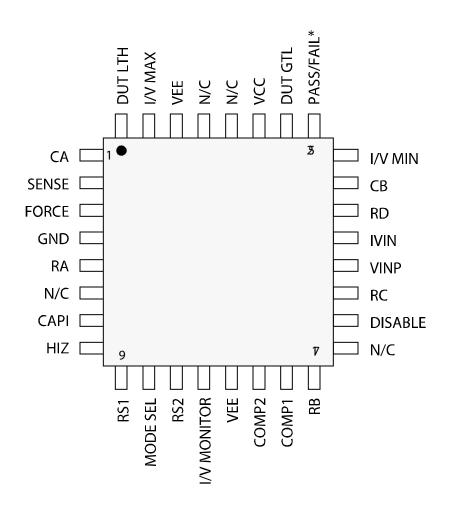
## Pin Description

Pin Name	Pin#	Description
VINP	20	Analog voltage input which forces the output voltage at FORCE (FV/MI mode).
IVIN	21	Analog voltage input which forces the output current at FORCE (FI/MV mode).
FORCE	3	Analog output pin which forces current or voltage.
SENSE	2	Analog input pin which senses voltage (typically connected to FORCE).
MODE SEL	10	Digital input which determines whether the PMU is forcing voltage or forcing current.
RS1, RS2	9, 11	Digital inputs which select one of the four current ranges.
I/V MIN I/V MAX	24 31	Analog input voltages which establish the lower and upper threshold level for the measurement comparator.
DUT LTH DUT GTL	32 26	Digital comparator open drain outputs that indicate the DUT measurement is less than the upper threshold and greater than the lower threshold.
PASS/FAIL*	25	Digital output that indicates whether or not the monitored voltage is between the comparator thresholds. Logic1 corresponds to a measurement that is between comparator thresholds.
DISABLE	18	Digital input which places the digital comparator outputs a I/V MONITOR in high impedance.
HiZ	8	Digital input which places the FORCE output into high impedance.
RA, RB RC, RD	5,16 19,22	External resistors corresponding to ranges A through D.
I/V MONITOR	12	Analog voltage output that provides a real time monitor of either the measured voltage or measured current level.
COMP1 COMP2	15 14	External compensation pins that require an external capacitor connected between the two pins.
VCC	27	Positive analog power supply.
VEE	13, 30	Negative analog power supply.
CA CB	1 23	External compensation pins that require an external capacitor connected between the two pins.
CAPI	7	External compensation pin that requires an external capacitor connected to ground.
GND	4	Ground.



Pin Description (continued)

32 Pin LQFP (7 mm x 7 mm x 1.4 mm) (Top View)





### **Circuit Description**

#### **Circuit Overview**

The E737 is a parametric test and measurement unit that can:

- Force Voltage / Measure Current
- · Force Current / Measure Voltage.

The E737 can force or measure voltage over a -5V to +7V range, and force or measure current over four distinct ranges:

- ± 40 mA
- ± 1 mA
- ± 100 µA
- ± 10 µA.

An on board window comparator provides three-bit measurement range classification. Also, a monitor passes a real time analog signal which tracks either the DUT's current or voltage performance.

#### **Control Inputs**

MODE SEL is a digital input which determines whether the PMU forces voltage or current, when it is not placed in a high impedance state by the HIZ input (see Table 1).

HiZ	Mode SEL	PMU Operation
1	X	High Impedance
0	0	FV/MI
0	1	FI/MV

Table 1.

RS1 and RS2 are digital inputs to an analog MUX which establishes the full scale current range of the PMU. One of four current ranges can be selected by using RS1 and RS2 as shown in Table 2.

Rext Nom	RS1	RS2	Current Range
RA = 200KΩ	0	0	A: ±10μA
RB = 20KΩ	0	1	B: ±100μA
$RC = 2K\Omega$	1	1	C: ±1mA
$RD = 50\Omega$	1	0	D: ±40mA

Table 2.

#### **Comparator Outputs**

The comparator outputs DUT GTL, DUT LTH, and PASS/FAIL\* are open drain outputs. When active (logical 0), they will pull to ground. When disabled (logical 1 or DISABLE = 1), they require an external pull up resistor to a positive voltage to achieve a high state.

#### Force / Sense

FORCE is an analog output which either forces a current or forces a voltage, depending on which operating mode is selected.

The SENSE pin is a high impedance analog input which measures the DUT voltage input in the FI / MV operating mode.

FORCE and SENSE are brought out to separate pins to allow for remote sensing.

#### I/V MONITOR

I/V MONITOR is a real time analog output which tracks the sensed parameter. I/V MONITOR functionality is described in Table 3.

Disable	Mode SEL	I/V Monitor		
1	X	High Impedance		
0	0	Measured Current		
0	1	Measured Voltage		

Table 3.

In the FI / MV mode, the output voltage is a 1:1 mapping of the DUT voltage. In the FV / MI mode, I/V MONITOR follows the equation:

I(measured) = I/V MONITOR / (4.0 \* REXT).

Using nominal values for the external resistors, I/V MONITOR of +8.0V corresponds to Imax and -8.0V corresponds to Imin of the selected current range.



### **Circuit Description (continued)**

#### HIZ

HIZ is a digital input which places the FORCE output into a high impedance state, regardless of the operating mode (forcing current or voltage.) This function allows the PMU to be connected directly to the pin electronics without an isolation relay while NOT adding any leakage current.

#### **DISABLE**

DISABLE is a digital input which places DUT LTH, DUT GTL, I/V MONITOR, and PASS/FAIL\* into high impedance states.

### Force Voltage / Measure Current Mode

In the FV / MI mode, VINP is a high input impedance, analog voltage input that maps directly to the voltage forced at the DUT (see Figure 1), where FORCE = VINP.

A current monitor is connected in series with the Op Amp driving the FORCE voltage. This monitor generates a voltage that is proportional to the current passing through it, and its output is brought out to I/V MONITOR. The monitor's voltage may also be evaluated using the Window Comparator whose operation is in accordance with the FV/MI functional truth table (Table 6).

I/V MAX and I/V MIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator (see Table 4). In the FV / MI mode, a maximum voltage input corresponds to at least a maximum current output. Positive current is defined as current flowing out of the PMU.

I/V MAX I/V MIN	Comparator Threshold
+8.0V	> Imax (full scale)
0V	0
-8.0V	< Imin (full scale)

Table 4.

The voltage at I/V MONITOR follows the equation: I(measured) = I/V MONITOR / (4.0 \* REXT).

Nominally, the external resistors (RA, RB, RC, and RD) should be chosen such that Imax \* REXT = 2.0V.

#### Force Current / Measure Voltage Mode

In the FI / MV mode, IVIN is a high input impedance, analog voltage input that is converted into a current (see Table 5) using the following relationship:

FORCE = 
$$IVIN / (4.0 * REXT)$$

where positive current is defined as current flowing out of the PMU.

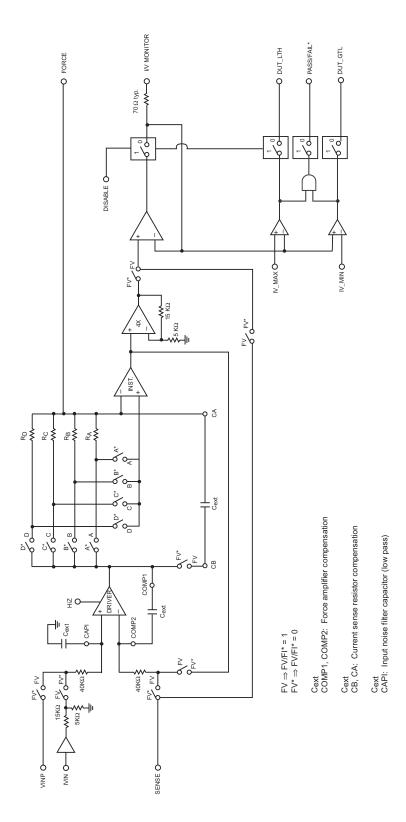
IVIN	Forced Current
+8.0V	Imax (full scale)
0V	0
-8.0V	lmin (full scale)

Table 5.

The resulting DUT voltage is then tested via the SENSE input by a window comparator, whose functional truth table is shown in Table 7.

I/V MAX and I/V MIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator. In the FI / MV mode, the reference inputs translate 1:1 to SENSE level thresholds.

### Circuit Description (continued)



Edge 737 Functional Schematic

Figure 1. E737 Functional Schematic



## **Circuit Description (continued)**

TEST CONDITION	DISABLE	DUT LTH	DUT GTL	I/V MONITOR	PASS/FAIL*
X	1	HiZ	HiZ	HiZ	
I/V MONITOR > I/V MAX I/V MONITOR < I/V MAX	0 0	0 1	N/A N/A	I/V MONITOR = lout * 4.0 * REXT I/V MONITOR = lout * 4.0 * REXT	0 N/A
I/V MONITOR > I/V MAX I/V MONITOR < I/V MAX	0 0	N/A N/A	1 0	I/V MONITOR = lout * 4.0 * REXT I/V MONITOR = lout * 4.0 * REXT	N/A 0
I/V MONITOR < I/V MAX and I/V MONITOR > I/V MAX	0	1	1	I/V MONITOR = lout * 4.0 * REXT	1

Table 6. FV/MI Truth Table

TEST CONDITION	DISABLE	DUT LTH	DUT GTL	I/V MONITOR	PASS/FAIL*
X	1	HiZ	HiZ	HiZ	
SENSE > I/V MAX SENSE < I/V MAX	0 0	0 1	N/A N/A	I/V MONITOR = SENSE I/V MONITOR = SENSE	0 N/A
SENSE > I/V MIN SENSE < I/V MIN	0 0	N/A N/A	1 0	I/V MONITOR = SENSE I/V MONITOR = SENSE	N/A 0
DUT < I/V MAX and DUT > I/V MAX	0	1	1	I/V MONITOR = SENSE	1

Table 7. FI / MV Truth Table



## **Circuit Description (continued)**

#### **REXT Selection**

The E737 is designed for the voltage drop across RA, RB, RC, and RD to be ≤2V with the maximum current passing through them. However, these resistor values can be changed to support different applications.

Increasing the maximum current beyond the nominal range is not recommended. However, decreasing the maximum current is allowed.

#### **Short Circuit Protection**

The E737 is designed to survive a direct short circuit to any voltage within the supply rails at the FORCE and SENSE pins.

#### **Transient Clamps**

The E737 has on-board clamps to limit the voltage and current spikes that might result from either changing the current range or changing the operating mode.

#### **Common Mode Error/Calibration**

In order to attain a high degree of accuracy in a typical ATE application, offset and gain errors are accounted for through software calibration. When forcing or measuring a current with the E737, an additional source of error, common mode error, should be accounted for. Common mode error is a measure of how the common mode voltage,  $V_{\text{CM}}$ , at the input of the current sense amplifier affects the forced or measured current values (see Figure 2). Since this error is created by internal resistors in the current sense amplifier, it is very linear in nature.

Using the common mode error and common mode linearity specifications, one can see that with a small number of calibration steps (see Applications note PMU-A1), the effect of this error can be significantly reduced.

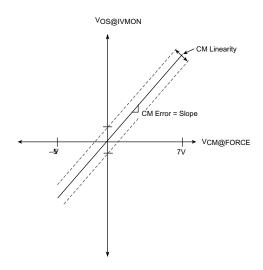


Figure 2. Graphical Representation of Common Mode Error

#### **Compensation Capacitors**

COMP1 and COMP2 are internal op amp compensation pins that require a 120 pF capacitor connected between the two pins.

CAPI is an external noise compensation pin that can be used as a low pass filter to eliminate noise from the IVIN and VINP input pins through the connection of an external capacitor from CAPI to GND. The relationship between the roll-off frequency of noise filtered (in Hz) to the external capacitance (in farads) can be seen below:

Filter Frequency = 
$$\frac{1}{80,000 \pi \times C_{CAPI}}$$

CA and CB are internal compensation pins that require a 120 pF capacitor connected between them.

#### **Power Supply Sequencing**

In order to help protect the E737 from a latch-up condition, it is important that VCC All Input Voltages  $\geq$  VEE, and VCC  $\geq$  GND  $\geq$  VEE at all times.



### **Application Information**

# FORCE Pin Output Voltage (Positive Headroom Requirement)

The maximum positive voltage that can be forced at the FORCE pin by the Edge 737 in the force voltage/measure current (FV/MI) mode and the maximum compliance voltage that can appear at the FORCE pin in the force current/measure voltage mode (FI/MV) is a function of the positive power supply (VCC), device case temperature (Tc), and selected current range. The plot in Figure 3 depicts the typical positive voltage that can appear at the FORCE pin for various power supply combinations across the specified case temperature range of the device. All plots represent the Edge 737 being used with a  $\pm$  2V full-scale swing across the external current sense resistors for each range.

#### **E737 FORCE Voltage Positive Headroom**

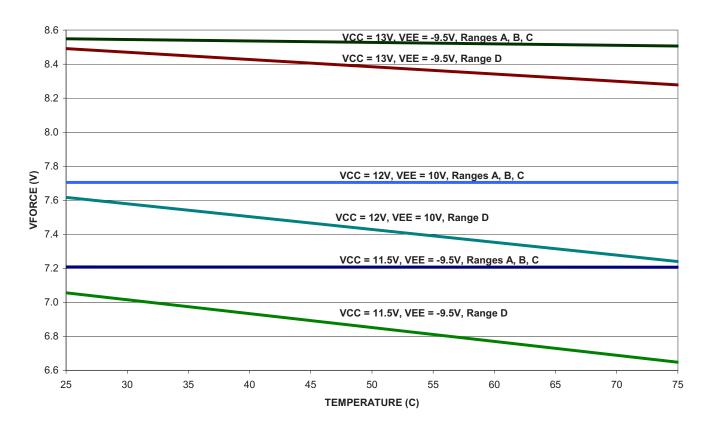
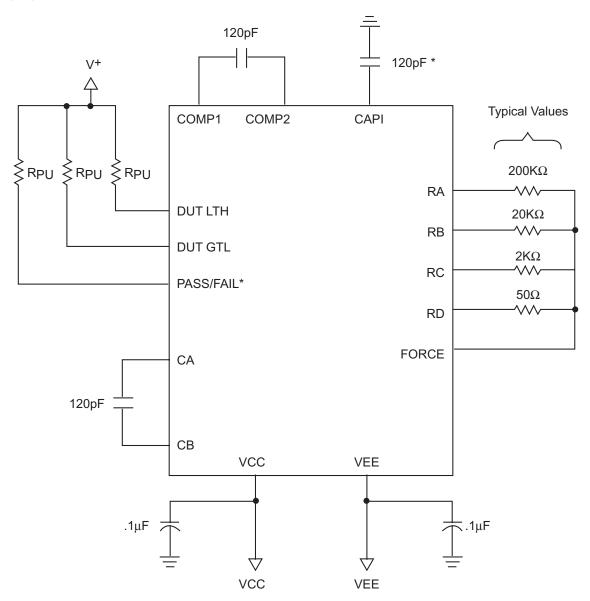


Figure 3. Typical E737 FORCE Pin Voltage vs. Case Temperature

### **Application Information (continued)**

#### **Required External Components**

Choose Rext such that:  $Iout (Iow) = V^+ / RPU < 1mA, V^+ \le VCC$ 



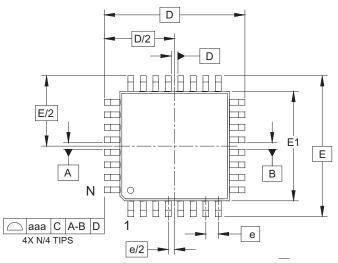
<sup>\*</sup> Optional (see Compensation Capacitors Section)

Actual decoupling capacitor values depend on the actual system environment.



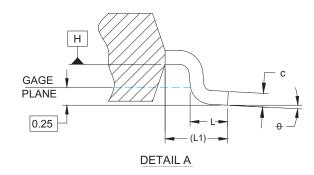
## Package Information

### 32 Pin LQFP Package 7 mm x 7 mm x 1.4 mm



	SEE DETAIL A
A A2	SEATING PLANE
bxN →	O

	DIMENSIONS						
DIM.	INCHES			MILLIMETERS			
DIW.	MIN	NOM	MAX	MIN	NOM	MAX	
Α	.055	-	.063	1.40	-	1.60	
A1	.002	-	.006	0.05	-	0.15	
A2	.053	.055	.057	1.35	1.40	1.45	
b	.012	-	.018	0.30	-	0.45	
С	.004	-	.008	0.09	-	0.20	
D		354 BS0	5	9.00 BSC			
D1	.272	.276	.280	6.90	7.00	7.10	
Е		354 BS0	0	9.00 BSC			
E1	.272	.276	.280	6.90	7.00	7.10	
е		031 BS0	0	0.80 BSC			
L	.018	.024	.030	0.45	0.60	0.75	
L1		(.039)			(1.00)		
N		32			32		
θ	0-7°				0-7°		
aaa	.008				0.20		
bbb	.003			0.08			
CCC		.003			0.08		



#### NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DATUMS -A- , -B- AND -C- TO BE DETERMINED AT DATUM PLANE -H-.
- 3. DIMENSIONS "E1" AND "D1" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 4. REFERENCE JEDEC MS-026, VARIATION BBA.



### **Absolute Maximum Ratings**

Parameter	Symbol	Min	Тур	Max	Units
Positive Power Supply	VCC	0		14	V
Negative Power Supply	VEE	-13		0	V
Total Power Supply	VCC – VEE	0		23	V
Digital Inputs		-0.5		7	V
Storage Temperature	TS	-55		150	${\mathfrak C}$
Junction Temperature	TJ	-65		150	${\mathfrak C}$
Soldering Temperature				260	${\mathfrak C}$

Stresses above listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## **Recommended Operating Conditions**

Parameter	Symbol	Min	Тур	Max	Units
Positive Analog Power Supply (Relative to GND)	VCC	11.5	12	13	V
Negative Analog Power Supply (Relative to GND)	VEE	-11	-10	-9.5	V
Total Analog Power Supply	VCC – VEE	21	22	22.5	V
Case Temperature	TC	25		75	C
Junction Temperature	TJ			125	C
Thermal Resistance of Package (Junction to Case)	θЈС		14.1		€\M

Production tested @ +12V, -10V for linearity and min/max parametric testing.



## **DC Characteristics**

Description	Symbol	Min	Тур	Max	Units
Power Supplies					
Power Supply Consumption Positive Supply (no-load) Negative Supply (no-load) Positive Supply Breakdown (Note 1) Positive Supply Rejection (Note 1) Negative Supply Breakdown (Note 1) Negative Supply Rejection (Note 1)	ICC IEE ICCB AICC IEEB AIEE	3 -11 3 0 -55 -3	5 -5	11 -3 11 3 -42 0	mA mA mA mA mA
Power Supply Rejection Ratio (Note 2) VCC/VEE to FORCE 0.1 kHz 1.0 kHz 10 kHz 100 kHz	PSRR		65 60 50 20		dB dB dB dB
VCC/VEE to I/V MONITOR  0.1 kHz  1.0 kHz  10 kHz  100 kHz  100 kHz (MI Mode)  100 kHz (MV Mode)			65 60 50 1.5 15		dB dB dB dB
Force Voltage/Measure Current Mode					
Input Voltage Range @ VINP Input Bias Current @ VINP Capacitive Loading Range @ FORCE for Stability Output Forcing Voltage Range	VINP IBIAS C <sub>FORCE</sub> V <sub>FORCE</sub>	VEE + 4 -0.4 0 VEE + 4.5		VCC - 4 0.4 12 VCC - 5.0	V µA nA V
Forcing Voltage Accuracy (@ FORCE) Offset (VINP = 0V, no load) Linearity Gain	VOS FV INL FV Gain	-100 -0.025 -0.985	1	100 0.025 1.015	mV % FSVR V/V
FORCE/SENSE Combined Leakage Current in HiZ Mode	I <sub>LEAK</sub>	-20		20	nA
Compliance Current Measurement Range Range A Range B Range C Range D		-10 -100 -1 -40		10 100 1 40	μΑ μΑ mA mA
Current Measurement Accuracy (@ I/V MONITOR) Offset Linearity (Note 3) Gain (Note 4) Common Mode Error Common Mode Linearity I/V MONITOR Output Leakage Current in Disable Mode	VOS MI INL MI Gain CM Error ΔCM Error I <sub>LEAK</sub>	-400 -0.122 3.94 -10 -10.5 -150	4	400 0.122 4.06 10 10.5 150	mV % FSCR V/V mV/V mV nA
	I <sub>LEAK</sub>	-150		150 12	



## DC Characteristics (continued)

Description	Symbol	Min	Тур	Max	Units
Force Current/Measure Voltage Mode					
Input Voltage Range @ IVIN Input Bias Current @ IVIN Capacitive Loading Range @ FORCE for Stability	IVIN IBIAS C <sub>FORCE</sub>	-9.0 -0.4		+9.0 0.4 12	V μA nF
Output Forcing Current Range A Range B Range C Range D	I <sub>FORCE</sub>	-10 -100 -1 -40		10 100 1 40	μΑ μΑ mA mA
Forcing Current Accuracy (@ FORCE) Offset Gain (Note 5) Linearity @ FORCE = -5V to 7V Common Mode Error Common Mode Linearity FORCE/SENSE Combined Leakage Current in HiZ Mode	IOS FI Gain FI INL ICM Error ΔCM Error I <sub>LEAK</sub>	-4 0.24 -0.35 -0.075 -0.1 -20	0.25	4 0.26 0.35 0.075 0.1 20	% FSCR V/V % FSCR % FSCR/V % FSCR nA
Compliance Voltage Range Voltage Measurement Accuracy (@ I/V MONITOR) Offset Gain Linearity (Note 3)	V <sub>COMPLIANCE</sub> VOS MV Gain MV INL	-100 0.985 -0.025	1	100 1.015 0.025	V mV V/V % FSVR
I/V MONITOR Output Leakage Current in Disable Mode	I <sub>LEAK</sub>	-150		150	nA
Capacitive Loading Range @ I/V MONITOR	C <sub>I/V MONITOR</sub>			12	nF
Comparator Input Voltage Range (I/V MIN, I/V MAX)	VIN	VEE + 1		VCC - 3	V
Input Offset Voltage Input Bias Current (I/V MIN, I/V MAX)	VOS IIN	-100 -0.4		100 0.4	mV μA
Output Low Level @ IOL = 1mA (DUT LTH, DUT GTL, PASS/FAIL*)	VOL	-0.4		400	mV
Output Leakage in DISABLED Mode	IOH	-1		1	μΑ
Output Leakage in DISABLED Mode DISABLE Input Bias Current	I <sub>LEAK</sub> IIN	-0.2 -0.2		0.2 0.2	μA μA



### **DC Characteristics (continued)**

Description	Symbol	Min	Тур	Max	Units
Analog MUX (RS1, RS2)					
Input High Level	VIH	2.4			V
Input Low Level	VIL			0.8	V
Input Bias Current	IIN	-0.2		0.2	μΑ
Other Digital Inputs					
Input High Level (MODE SEL, HiZ)	VIH	2.4			V
Input Low Level (MODE SEL, HiZ)	VIL			0.8	V
MODE SEL Input Bias Current	IIN	-0.2		0.2	μΑ
HiZ Input Bias Current	IIN	-1		50	μΑ

DC Test Conditions: CAPI = 120 pF connected to GND, CA – CB = 120 pF, COMP1 – COMP2 = 120 pF, TA =  $25^{\circ}$ C unless otherwise noted.

- Note 1: Test Conditions are as follows: VCC = 12 to 13V, VEE = -10V, 40 mA is externally forced into FORCE pin.
- Note 2: Guaranteed by design and characterization. Not production tested.
- Note 3: Characterized with a ±10 µA current load at I/V MONITOR.
- Note 4: V/V units derived as follows:

MI Gain = 
$$\frac{V_{\text{IVMON}}}{(I_{\text{MEASURED}} \times R_{\text{EXT}})}$$

Note 5: V/V units derived as follows:

FI Gain = 
$$\frac{I_{FORCE} \times R_{EXT}}{V_{IVIN}}$$

#### **Unit Definitions:**

FSCR = Full Scale Current Range

Range A, FSCR = 20  $\mu$ A

Range B, FSCR = 200 µA

Range C, FSCR = 2 mA

Range D, FSCR = 80 mA

FSVR = Full Scale Voltage Range = 12V nominal (-5V to 7V)



## DC Characteristics (continued)

Description	Symbol	Min	Тур	Max	Units
Force Voltage/Measure Current Mode					
FORCE Voltage Settling Time (100pF load @ FORCE) To 0.1% of 10V Step Range A Ranges B, C, D	<sup>‡</sup> settle			150 120	μs μs
To 0.025% of 10V Step All Ranges				300	μs
FORCE Amp Saturation Recovery Time	T <sub>sat</sub>			35	μs
Measure Current Settling Time (100pF load @ I/V MONITOR) To 0.1% of FSCR Range A Ranges B, C, D	t <sub>settle</sub>			400 125	μs μs
To 0.025% of FSCR Range A Ranges B, C, D				1.5 300	ms µs
Disable Time, HiZ Low to High	t <sub>Z</sub>			1	μs
Enable Time, HiZ High to Low	t <sub>oe</sub>			450	ns
Force Current/Measure Voltage Mode					
FORCE Output Current Settling Time (100pF load @ FORCE) To 0.1% of FSCR Range A Ranges B, C, D To 0.025% of FSCR Range A Ranges B, C, D	<sup>†</sup> settle			700 250 2 300	μs μs ms μs
FORCE Amp Saturation Recovery Time	T <sub>sat</sub>			35	μs
Measure Voltage Settling Time (100pF load @ I/V MONITOR) To 0.1% of 10V Step	t <sub>settle</sub>				
Range A Ranges B, C, D				700 250	μs μs
To 0.025% of 10V Step Range A Ranges B, C, D				2 350	ms µs
Disable Time, HiZ Low to High	t <sub>Z</sub>			1	μs
Enable Time, HiZ High to Low	t <sub>oe</sub>			0.45	μs



## **AC Characteristics**

Description	Symbol	Min	Тур	Max	Units
Comparator					
Propagation Delay	tpd			30	μs
Disable Time, DISABLE Low to High	t <sub>Z</sub>			300	ns
Enable Time, DISABLE High to Low	t <sub>oe</sub>			5.5	μs
I/V MONITOR					μs
Disable Time, DISABLE Low to High	t <sub>Z</sub>			350	ns
Enable Time, DISABLE High to Low	t <sub>oe</sub>			40	μs
I/V MONITOR					
MODE SEL Propagation Delay	tpd			10	μs
RS0/RS1 Propagation Delay	tpd			1	μs

AC Test Conditions: CAPI = 120 pF connected to GND, CA - CB = 120 pF, COMP1 - COMP2 = 120 pF, TA = 25 $^{\circ}$ C unless otherwise noted.

Settling times guaranteed by design and characterization (not production tested).



## **Ordering Information**

Model Number	Package
E737ATF	32-Pin LQFP 7mm x 7mm
E737ATFT	32-Pin LQFP 7mm x 7mm Lead Free
EVM737ATF	E737H Evaluation Module



This device is ESD sensitive. Care should be taken when handling and installing this device to avoid damaging it.

## Contact Information

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