

Multiple Output Timing-Safe™ Peak EMI reduction IC

General Features

- Input frequency range: 50MHz to 100MHz
- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Zero input - output propagation delay
- Multiple low-skew outputs
- Output-output skew less than 250pS
- Device-device skew less than 700pS
- One input drives 9 outputs, grouped as 4 + 4 + 1 (PCS5P23Z09C)
- One input drives 5 outputs (PCS5P23Z05C)
- Less than 200 pS cycle-to-cycle jitter
- Available in 16pin 150-mil SOIC, 4.4 mm TSSOP (PCS5P23Z09C), and in 8pin 150-mil SOIC, 4.4mm TSSOP package (PCS5P23Z05C)
- 3.3V operation
- Commercial temperature range
- Advanced 0.35µ CMOS technology
- The First True Drop-in Solution

Functional Description

PCS5P23Z05C/09C is a versatile, 3.3V zero-delay buffer designed to distribute high-speed Timing-Safe™ clocks with Peak EMI reduction. PCS5P23Z09C accepts one reference input and drives out nine low-skew clocks. It is available in a 16-pin package. The PCS5P23Z05C is the eight-pin version of the PCS5P23Z09C. It accepts one reference input and drives out five low-skew clocks.

All parts have on-chip PLLs that lock to an input clock on

the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The PCS5P23Z09C has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding Table. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

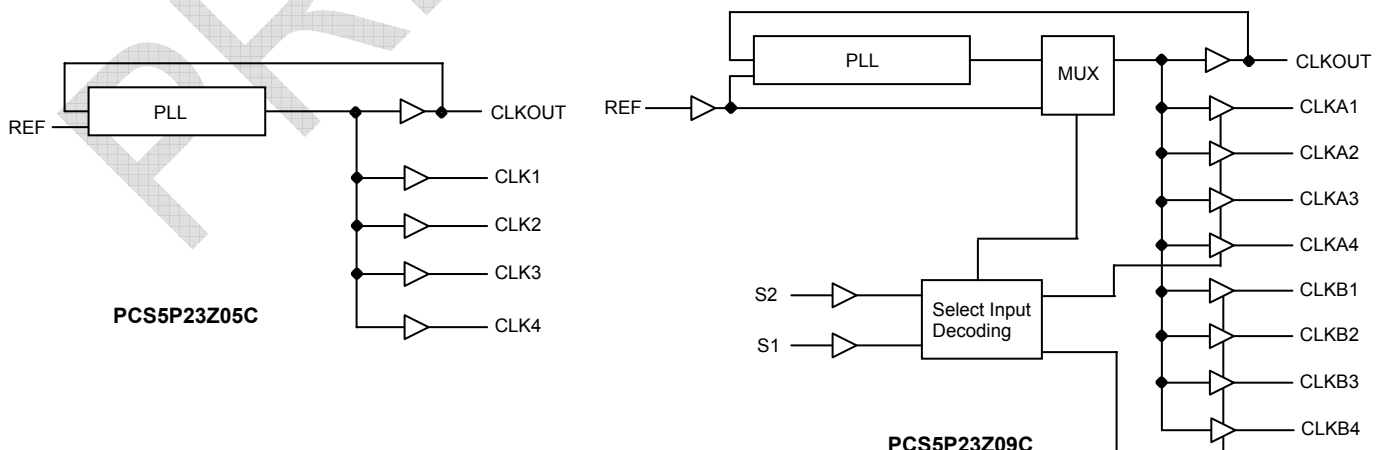
Multiple PCS5P23Z05C/09C devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700pS.

All outputs have less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than ±350pS, and the output to output skew is guaranteed to be less than 250pS.

Refer “Spread Spectrum Control and Input-Output Skew Table” for deviations and Input-Output Skew for PCS5P23Z05C and PCS5P23Z09C devices.

The PCS5P23Z05C/09C is available in two different package configurations, as shown in the ordering information table.

Block Diagram



Select Input Decoding for PCS5P23Z09C

S2	S1	Clock A1 - A4	Clock B1 - B4	CLKOUT ¹	Output Source	PLL Shut-Down
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

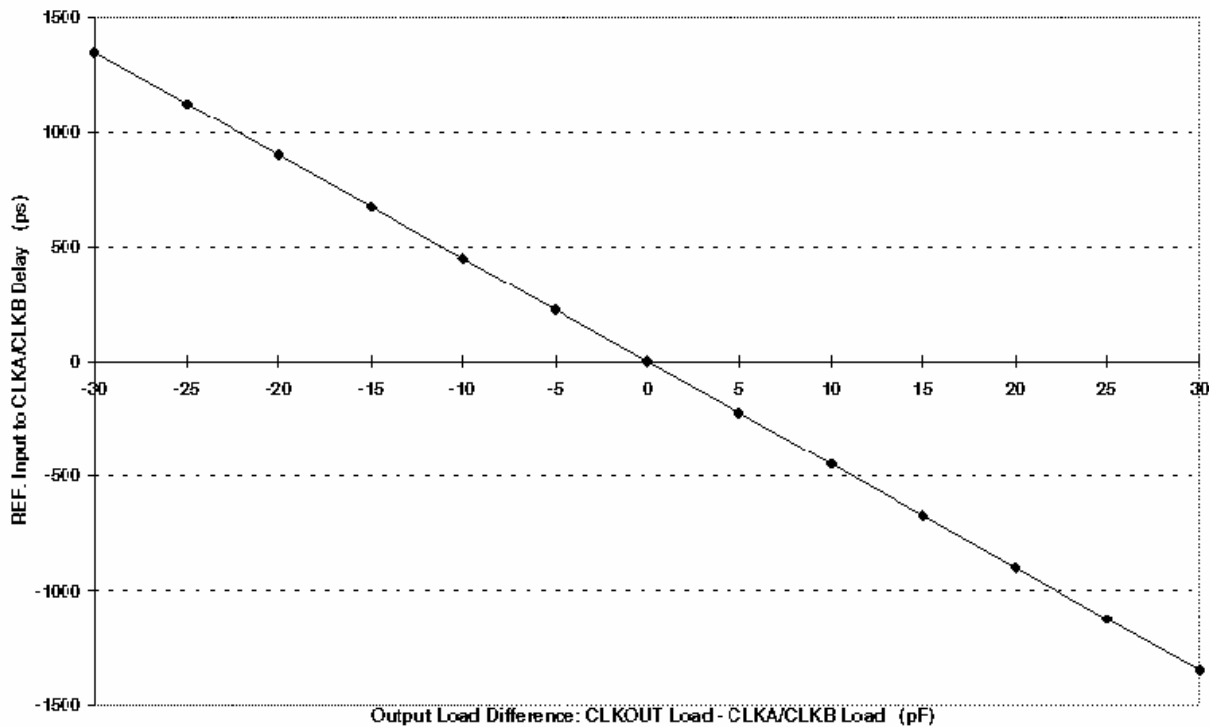
Notes:

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.



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Spread Spectrum Frequency Generation

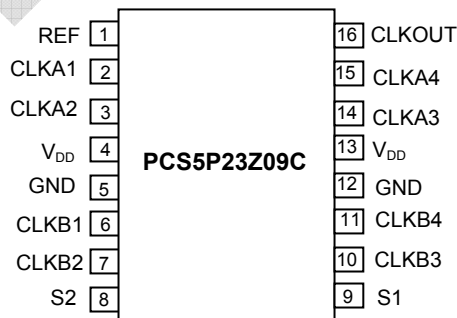
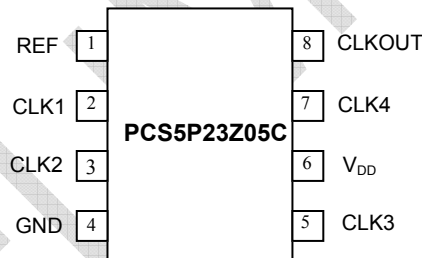
The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of

reducing EMI are to use shielding, filtering, multi-layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The PCS5P23Z05C/09C uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is same as the unmodulated frequency and there is no performance degradation

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration



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Pin Description for PCS5P23Z05C

Pin #	Pin Name	Description
1	REF	Input reference frequency, 5V-tolerant input
2	CLK1 ¹	Buffered clock output
3	CLK2 ¹	Buffered clock output
4	GND	Ground
5	CLK3 ¹	Buffered clock output
6	V _{DD}	3.3V supply
7	CLK4 ¹	Buffered clock output
8	CLKOUT ^{1,2}	Buffered clock output, internal feedback on this pin

Notes: 1. Weak pull-down on these outputs
2. This output is driven and has an internal feedback for the PLL
3. Buffered clock outputs are Timing-Safe™

Pin Description for PCS5P23Z09C

Pin #	Pin Name	Description
1	REF	Input reference frequency, 5V tolerant input
2	CLKA1 ¹	Buffered clock output, bank A
3	CLKA2 ¹	Buffered clock output, bank A
4	V _{DD}	3.3V supply
5	GND	Ground
6	CLKB1 ¹	Buffered clock output, bank B
7	CLKB2 ¹	Buffered clock output, bank B
8	S2 ²	Select input, bit 2
9	S1 ²	Select input, bit 1
10	CLKB3 ¹	Buffered clock output, bank B
11	CLKB4 ¹	Buffered clock output, bank B
12	GND	Ground
13	V _{DD}	3.3V supply
14	CLKA3 ¹	Buffered clock output, bank A
15	CLKA4 ¹	Buffered clock output, bank A
16	CLKOUT ^{1,3}	Buffered output, internal feedback on this pin

Notes: 1. Weak pull-down on these outputs
2. Weak pull-up on these inputs
3. This output is driven and has an internal feedback for the PLL.
4. Buffered clock outputs are Timing-Safe™

Spread Spectrum Control and Input-Output Skew Table

(Note: The values given in the table are for an input frequency of 75MHz)

Device	Deviation	Input-Output Skew($\pm T_{SKEW}$)
PCS5P23Z05C	$\pm 0.5\%$	0.125
PCS5P23Z09C	$\pm 0.5\%$	0.125

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V _{DD}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T _{STG}	Storage temperature	-65 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions for PCS5P23Z05C and PCS5P23Z09C

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	3.0	3.6	V
T _A	Operating Temperature (Ambient Temperature)	0	70	°C
C _L	Load Capacitance		30	pF
C _{IN}	Input Capacitance		7	pF

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Electrical Characteristics for PCS5P23Z05C and PCS5P23Z09C

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V _{IL}	Input LOW Voltage ¹				0.8	V
V _{IH}	Input HIGH Voltage ¹		2.0			V
I _{IL}	Input LOW Current	V _{IN} = 0V			50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}			100	μA
V _{OL}	Output LOW Voltage ²	I _{OL} = 8mA			0.4	V
V _{OH}	Output HIGH Voltage ²	I _{OH} = -8mA	2.4			V
I _{DD}	Supply Current	Unloaded outputs at 66.67MHz			34	mA
Z _o	Output Impedance			23		Ω

Notes:

1. REF input has a threshold voltage of V_{DD}/2
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Characteristics for PCS5P23Z05C and PCS5P23Z09C

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
1/t ₁	Output Frequency	30pF load	50		100	MHz
	Duty Cycle ² = (t ₂ / t ₁) * 100	Measured at 1.4V, F _{OUT} = 66.67MHz	40	50	60	%
t ₃	Output Rise Time ^{1,2}	Measured between 0.8V and 2.0V			2.50	nS
t ₄	Output Fall Time ^{1,2}	Measured between 2.0V and 0.8V			2.50	nS
t ₅	Output-to-output skew ²	All outputs equally loaded			250	pS
t ₆	Delay, REF Rising Edge to CLKOUT Rising Edge ²	Measured at V _{DD} /2		0	±350	pS
t ₇	Device-to-Device Skew ²	Measured at V _{DD} /2 on the CLKOUT pins of the device		0	700	pS
t _J	Cycle-to-cycle jitter ²	Measured at 66.67MHz, loaded outputs			200	pS
t _{LOCK}	PLL Lock Time ²	Stable power supply, valid clock presented on REF pin			1.0	mS

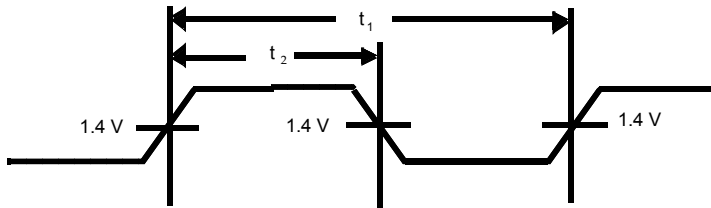
Notes:

1. All parameters specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

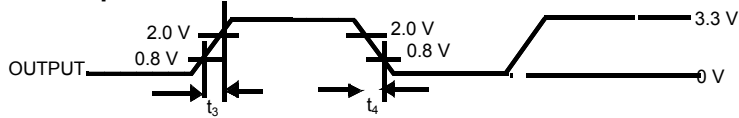
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Switching Waveforms

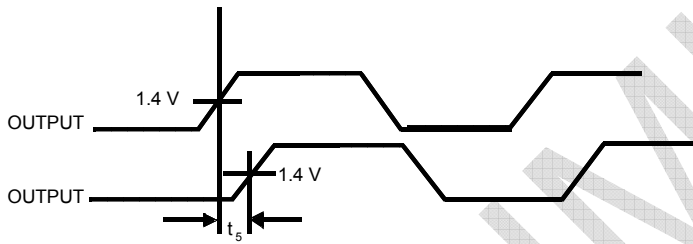
Duty Cycle Timing



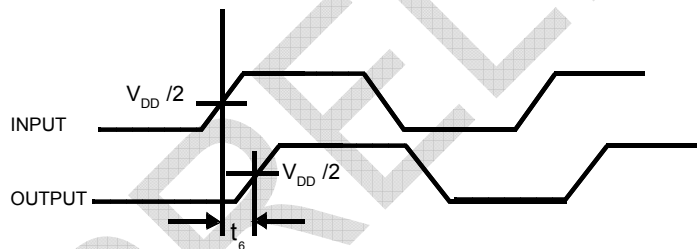
All Outputs Rise/Fall Time



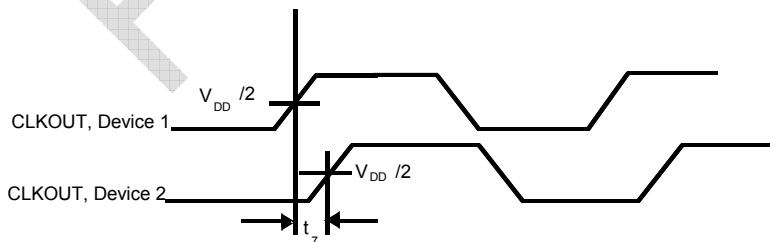
Output - Output Skew



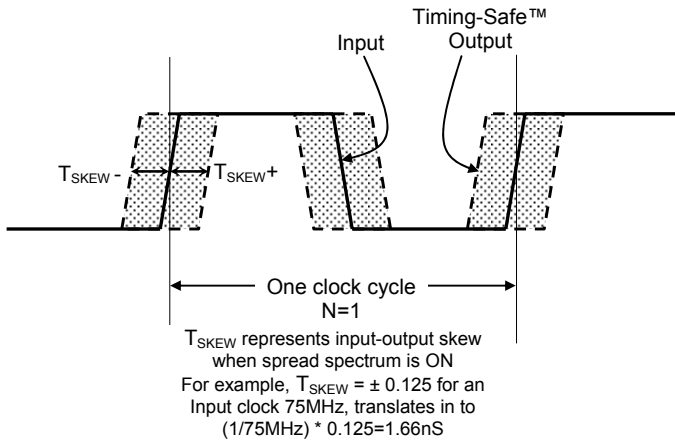
Input - Output Propagation Delay



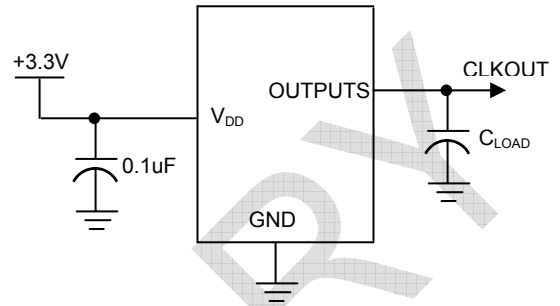
Device - Device Skew



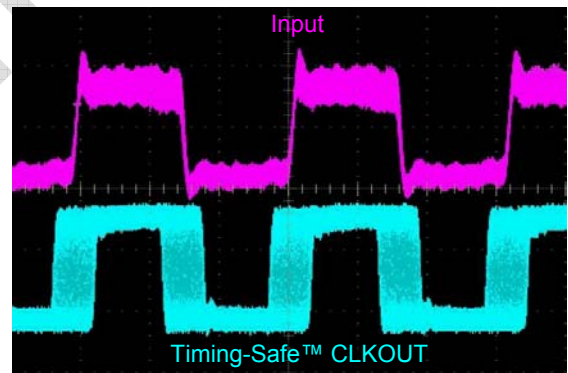
Input-Output Skew



Test Circuit



A Typical example of Timing-Safe™ waveform

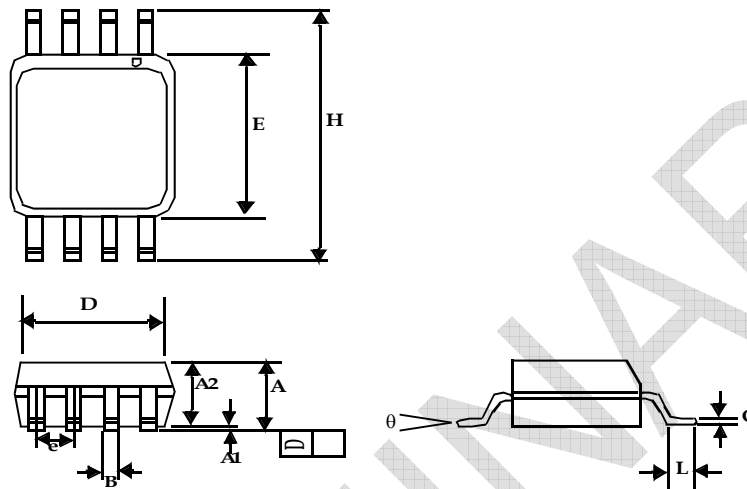


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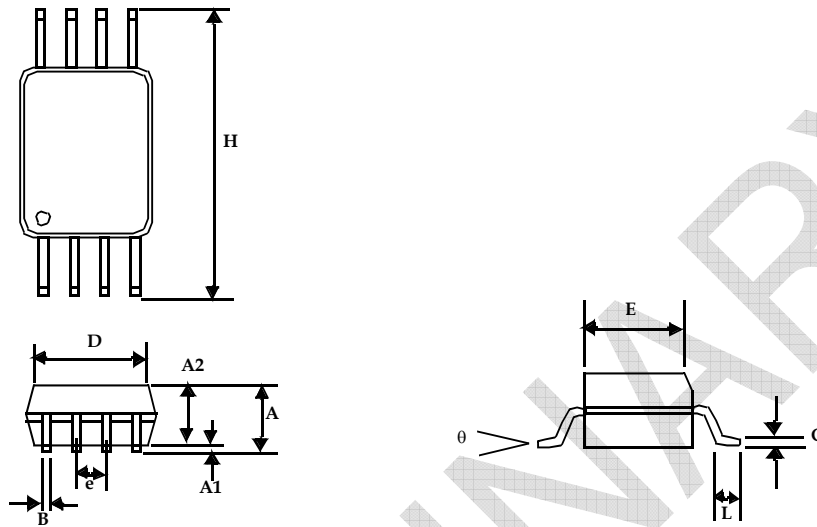
Package Information

8-lead (150-mil) SOIC Package



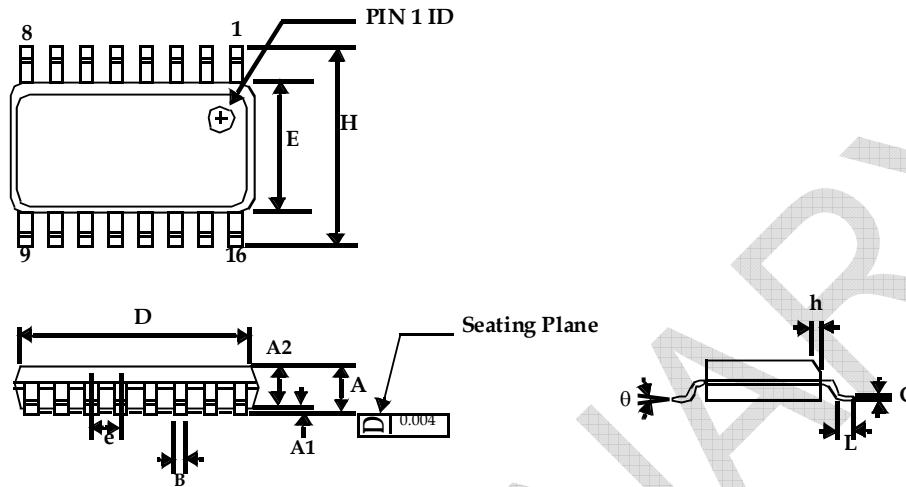
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
theta	0°	8°	0°	8°

8-lead TSSOP Package (4.40-MM Body)



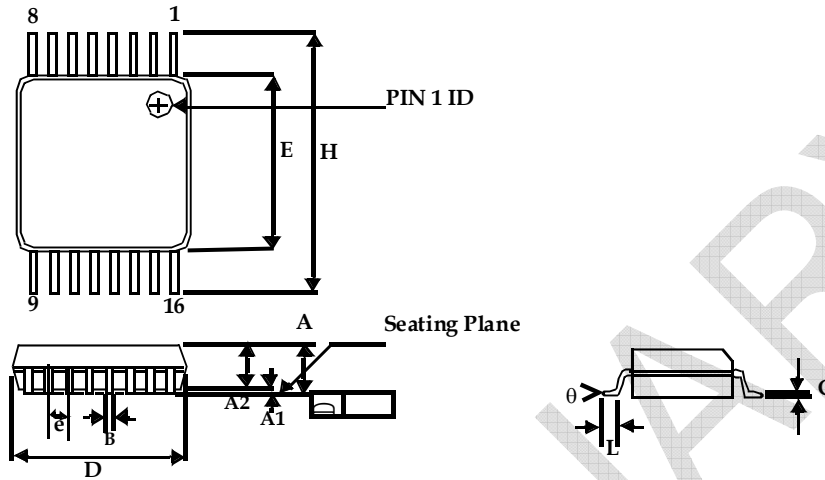
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
theta	0°	8°	0°	8°

16-lead (150 Mil) Molded SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.013	0.022	0.33	0.53
C	0.008	0.012	0.19	0.27
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

16-lead TSSOP Package (4.40-MM Body)



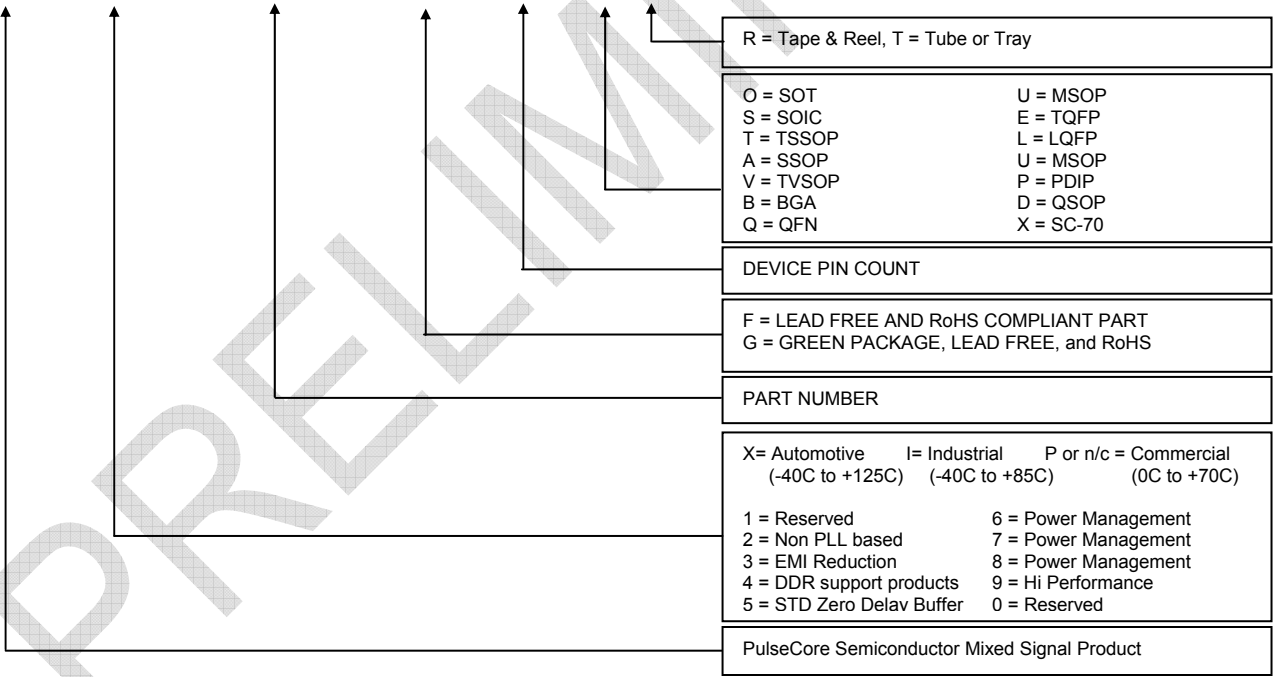
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
theta	0°	8°	0°	8°

Ordering Codes

Ordering Code	Marking	Package Type	Temperature
PCS5P23Z05CG-08-ST	5P23Z05CG	8-pin 150-mil SOIC-TUBE	Commercial
PCS5P23Z05CG-08-SR	5P23Z05CG	8-pin 150-mil SOIC-TAPE & REEL	Commercial
PCS5P23Z05CG-08-TT	5P23Z05CG	8-pin 4.4-mm TSSOP - TUBE	Commercial
PCS5P23Z05CG-08-TR	5P23Z05CG	8-pin 4.4-mm TSSOP - TAPE & REEL	Commercial
PCS5P23Z09CG-16-ST	5P23Z09CG	16-pin 150-mil SOIC-TUBE	Commercial
PCS5P23Z09CG-16-SR	5P23Z09CG	16-pin 150-mil SOIC-TAPE & REEL	Commercial
PCS5P23Z09CG-16-TT	5P23Z09CG	16-pin 4.4-mm TSSOP - TUBE	Commercial
PCS5P23Z09CG-16-TR	5P23Z09CG	16-pin 4.4-mm TSSOP - TAPE & REEL	Commercial

Device Ordering Information

P C S 5 P 2 3 Z 0 5 C G - 0 8 - T R



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



Giving you the edge

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PCS5P23Z09C
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US Patent Pending.

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