TS2GSD150

2GB 150x Secure Digital Card

Description

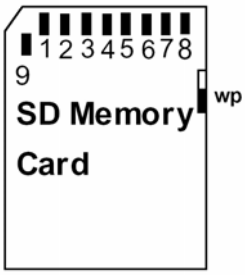
TS2GSD150 is a 2GB Secure Digital Card of 150X ultra-high performance. It is specifically designed to meet the security, capacity, performance and small form factor requirements in newly emerging audio and video consumer electronic devices. Based on dual channel technology and high quality SLC (Single Level Cell) NAND flash chip, TS2GSD150 is the ideal companion to bring out the most from your high-performance electronic devices.

Features

- ROHS compliant product
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Insertion/removal durability: 10,000 cycles
- Fully compatible with SD card spec. v1.1
- Mechanical Write Protection Switch
- Support clock frequencies: 0~50MHz
- Support different Bus width: x1, x4
- Support SD command class 0,2,4,5,7,8
- Supports Copy Protection for Recorded Media(CPRM) for music and other commercial media
- Form Factor: 24mm x 32mm x 2.1mm

Placement

Front

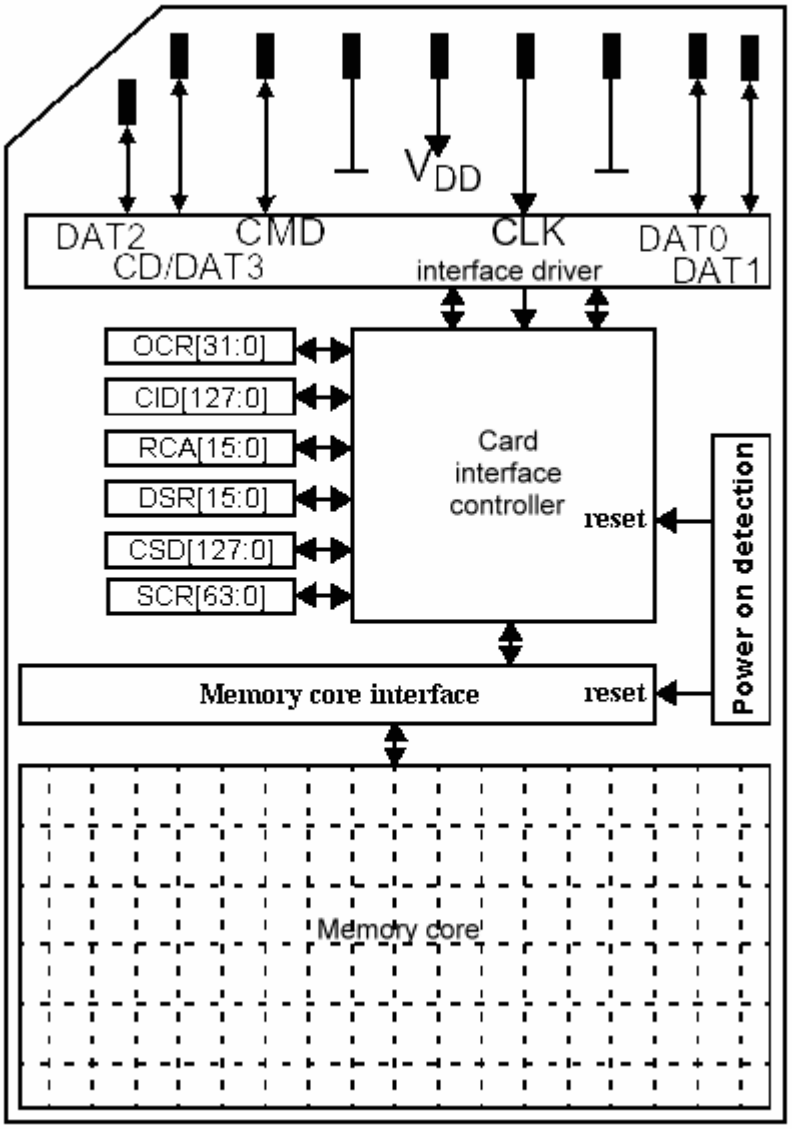


Back

Pin Definition

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT3	I/O/PP	Card Detect/Data Line [Bit3]	CS	I	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit2]	RSV		

Architecture



Bus Protocol

SD bus

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

• **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

• **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

• **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

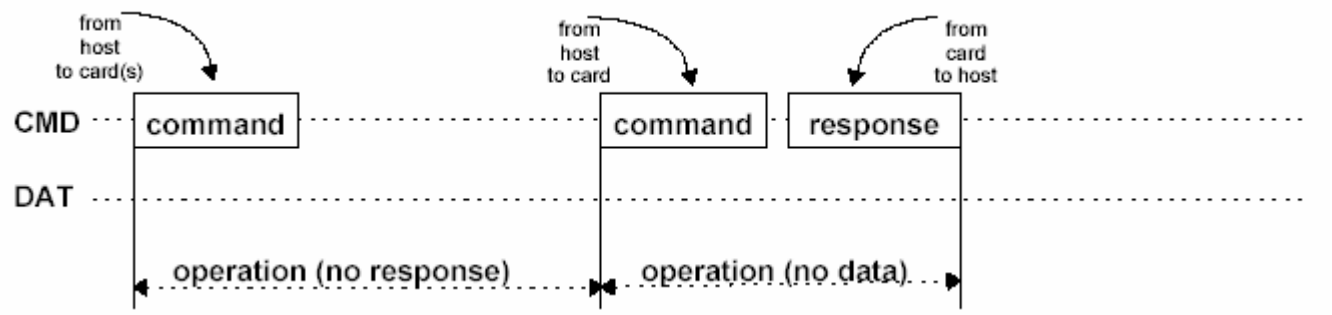


Figure 4: “no response” and “no data” operations

Card addressing is implemented using a session address, assigned to the card during the initializa-tion phase. The basic transaction on the SD bus is the command/response transaction (refer to Figure 4). This type of bus transactions transfer their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Memory Card are done in blocks. Data blocks always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

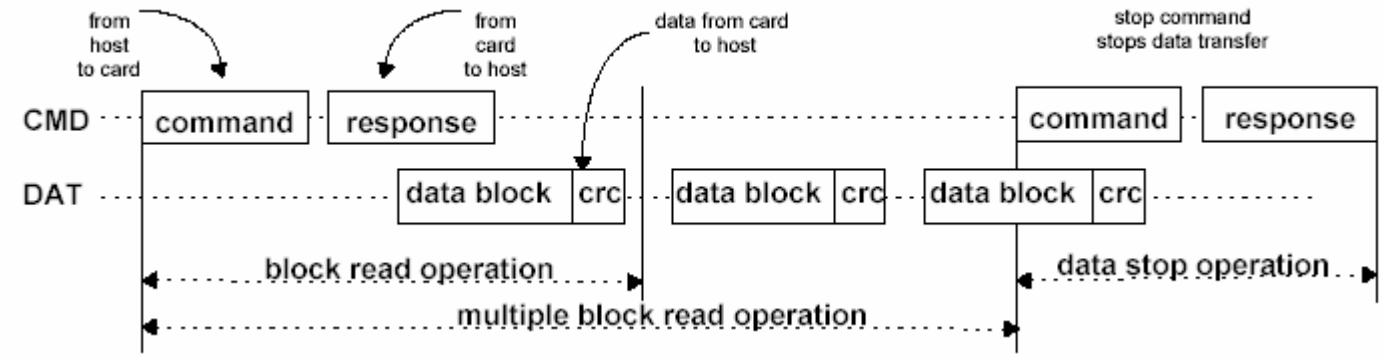


Figure 5: (Multiple) Block read operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 6) regardless of the number of data lines used for transferring the data.

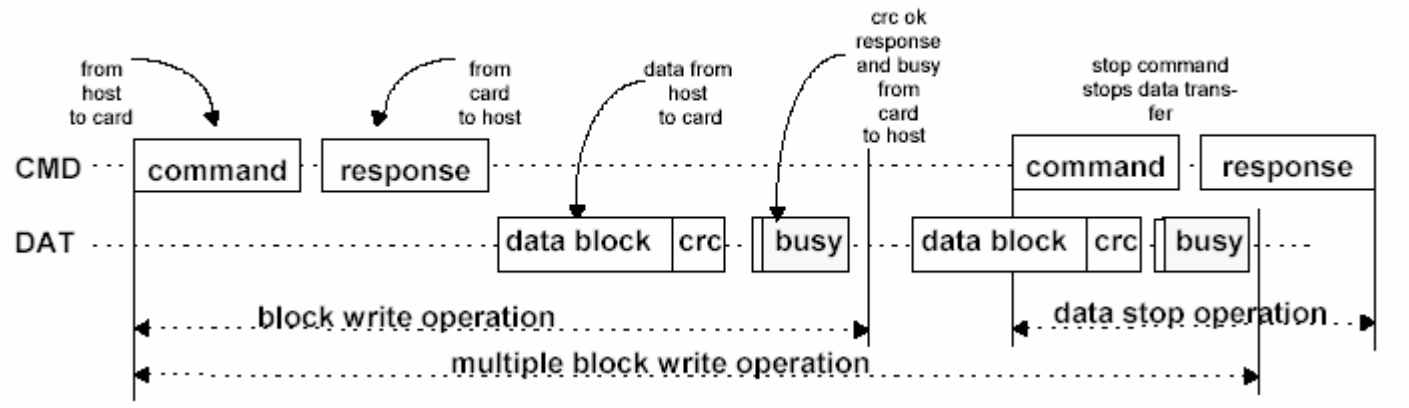


Figure 6: (Multiple) Block write operation

Command tokens have the following coding scheme:

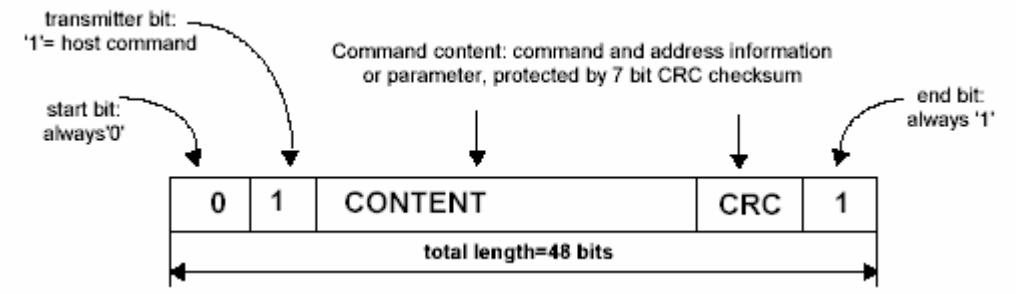


Figure 7: Command token format

Each command token is preceded by a start bit (‘0’) and succeeded by an end bit (‘1’). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated.

Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits.

The CRC protection algorithm for block data is a 16 bit CCITT polynomial.

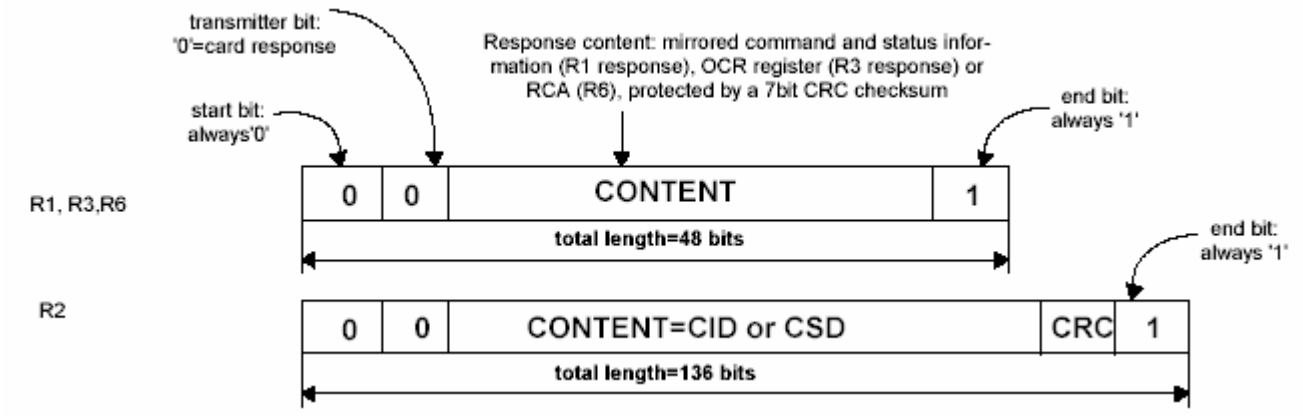


Figure 8: Response token format

In the CMD line the MSB bit is transmitted first the LSB bit is the last.

When the wide bus option is used, the data is transferred 4 bits at a time (refer to Figure 10). Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indica-tion will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).

SPI bus

While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles).

Similar to the SD protocol, the SPI messages consist of command, response and data-block tokens All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low.

The response behavior in the SPI mode differs from the SD mode in the following three aspects:

• The selected card always responds to the command.

• Two new (8 & 16 bit) response structure is used

• When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than by a time-out as in the SD mode.

In addition to the command response, every data block sent to the card during write operations will be responded with a special data response token.

• Data Read

Single and multiple block read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signal are used. Upon reception of a valid read command the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command. A multiple block read operation is terminated, similar to the SD protocol, with the STOP_TRANSMISSION command.

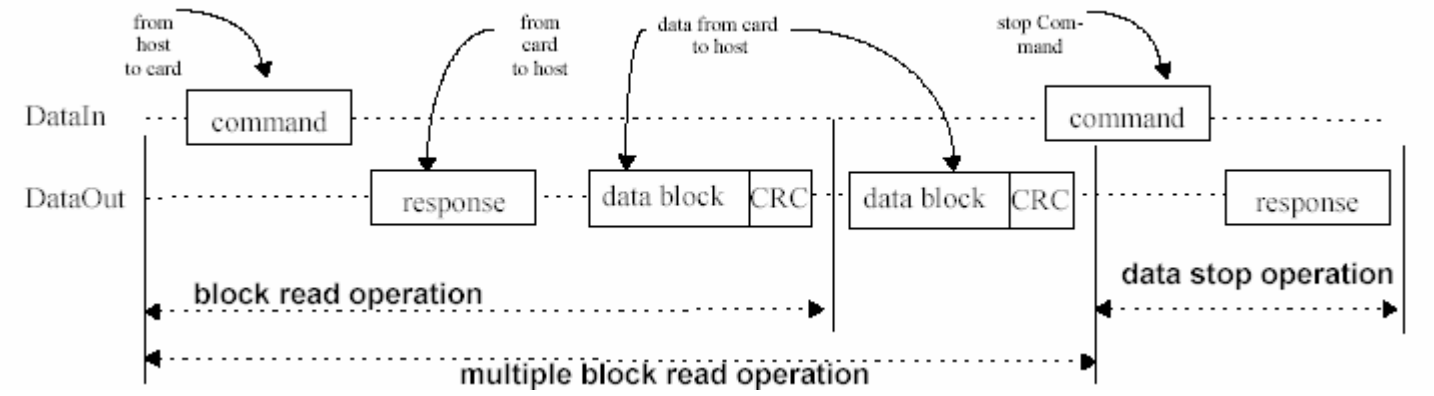


Figure 11: Read operation

A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial $X^{16} + X^{12} + X^5 + 1$.

In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host Figure 12 shows a data read operation which terminated with an error token rather than a data block.

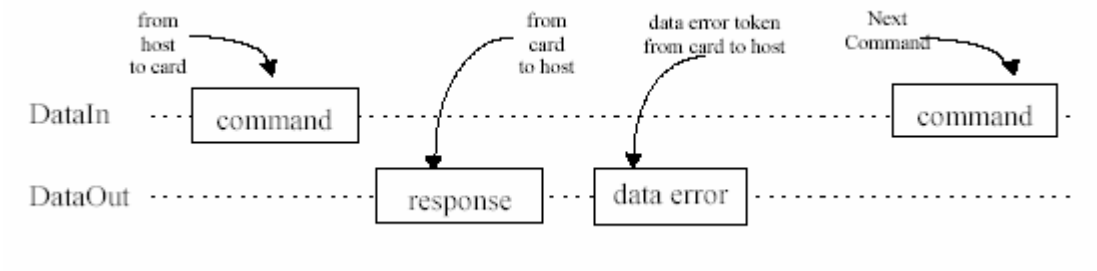


Figure 12: Read operation - data error

• Data Write

Single and multiple block write operations are supported in SPI mode. Upon reception of a valid write command, the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are identical to the read operation (see Figure 13).

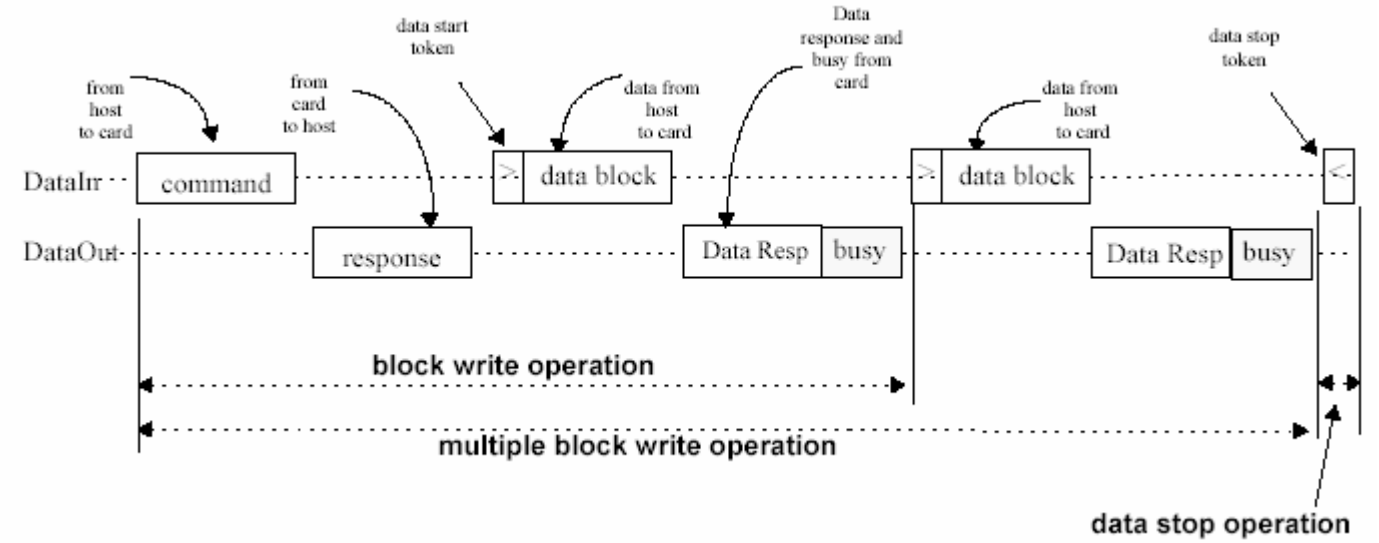


Figure 13: Write operation

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

Card Registers

1. OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by all cards. The supported voltage range is coded as shown in the following table. As long as the card is busy, the corresponding bit (31) is set to LOW.

OCR bit	VDD voltage window	SD
[6:0]	Reserved	000 0000 b
[7]	1.65V – 1.95V	0 b
[14:8]	2.0V – 2.6V	000 0000 b
[23:15]	2.7V – 3.6V	1 1111 1111 b
[30:24]	Reserved	000 0000 b
[31]	Card power status bit	

(1) OCR bit [31] is set to LOW if the card has not finished the power up routine.

2. Card Identification Register (CID)

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash or I/O card shall have an unique identification number. The structure of the CID register is defined in the following
table

CID bit	width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:56]	48	Product Name	PNM
[55:48]	8	Product Revision	PRV
[47:16]	32	Product Serial Number	PSN
[15:8]	8	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used, always '1'	---

3. Driver Stage Register (DSR)

The 16-bit driver stage register is optionally used to improve the bus performance for extended operating conditions.The CSD register carries the information about the DSR register usage. This register is not implemented

4. Relative Card Address Register (RCA)

The writable 16-bit relative card address register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7. In SD mode, the value of this register is generated by random number generator inside the card. Please reference to SD specification for detail information.

5. Card Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register can be changed by CMD27.

CSD bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	00 b	v1.0
[125:120]	6	Reserved	---	---	---
[119:112]	8	Data read access-time 1	TAAC	7F h	80 ms
[111:104]	8	Data read access-time 2	NSAC	FF h	25.5k clocks
[103:96]	8	Max. bus clock freq.	TRAN_SPEED	32 h	25 MHz
[95:84]	12	Card command classes	CCC	1F5 h	(*1)
[83:80]	4	Max. read data block length	READ_BL_LEN	9 h	512 bytes
[79]	1	Partial block read allowed	READ_BL_PARTIAL	1 b	Support
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	1 b	Support
[77]	1	Read block misalignment	READ_BLK_MISALIGN	1 b	Support
[76]	1	DSR implemented	DSR_IMP	0 b	Not support
[75:74]	2	Reserved	---	---	---
[73:62]	12	Device size	C_SIZE	(*2)	(*2)
[61:59]	3	Max. R_curr @ V_{DD} min	VDD_R_CURR_MIN	101 b	35 mA
[58:56]	3	Max R_curr @ V_{DD} max	VDD_R_CURR_MAX	101 b	45 mA
[55:53]	3	Max W_curr @ V_{DD} min	VDD_W_CURR_MIN	101 b	35 mA
[52:50]	3	Max W_curr @ V_{DD} max	VDD_W_CURR_MAX	101 b	45 mA
[49:47]	3	Device size multiplier	C_SIZE_MULT	(*2)	(*2)
[46]	1	Erase single block enable	ERASE_BLK_EN	0 b	Not allowed
[45:39]	7	Erase sector size	SECTOR_SIZE	(*3)	(*3)
[38:32]	7	Write protect group size	WP_GRP_SIZE	(*4)	(*4)
[31]	1	Write protect group enable	WP_GRP_ENABLE	1 b	Support
[30:29]	2	Reserved	---	---	---
[28:26]	3	Write speed factor	R2W_FACTOR	101 b	32X
[25:22]	4	Max. write data block length	WRITE_BL_LEN	9 h	512 bytes
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	1 b	Support
[20:16]	5	Reserved	---	---	---
[15]	1	File format group	FILE_FORMAT_GRP	0 b	HD like FAT

[14]	1	Copy flag	COPY	0 b	Not copied
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0 b	Not protected
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0 b	Not protected
[11:10]	2	File format	FILE_FORMAT	00 b	HD like FAT
[9:8]	2	ECC code	ECC	00 b	None
[7:1]	7	CRC	CRC	---	---
[0]	1	Not used always ‘1	---	1 b	---

(*1) Support command class 0,2,4,5,6,7,8. Include : Basic, Block read/write, Erase, Write protection, application command, and Lock card. Not support 1,3. Include : Stream read/write.

(*2)~(*4) This field is not a constant value. The value will be changed by different flash memory.

6. Extended CSD Register (EXT_CSD)

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command.

7. SD card Configuration Register (SCR)

The CSD register is another configuration register in SD card. SCR provides on SD card s special features that were configured into the given card. The size of SCR is 64 bit.

For SD card only. SCR is a read only register.

SCR bit	Width	Name	Field	Value	Note
[63:60]	4	SCR structure	SCR_STRUCTURE	0000 b	v1.0
[59:56]	4	SD card spec. version	SD_SPEC	0000 b	v1.0
[55]	1	Data status after erase	DATA_STAT_AFTER_ERASE	0 b	Zero after erase
[54:52]	3	SD security support	SD_SECURITY	001 b	Secure-protocol 1.0
[51:48]	4	DAT bus width support	SD_BUS_WIDTH	0101 b	Support 1/4 bit
[47:32]	16	Reserved	---	---	---
[31:0]	32	Reserved	---	---	---

AC/DC Character

• General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55,ACMD41 commands
Supply voltage specified in OCR register		2.7	3.6	V	Except CMD0, 15,55, ACMD41 commands
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up time			250	ms	From 0v to V_{DD} Min.

• Bus Signal Line Load

The total capacitance C_L the CLK line of the SD Memory Card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:
$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$

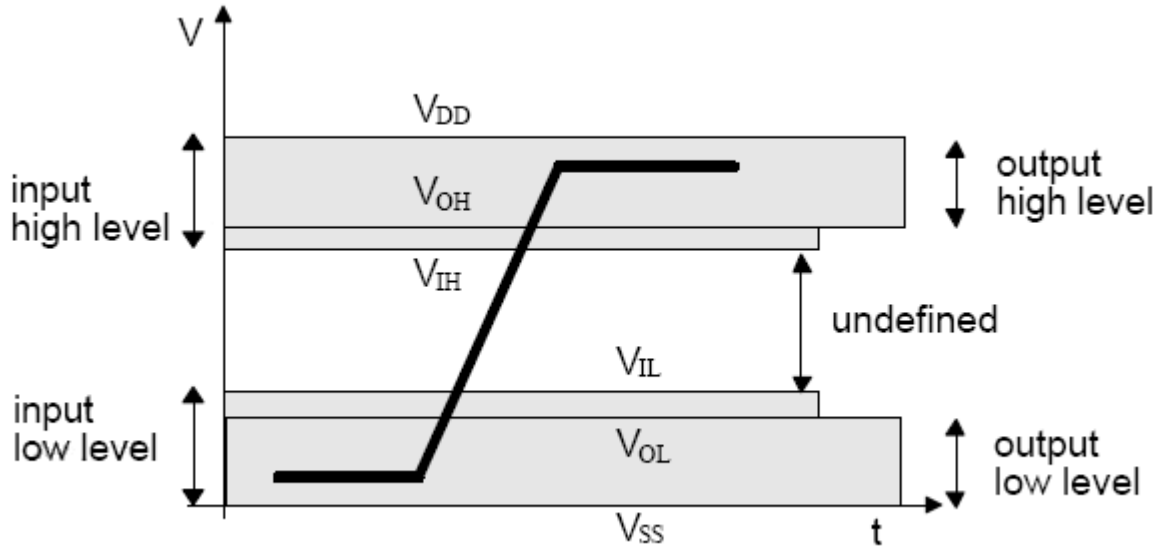
Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 7 cards
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD}, R_{DAT}	10	100	kΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 21 cards

• Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	0.75* V_{DD}		V	I_{OH} = -100 µA @V_{DD} min
Output LOW voltage	V_{OL}		0.125* V_{DD}	V	I_{OL} = -100 µA @V_{DD} min
Input HIGH voltage	V_{IH}	0.625* V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25* V_{DD}	V	

- **Bus Timing (Default)**

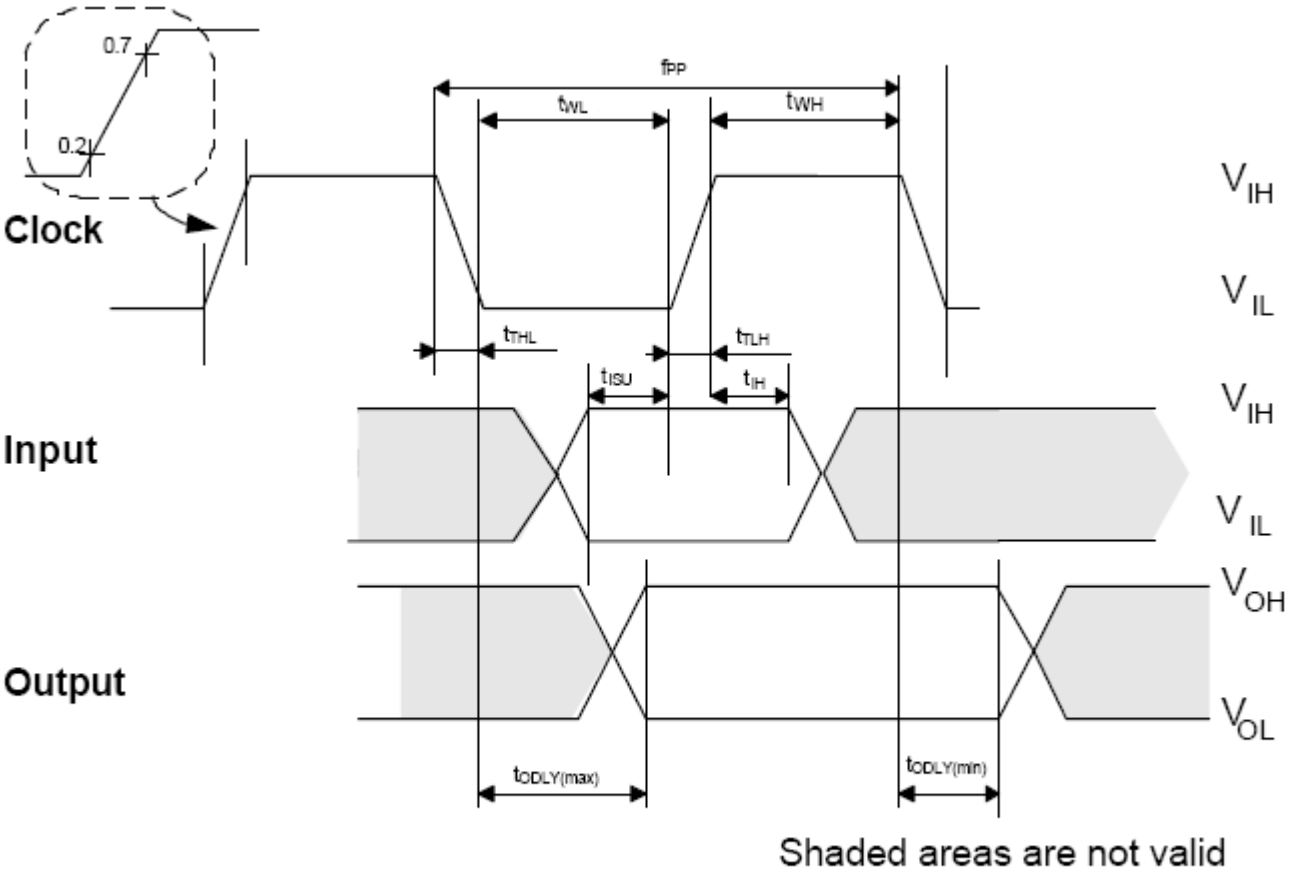


Figure 47: Timing diagram data input/output referenced to clock (Default)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_L \leq 100$ pF, (7 cards)
Clock frequency Identification Mode (The low freq. is required for MultiMediaCard compatibility.)	f_{OD}	0	400	KHz	$C_L \leq 250$ pF, (21 cards)
Clock low time	t_{WL}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock high time	t_{WH}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \leq 100$ pF, (7 cards)

			50	ns	$C_L \leq 250$ pF, (21 cards)
Clock fall time	t_{THL}		10	ns	$C_L \leq 100$ pF, (7 cards)
			50	ns	$C_L \leq 250$ pF, (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_L \leq 25$ pF, (1 cards)
Input hold time	t_{IH}	5		ns	$C_L \leq 25$ pF, (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 25$ pF, (1 cards)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leq 25$ pF, (1 cards)

- **Bus Timing (High Speed Mode)**

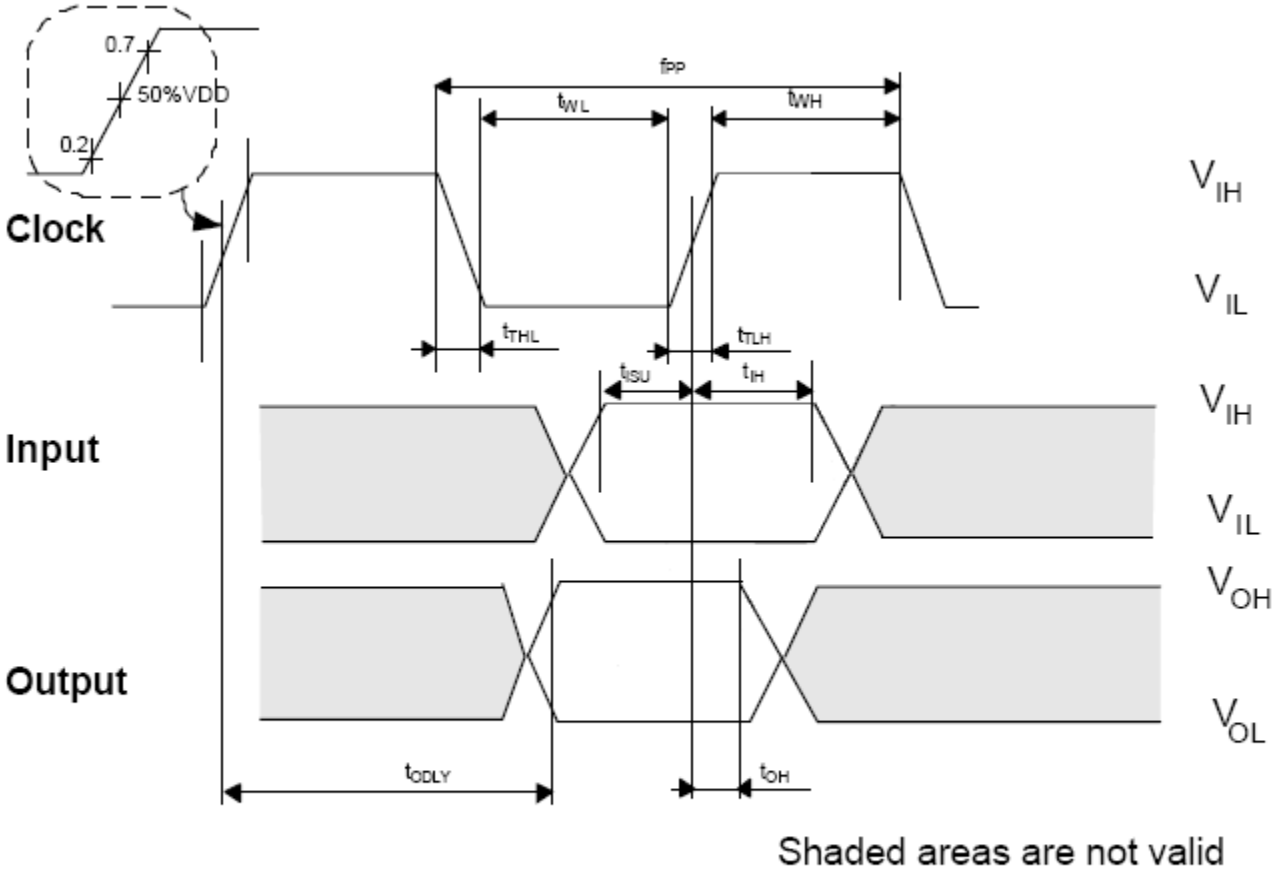


Figure 48: Timing diagram data input/output referenced to clock (High-Speed)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	
Clock low time	t_{WL}	7		ns	
Clock high time	t_{WH}	7		ns	
Clock rise time	t_{TLH}		3	ns	
Clock fall time	t_{THL}		3	ns	
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	
Input hold time	t_{IH}	2		ns	
Outputs CMD, DAT (referenced to CLK)					

Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	
Output Hold time	t_{OH}	2.5		ns	
Total System capacitance for each line	C_L		40	pF	

Reliability and Durability

Temperature	Operation: -25°C / 85°C (Target spec) Storage: -40°C (168h) / 85°C (500h) Junction temperature: max. 95°C
Moisture and corrosion	Operation: 25°C / 95% rel. humidity Storage: 40°C / 93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10.000 mating cycles;
Bending	10N
Torque	0.15N.m or +/-2.5 deg
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO 7816-1
Visual inspection Shape and form	No warp page; no mold skin; complete form; no cavities surface smoothness <= -0.1 mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf
WP Switch cycles	minimum 1000 Cycles(@Slide force 0.4N to 5N)

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