NEC

MOS INTEGRATED CIRCUIT

# μPD99911

## AUDIO PROCESSOR LSI WITH SD CARD INTERFACE FOR MOBILE PHONES

### DESCRIPTION

The μPD99911 is an audio processor LSI with CPU and SD memory card interface. This LSI can perform the functions of an SD audio player without host interactions during playback, which helps the system to achieve low power consumption. This LSI also performs audio streaming playback. It supports not only MP3 but also AAC decoding.

### FEATURES

- High performance on-chip digital signal processor for the following functions.
  - Decoder: MP3, WMA, AAC, HE-AAC, Enhanced aacPlus
  - AGC (Automatic Gain Controller)
  - SRC (Sampling Rate Converter)
  - 5-band PEQ (Parametric Equalizer)
- SD memory card interface with CPRM function
- 2 sets of audio serial I/O interface (16 bits stereo) provided. The serial data input frequency is variable from 32 fs to 128 fs in the slave mode. I2S is supported.
- 16-bit parallel host interface
- 8 general-purpose on-chip output ports
- Programmable PLL on-chip for 32.768 kHz input clock, such as an RTC clock.
- Power management system on-chip
  - Operation mode
  - Sleep mode (resume data of memory and register)
  - Transparency mode (direct connection between ASIO1 and ASIO2)
  - Deep sleep mode
- Power supply voltages:
  - EVDD: 1.7 to 2.0 V
  - DVDD: 1.16 to 1.24 V
  - PLLVDD: 1.16 to 1.24 V
  - SDVDD: 1.7 to 3.0 V

### ORDERING INFORMATION

| | Part number | Package |
|---|---|---|
| <R> | μPD99911F1-BAC-A | 97-pin plastic FBGA (6 × 6) |

**Remark** A lead-free product.



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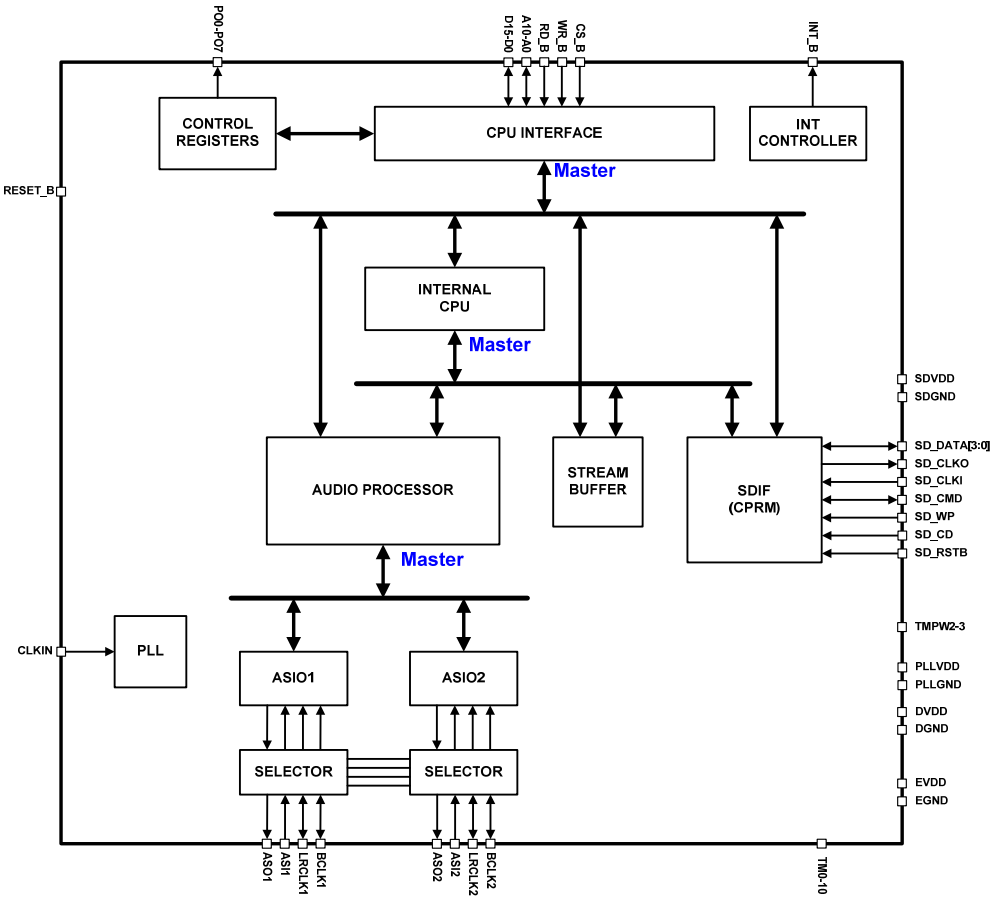
**The mark <R> shows major revised points.**



**The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.**

## BLOCK DIAGRAM AND FUNCTIONS




**(1) Audio processor**

The LSI contains a high-performance digital signal processor for decoding and encoding audio. For operation, firmware needs to be downloaded in advance from external memory via a host CPU. The firmware provides the following different configurable functions:

- Audio decoder
  MP3, WMA, AAC, HE-AAC, Enhanced aacPlus
- Sampling rate converter (SRC)
- Volume controller (including soft volume function)
- Automatic gain controller (AGC)
- 5-band parametric equalizer
- Channel controller
  Stereo/mono

**(2) PLL**

Clock input of 32.768 kHz is supported. When a clock with a frequency in this range is input, it is multiplied by the PLL to generate the fixed frequency clock that is required internally. After activation, normal operation begins after at least 2 ms have elapsed.

**(3) General-purpose output (PO0 to PO7)**

The PO0 to PO7 ports can be controlled by the command register.

**(4) Host interface**

16-bit parallel interface is supported for the host interface.

**(5) Audio serial interface (ASIO1 and ASIO2)**

These are two I/O interface lines for external audio serial data communication. The serial data input frequency is variable. The frequency can be selected in 2-bit steps within a range from 32 to 128 bits. The I2S format is available.

It is possible to make a direct connection of ASIO1 and ASIO2 internally (transparency mode). Very low power consumption can be achieved during the transparency mode.

**(6) SD memory card interface**

An SD memory card can be directly connected to the LSI.

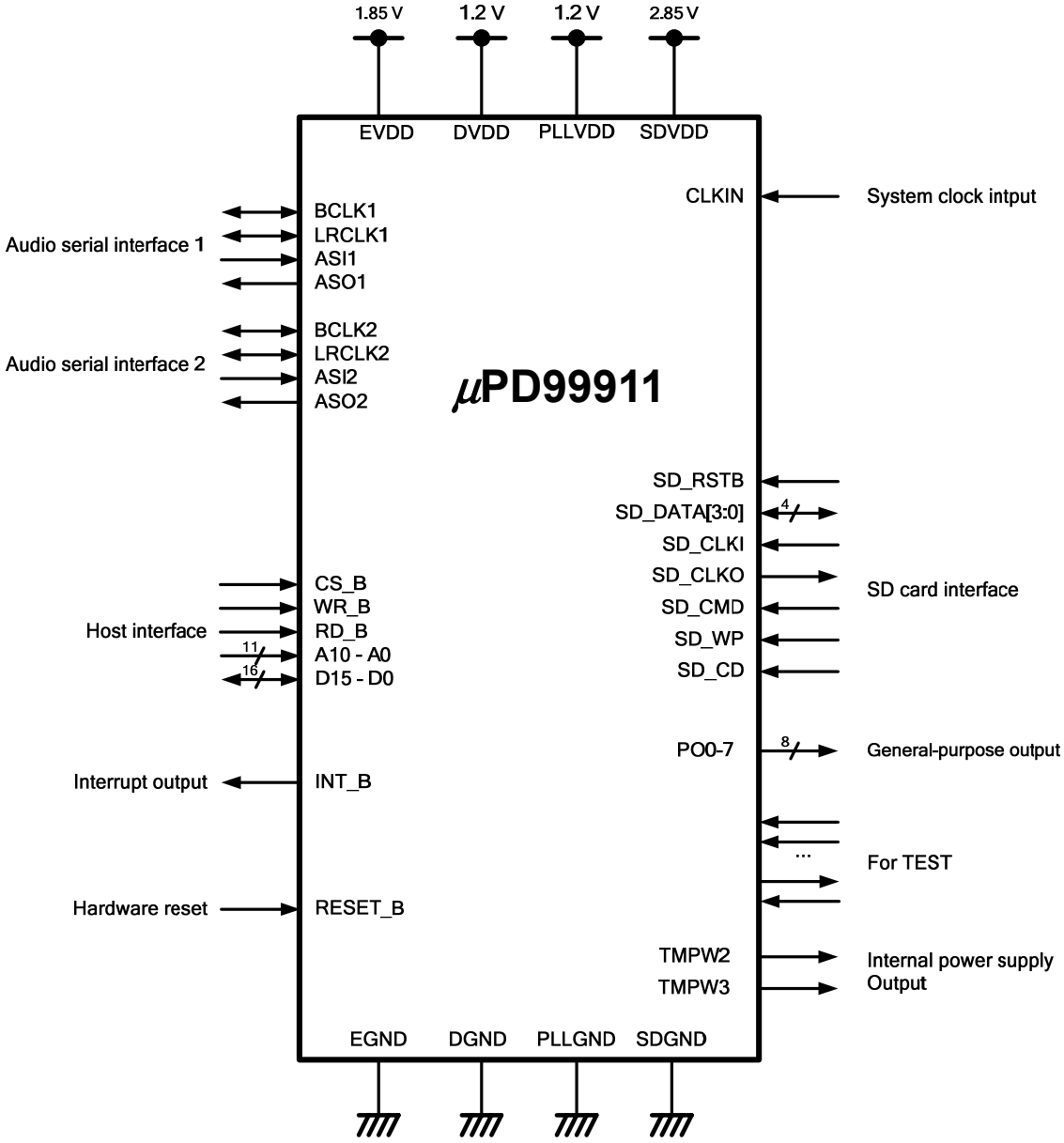
**(7) Power management system**

Power management system is included internally, which provides suitable operation modes for low power consumption.

CONTENTS

## 1. PIN FUNCTIONS

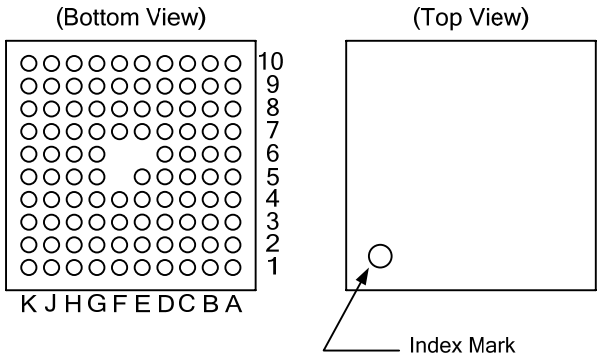
### 1.1 Pin Configuration



### 1.2 Pin Configuration

<R> 97-pin plastic FBGA (6 x 6)

μPD99911F1-BAC-A




| Pin No. | Pin Name |
|---|---|
| A1 | N.C. |
| B1 | EVDD |
| C1 | BCLK1 |
| D1 | DGND |
| E1 | SDVDD |
| F1 | SD_DATA0 |
| G1 | SD_WP |
| H1 | PLLVDD |
| J1 | PLLGND |
| K1 | N.C. |
| A2 | TM10 |
| B2 | EGND |
| C2 | LRCLK2 |
| D2 | ASI1 |
| E2 | TMPW3 |
| F2 | SD_DATA1 |
| G2 | SD_CMD |
| H2 | SD_CD |
| J2 | TM4 |
| K2 | TM3 |
| A3 | WR_B |
| B3 | TM6 |
| C3 | ASO1 |
| D3 | LRCLK1 |
| E3 | SD_RSTB |
| F3 | SD_CLKO |
| G3 | SD_DATA3 |
| H3 | CLKIN |
| J3 | PO0 |
| K3 | PO1 |
| A4 | RD_B |
| B4 | ASO2 |
| C4 | CS_B |

| Pin No. | Pin Name |
|---|---|
| D4 | SD_CLKI |
| E4 | SDGND |
| F4 | SD_DATA2 |
| G4 | DVDD |
| H4 | EGND |
| J4 | PO2 |
| K4 | PO3 |
| A5 | D0 |
| B5 | ASI2 |
| C5 | D1 |
| D5 | DGND |
| E5 | DVDD |
| G5 | DVDD |
| H5 | PO4 |
| J5 | PO5 |
| K5 | PO6 |
| A6 | BCLK2 |
| B6 | D2 |
| C6 | D3 |
| D6 | DVDD |
| G6 | DGND |
| H6 | PO7 |
| J6 | EGND |
| K6 | INT_B |
| A7 | D5 |
| B7 | D4 |
| C7 | D6 |
| D7 | D12 |
| E7 | D15 |
| F7 | TMPW2 |
| G7 | A0 |
| H7 | EGND |
| J7 | RESET_B |

| Pin No. | Pin Name |
|---|---|
| K7 | EVDD |
| A8 | EVDD |
| B8 | EGND |
| C8 | TM5 |
| D8 | D11 |
| E8 | D14 |
| F8 | A9 |
| G8 | A8 |
| H8 | A1 |
| J8 | A3 |
| K8 | A2 |
| A9 | TM7 |
| B9 | TM8 |
| C9 | D8 |
| D9 | D9 |
| E9 | D13 |
| F9 | A10 |
| G9 | A6 |
| H9 | A5 |
| J9 | TM2 |
| K9 | TM1 |
| A10 | N.C. |
| B10 | TM9 |
| C10 | D7 |
| D10 | D10 |
| E10 | DGND |
| F10 | DVDD |
| G10 | A7 |
| H10 | A4 |
| J10 | TM0 |
| K10 | N.C. |

**Caution: Leave the N.C. pins open.**

## 1.3 Pin Functions

### (1) Power supply pins

| Pin Name | I/O | Function |
|---|---|---|
| DVDD | – | Power supply for digital core block<br>Be sure to connect a 0.1 μF capacitor between this pin and DGND. |
| DGND | – | Ground for digital core block |
| EVDD | – | Power supply for I/O<br>Be sure to connect a 0.1 μF capacitor between this pin and EGND. |
| EGND | – | Ground for I/O |
| PLLVDD | – | Power supply for PLL<br>Be sure to connect a 0.1 μF capacitor between this pin and PLLGND. |
| PLLGND | – | Ground for PLL block |
| SDVDD | – | Power supply for SD I/O<br>Be sure to connect a 0.1 μF capacitor between this pin and SDGND. |
| SDGND | – | Ground for SD I/O block |

### (2) Clock and system control pins

| Pin Name | I/O | Function |
|---|---|---|
| CLKIN | Input | Clock input<br>This is the reference clock input that is used to generate the internal master clock. |
| RESET_B | Input | Hardware reset input signal<br>This resets the LSI. Registers are initialized to their initial values after a reset. |

### (3) Host interface pins

| Pin Name | I/O | Function |
|---|---|---|
| A0 to A10 | Input | Host interface address signal input |
| D0 to D15 | I/O | Host data bus (D15 to D0).<br>Data I/O is performed when the host CPU accesses this LSI.<br>This bus is set to high impedance when the CS_B signal is inactive (high). |
| CS_B | Input | Chip select strobe input<br>This is the input pin for the host interface select signal. This pin must be active (low) while the host CPU accesses a host interface register. |
| WR_B | Input | Host write strobe input<br>This pin must be active (low) while the host CPU writes to a host interface register. Do not set this pin and the RD_B pin as active at the same time. |
| RD_B | Input | Host read strobe input<br>This pin must be active (low) while the host CPU reads a host interface register. Do not set this pin and the WR_B pin as active at the same time. |
| INT_B | Output | Interrupt request (Level trigger)<br>This is used to request data transfer or to notify the internal status. |

**(4) Audio serial interface 1 (option)**

| Pin Name | I/O | Function |
|---|---|---|
| BCLK1 | I/O | Bit synchronization clock I/O for audio serial interface<br>This pin is used to input or output a bit synchronization clock for an audio serial interface.<br>Leave this pin open when not used. |
| LRCLK1 | I/O | Audio serial frame synchronization clock I/O<br>This pin is used to input or output a frame sync signal for serial transfers.<br>Leave this pin open when not used. |
| ASO1 | Output | Audio serial data output<br>Leave this pin open when not used. |
| ASI1 | Input | Audio serial data input<br>Connect this pin to GND when not used. |

**(5) Audio serial interface 2 (for DAC)**

| Pin Name | I/O | Function |
|---|---|---|
| BCLK2 | I/O | Bit synchronization clock I/O for audio serial interface<br>This pin is used to input or output a bit synchronization clock for an audio serial interface. |
| LRCLK2 | I/O | Audio serial frame synchronization clock I/O<br>This pin is used to input or output a frame sync signal for serial transfers. |
| ASO2 | Output | Audio serial data output |
| ASI2 | Input | Audio serial data input |

**(6) Internal power supply output pins**

| Pin Name | I/O | Function |
|---|---|---|
| TMPW2 | – | Internal DVDD2 output<br>Be sure to connect a 0.1 μF capacitor between this pin and DGND. |
| TMPW3 | – | Internal DVDD3 output<br>Be sure to connect a 0.1 μF capacitor between this pin and DGND. |

### (7) SD card interface pins

| Pin Name | I/O | Function |
|---|---|---|
| SD_RSTB | Input | Reset for SD card interface |
| SD_CLKI | Input | Clock input. Connect to SD_CLKO externally. |
| SD_CLKO | Output | Clock output |
| SD_DATA0 to 3 | I/O | Bi-directional SD data bus |
| SD_WP | Input | SD write protection |
| SD_CMD | I/O | SD command input |
| SD_CD | Input | SD card detection input |

### (8) General-purpose output pins

| Pin Name | I/O | Function |
|---|---|---|
| PO0 to PO7 | Output | General-purpose external output pins<br>These pins can be used to output control signals to peripheral devices. |

### (9) Test pins

| Pin Name | I/O | Function |
|---|---|---|
| TM0 | Input | Device test pin. Connect this pin to GND. |
| TM1 | Input | Device test pin. Connect this pin to GND. |
| TM2 | Input | Device test pin. Connect this pin to GND. |
| TM3 | Input | Device test pin. Connect this pin to GND. |
| TM4 | Input | Device test pin. Connect this pin to GND. |
| TM5 | Input | Device test pin. Connect this pin to GND. |
| TM6 | Input | Device test pin. Connect this pin to GND. |
| TM7 | Input | Device test pin. Connect this pin to GND. |
| TM8 | Output | Device test pin. Leave this pin open. |
| TM9 | Input | Device test pin. Connect this pin to GND. |
| TM10 | Input | Device test pin. Connect this pin to GND. |

### (10) Others

| Pin Name | I/O | Function |
|---|---|---|
| N.C. | – | Reserved pin for compatibility with future products.<br>Leave this pin open. |

### 1.4 Connection of Unused Pins

It is recommended to connect the unused pins as shown in the table below.

| Pin Name | I/O | Recommended Connection |
|---|---|---|
| A0 | Input | Connect to GND. |
| ASO1 | Output | Leave open. |
| ASI1 | Input | Connect to GND. |
| ASI2 | Input | Connect to GND. |
| BCLK1 | I/O | Leave open. |
| LRCLK1 | I/O | Leave open. |
| PO0 to PO7 | Output | Leave open. |
| SD_CLKI | Input | Connect to GND. |
| SD_CLKO | Output | Leave open. |
| SD_CD | Input | Connect to GND. |
| SD_CMD | I/O | Connect to GND. |
| SD_DATA0 to 3 | I/O | Connect to GND. |
| SD_WP | Input | Connect to GND. |
| TM0 to TM7 | Input | Connect to GND. |
| TM8 | Output | Leave open. |
| TM9, TM10 | Input | Connect to GND. |

**Caution: Leave the N.C. pins open.**

### 1.5 Initial State of Pins

| Pin Name | I/O | During Reset | After Reset |
|---|---|---|---|
| INT_B | Output | High-level output | High-level output |
| ASO1, ASO2 | Output | Hi-Z | Output |
| BCLK1 | I/O | Hi-Z | Output |
| BCLK2 | I/O | Hi-Z | Input |
| LRCLK1 | I/O | Hi-Z | Output |
| LRCLK2 | I/O | Hi-Z | Input |
| D0 to D15 | I/O | Hi-Z | Input |
| PO0 to PO7 | Output | Low-level output | Low-level output |
| SD_CLKO | Output | Low-level output | Low-level output |
| SD_CMD | I/O | Hi-Z | Input |
| SD_DATA0 to 3 | I/O | Hi-Z | Input |

**Notes 1.** This LSI enters the transparency mode after reset.

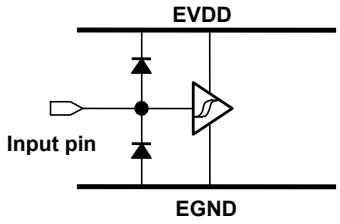
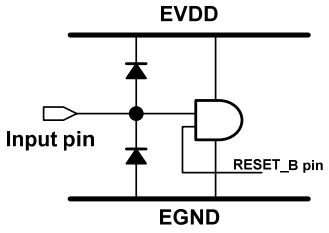
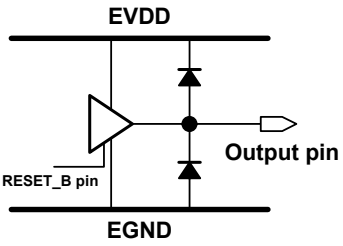
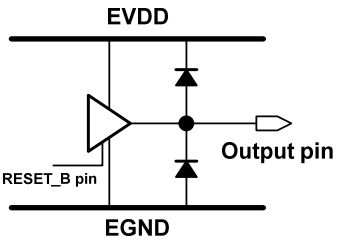
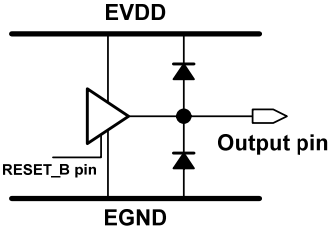
**2.** The pin status in the deep sleep mode is the same as that during reset.

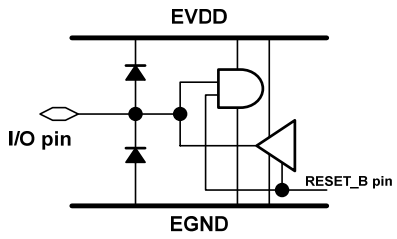
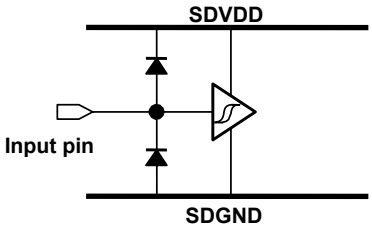
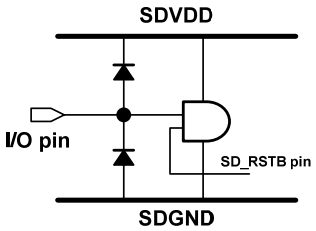
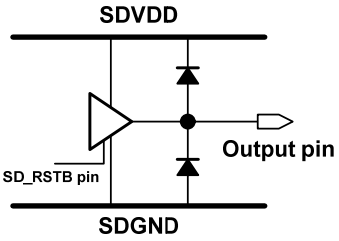
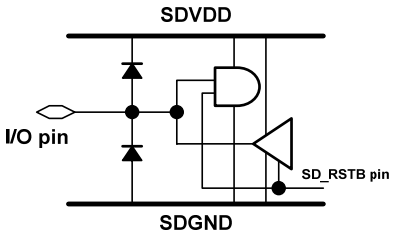
**3.** The statuses of the ASO1/2, BCLK1/2, and LRCLK1/2 pins can be controlled by the ASMODE register after reset.

### 1.6 Pin Protection

By setting the RESET_B pin to Low (during reset), pins are protected from the bus and no switching current flows into any of the functional pins even if the bus is activated.

### 1.7 Pin Outline Schematics

| Input Pin | Output Pin | I/O Pin | Pin Schematic Drawings |
|---|---|---|---|
| RESET_B | – | – |  |
| CLKIN<br>CS_B<br>WR_B<br>RD_B<br>A0 to A10<br>ASI1<br>ASI2 | – | – |  <br>The input buffer will be protected from the BUS and Clock during RESET_B=Low. |
| – | ASO1<br>ASO2 | – |  <br>The output will be Hi-Z during RESET_B = Low |
| – | PO0 to PO7 | – |  <br>The output will be Low state during RESET_B = Low |
| – | INT_B | – |  <br>The output will be High during RESET_B = Low |

| Input Pin | Output Pin | I/O Pin | Pin Schematic Drawings |
|---|---|---|---|
| – | – | D0 to D15<br>BCLK1<br>BCLK2<br>LRCLK1<br>LRCLK2 |  <br>The output will be Hi-Z and the input buffer will be protected from the BUS during RESET_B = Low. |
| SD_RSTB | – | – |  |
| SD_CLKI<br>SD_CD<br>SD_WP | – | – |  <br>The input buffer will be protected from the BUS and Clock during SD_RSTB = Low. |
| | SD_CLKO | – |  <br>The output will be Low during SD_RSTB = Low |
| – | – | SD_DATA0<br>SD_DATA1<br>SD_DATA2<br>SD_DATA3<br>SD_CMD |  <br>The output will be Hi-Z and the input buffer will be protected from the BUS during SD_RSTB = Low. |

## 2. INTERNAL POWER AND CLOCK DOMAINS

### 2.1 Power Domains

This LSI needs four power supplies (EVDD, DVDD, PLLVDD and SDVDD) and there are six power domains internally on this LSI. Internal DVDD1 is supplied while DVDD is supplied. Internal DVDD2 and DVDD3 are generated from DVDD by power switch, so it can cut off its domain internally.

**Table 2.1 Power Domains**

| Item | A/D | Voltage Range | Symbol | | Blocks |
|---|---|---|---|---|---|
| | | | Pin | Internal | |
| I/O | Digital | 1.7 to 2.0 V | EVDD<br>EGND | | Digital I/O buffer |
| Digital core | Digital | 1.16 to 1.24 V | DVDD<br>DGND | DVDD1<br>DGND | Host interface, pin control<br>Chip control register |
| | | | | DVDD2<br>DGND | CPU, audio processor, RAM |
| | | | | DVDD3<br>DGND | SD interface block |
| PLL | Analog | 1.16 to 1.24 V | PLLVDD<br>PLLGND | | PLL |
| SD I/O | Digital | 2.7 to 3.0 V | SDVDD | | SD I/O |

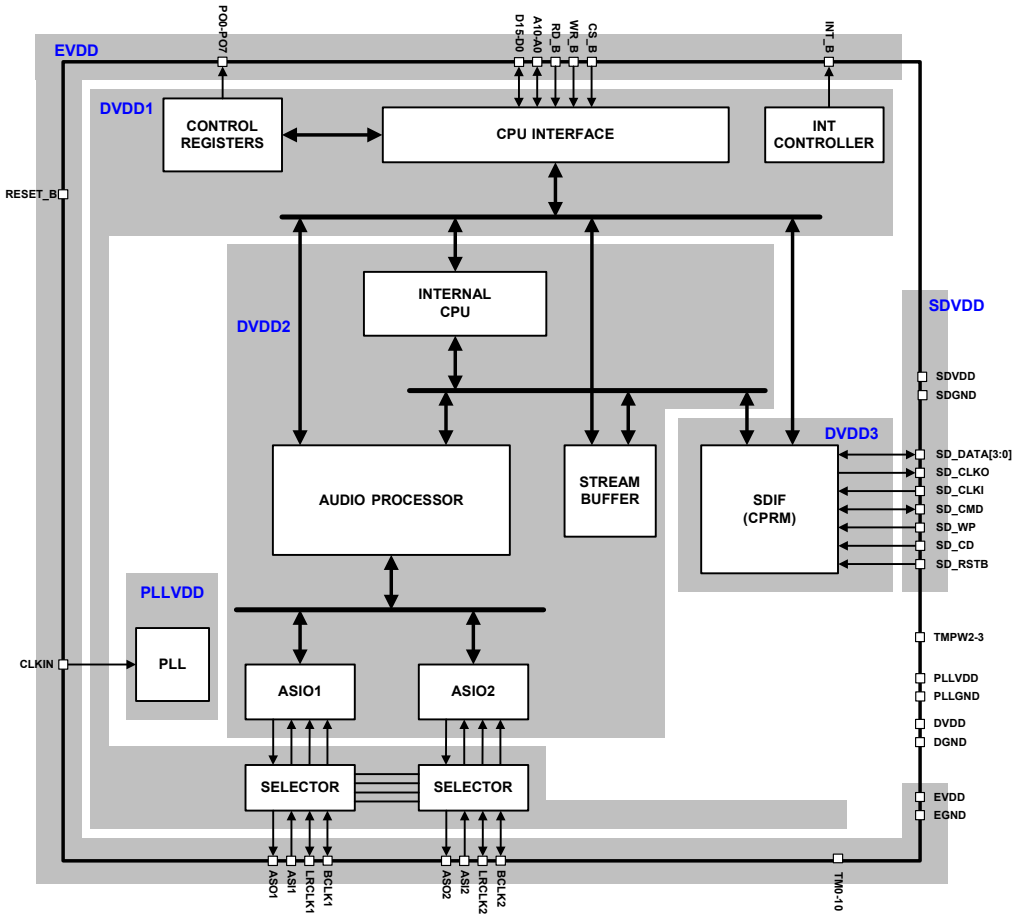



**Figure 2.1.1 Power Domains**

### 2.1.1 Hardware reset

There are two types of hardware reset on this LSI. One is controlled by a pin and the other is controlled by a command register.

**(1) RESET_B (pin)**

RESET_B is a hardware reset pin for all internal circuits of this LSI. The LSI enters the reset state when RESET_B set to Low (EGND level). The functions of these pins are as follows.

- Initialization of all registers
  All registers will be set to the default value immediately after RESET_B is set to Low.
  DVDD2 and DVDD3 domains are OFF after RESET_B is set to Low.
- Initialization of all circuits
- Initialization of I/O buffer functions (EVDD domain) for bus protection
- Protection of internal level shifter between internal EVDD and DVDD domains during power switching

**(2) RSTBFNC (command register)**

RSTBFNC is a hardware reset register for the DVDD2 domain. It can be controlled during RESET_B = High.

- Initialization of internal CPU registers and audio processor registers (DVDD2 domain)
- Initialization of all circuits of DVDD2 domain
- Protection of input between internal DVDD1 and DVDD2 domains during power switching

**(3) RSTBSD (command register)**

RSTBSD is a hardware reset register for the DVDD3 domain. It can be controlled during RESET_B = High. DVDD3 domain is initialized by RSTBSD after a clock is supplied for the DVDD3 domain.

- Initialization of SD interface registers (DVDD3 domain)
- Initialization of all circuits of DVDD3 domain
- Protection of input between internal DVDD1 and DVDD3 domains during power switching

**(4) SD_RSTB (pin)**

SD_RSTB is a hardware reset pin exclusively for SD interface I/O (SDIO). SDIO enters the reset state when SD_RSTB is set to Low (SDGND level). The circuits of the DVDD3 domain are not initialized by this pin.
The functions of these pins are as follows.

- Initialization of I/O buffer functions (SDVDD domain) for SD Card bus protection
- Protection of internal level shifter between SDVDD and DVDD domains during power switching

### 2.1.2 Power/reset control of DVDD2 and DVDD3 domains

It is possible to cut-off the internal DVDD2 and DVDD3 domains by command register control while DVDD is supplied, so it is also possible to reduce the standby current of each domain.

The PWFNC register is used for DVDD2 power control. PWFNC is OFF by default, which means the DVDD2 domain is OFF. Therefore, the DVDD2 domain circuits cannot be initialized by the RESET_B pin. The RSTBFNC register is also used to protect the input gates of the DVDD2 domain for security reasons. The DVDD2 domain must therefore be reset by the RSTBFNC register before DVDD2 will be ON.

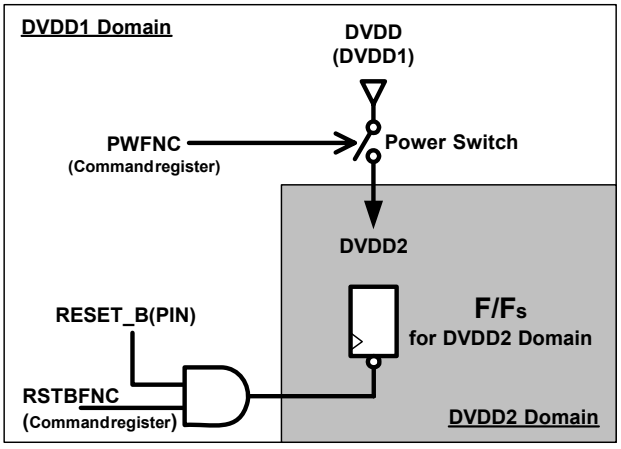



**Figure 2.1.2 Power/Reset Control of DVDD2 Domain**

The PWSD register is used for DVDD3 power control. PWSD is OFF by default, which means the DVDD3 domain is OFF. Therefore, the DVDD3 domain circuits cannot be initialized by the RESET_B pin. They are initialized by the RSTBSD register after the DVDD3 domain is turned on. RSTBSD is also used to protect input gates of DVDD3 domain for security reasons. The DVDD3 domain must therefore be reset by the RSTBSD register before DVDD3 will be ON.

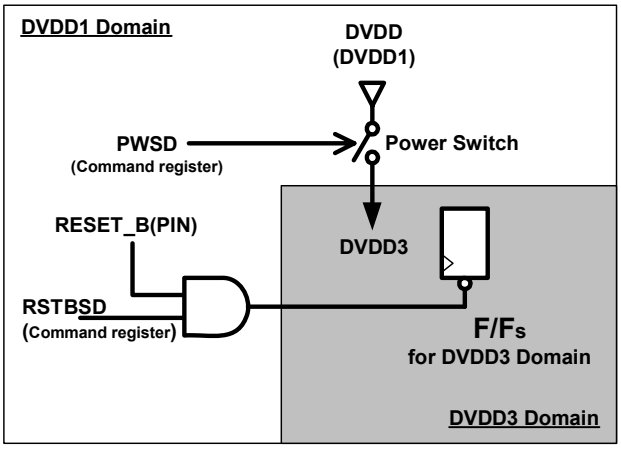



**Figure 2.1.3 Power and Reset Control of DVDD3 Domain**

The power control sequence is described in section 7.

## 2.2 Clock Domains

### 2.2.1 CLKIN

CLKIN is a system clock input pin. It is necessary to supply a 32.768 kHz clock from the RTC.

### 2.2.2 PLL

The PLL circuit generates an internal master clock from the CLKIN input (32.768 kHz).
It is controllable by a command register (PLLOSC).

### 2.2.3 Divider and domains

This LSI has three clock domains. Dividers make a clock of domain from the PLL output. They are controllable by command registers (DSPCKDIV, CPUCKDIV, and SDCKDIV).

- DSP domain
  Audio processor, ASIO1/2
- CPU domain
  Internal CPU for stream control, stream buffer
- SD domain
  SD interface core

### 2.2.4 Standby

Standby registers enable internal clocks to be supplied. The standby registers are also used for saving power.

- STPLL
  Enables PLL block operation.
- STDSP
  Enables clock supply to DSP domain.
- STCPU
  Enables clock supply to CPU domain.
- STSD
  Enables clock supply to SD domain.

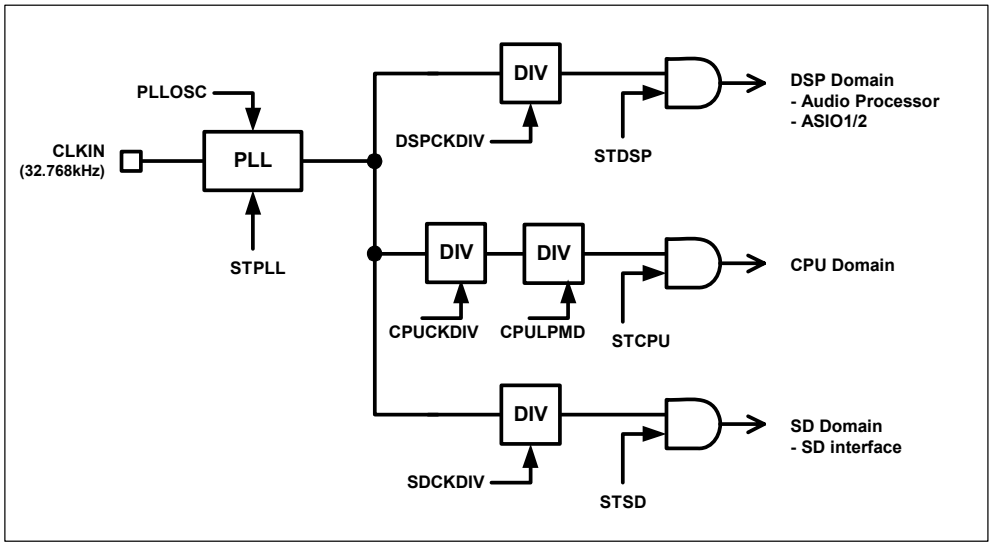



**Figure 2.2.1 Clock Domains**

## 3. HOST CPU INTERFACE

This LSI communicates as a slave device, with the host system by using a 16-bit parallel interface.
This LSI detects the address and data at a low level period of the CS_B pin and takes into the data at a low level width and a rising edge of the WR_B pin.

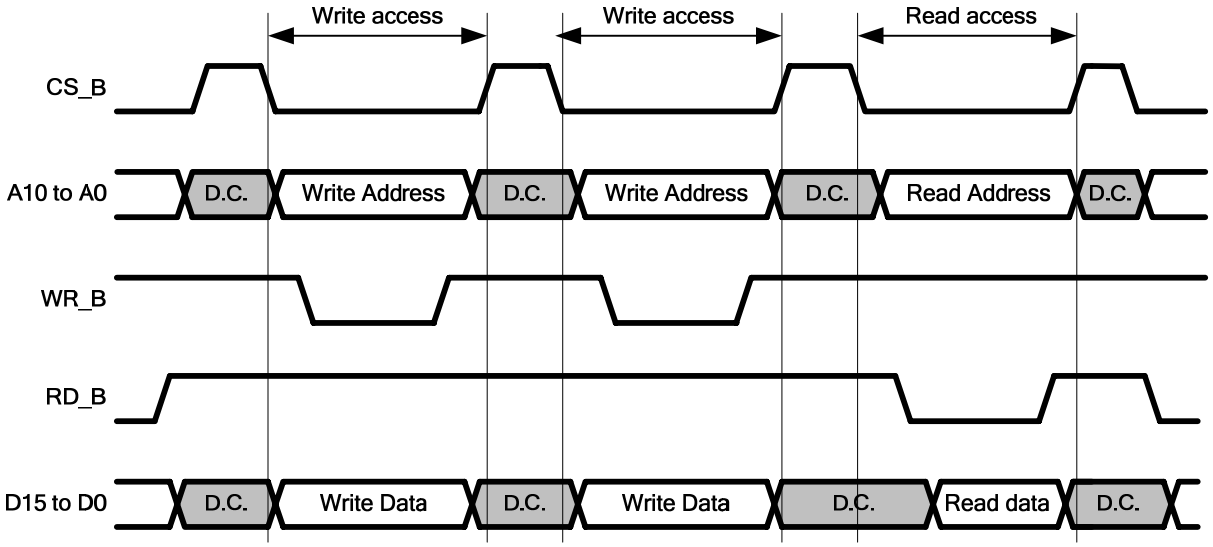



**Figure 3.1 Parallel Interface Format**

**Caution: 1. Be sure to observe the timing requirements of the parallel interface.**
**2. Be sure to fix the RD_B pin to high during the write cycle (WR_B = Low). Be sure also to fix the WR_B pin to high level during the read cycle (RD_B = Low).**

**Remark:** D.C.: Don't care.

## 4. AUDIO SERIAL INTERFACE

The audio serial interface (ASIO) is used for transmitting and receiving 16-bit PCM data serially. This LSI has two ASIOs, so it is easy to perform signal processing between the host and audio front-end device.
The available functions on each ASIO are as follows. These functions can be enabled by setting command registers.

- The $I^2S$ format is available.
- Master operation and slave operation are supported.
  Master operation: The signal received as a slave is used for the master.

| ASIO1 | ASIO2 | Comments |
|---|---|---|
| Slave | Slave | Prohibited |
| Slave | Master | Available. ASIO1 and ASIO2 must be used under the same conditions and operated synchronously.<br>ASIO2 can not be operated alone. |
| Master | Slave | Available. ASIO1 and ASIO2 must be used under the same conditions and operated synchronously.<br>ASIO1 cannot be operated alone. |
| Master | Master | Prohibited |

- Serial data clock (the number of data bits per sample) can be varied.
  32 to 128 fs, by 2 fs steps
- Transparency mode (direct connection between ASIO1 and ASIO2) is supported. (This mode is set by default.)

### 4.1 Format

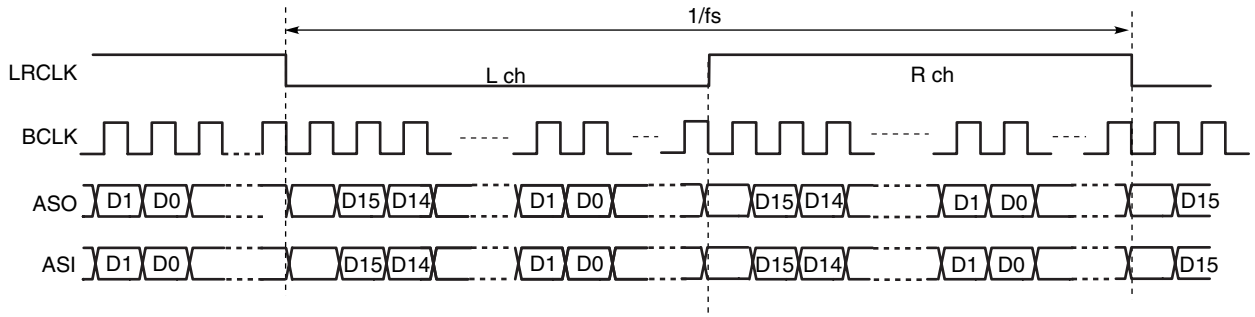



**Figure 4.1 $I^2S$ Format**

## 4.2 Synchronous Operation

Synchronous operation is available when placing this LSI between a master device and a slave device on a serial PCM bus. This LSI outputs a serial clock (BCLK) and a word sync signal (LRCLK) to a slave device, as a master operation. These clocks are the same as those received from a master device. ASIO1 and ASIO2 therefore operate with the same format and setting.

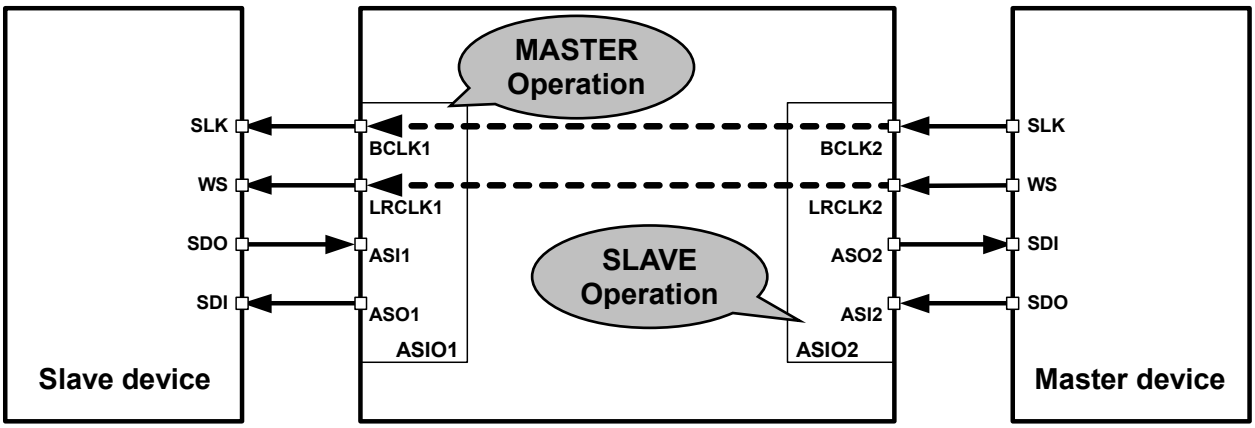



**Figure 4.2 Synchronous Operation**

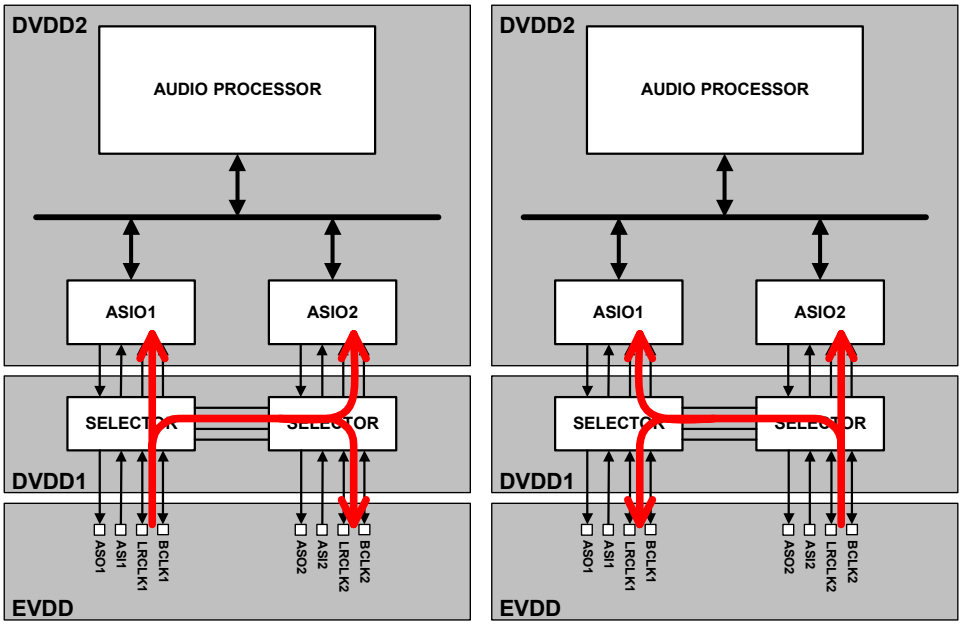



**Figure 4.3 Relation Between Master and Slave**

### 4.3 Transparency Mode

ASIO1 and ASIO2 can be directly connected internally (transparency mode).
There are two types of the transparency modes.

- Connection of ASIO1 and ASIO2
  ASI1 → ASO2, ASI2 → ASO1

- Connection inside ASIO1 or ASIO2)
  ASI1 → ASO1, ASI2 → ASO2

The connection type can be specified by using a control register. These pins are assigned in the DVDD1 domain. The other DVDD domains can be cut off during this mode, so the power consumption can be reduced.

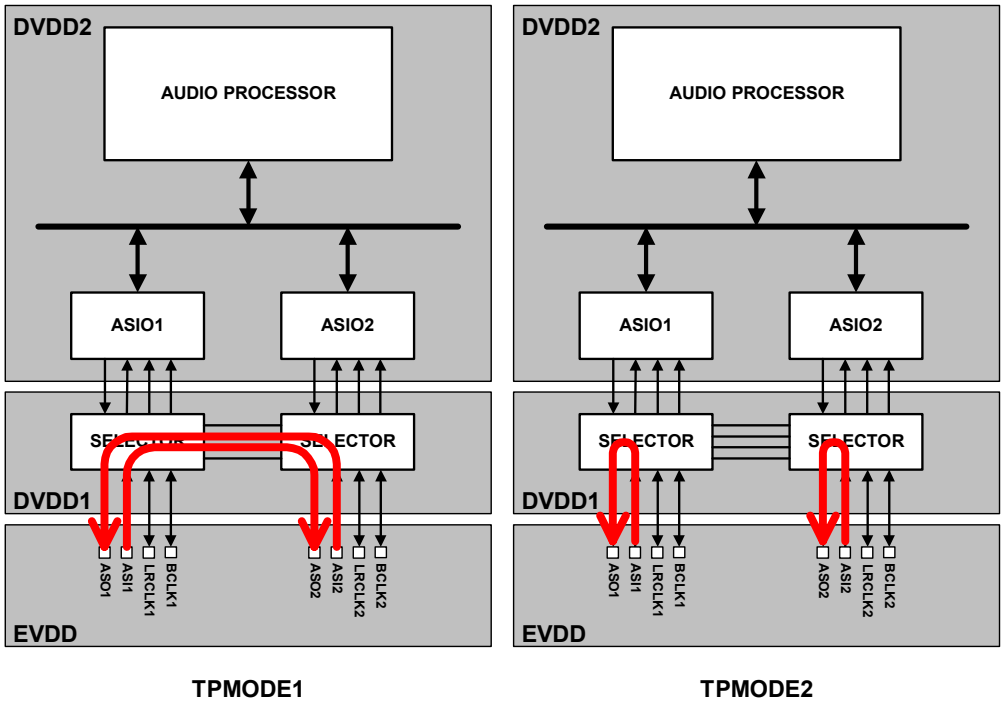



**Figure 4.4 Transparency Mode**

# 5. REGISTERS

## 5.1 Register Maps

| Address | | Sync/Async | Power domain |
|---|---|---|---|
| 000H | Chip control | S/A | DVDD1 |
| 100H | Reserved | A | DVDD1 |
| 200H | DSP control | S | DVDD2 |
| 300H | CPU control | S | DVDD2 |
| 400H | SD (1) | S | DVDD3 |
| 500H | SD (2) | S | DVDD3 |
| 600H | Reserved | S | DVDD2 |
| 700H | Reserved | S | DVDD2 |

### 5.1.1 Register map for chip control

**Table 5.1.1 Register Map for Chip Control**

| Address | W/R | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Contents | Register Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PWSD | 0 | 0 | 0 | PWFNC | 0000H | Power domains | PWSW |
| 002H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RSTBSD | 0 | 0 | 0 | RSTBFNC | 0000H | Async RESET for Power domains | RSTB |
| 004H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STSD | 0 | 0 | STCPU | STDSP | 0 | 0 | 0 | STPLL | 0000H | Standby setting | STNBYB |
| 006H | W/R | 0 | 0 | SDCKDIV[1:0] | | CPUCKDIV[1:0] | | DSPCKDIV[1:0] | | CPULPMD[1:0] | | PLLOSC[5:0] | | | | | | 0827H | Master clock setting | MCLK |
| 00AH | W | 0 | 0 | 0 | 0 | 0 | 0 | TPMODE[1:0] | | 0 | 0 | ASMODE[1:0] | | ASI1EN | ASO1EN | ASI2EN | ASO2EN | 012FH | ASIO control | ASIOCNT |
| 020H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 | 0000H | General purpose port output setting | POUT |
| 030H | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | INTSRC7 | INTSRC6 | INTSRC5 | INTSRC4 | INTSRC3 | INTSRC2 | INTSRC1 | INTSRC0 | 0000H | Interrupt source register | INTSRC |
| 032H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ITIM2 | ITIM1 | ITIM0 | 0000H | Interrupt clear for Timer | ITIM |
| 034H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | INTM7 | INTM6 | INTM5 | INTM4 | INTM3 | INTM2 | INTM1 | INTM0 | 0000H | Mask for INT controllor input | INTM |
| 040H | W/R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ENFLG | 0000H | Enable flag for device access | ENFLG |
| 042H | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CSTCPU | CSTDSP | 0000H | Status of continuous access | CSTA |
| 044H | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CCLRCPU | CCLRDSP | 0000H | Release of continuous access | CCLR |
| 070H | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PVER[3:0] | | | | MVER[3:0] | | | | 004*H | Product discernment and LSI Version | VER |

**Note:** Addresses 030H, 032H and 034H can be read or written after PLL is activated.

**Caution: Register accesses except for the above addresses are prohibited.**

### 5.1.2 Register map for DSP control

**Table 5.1.2 Register Map for DSP Control**

| Address | W/R | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Contents | Register Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 200H : 2FEH | W/R | Registers for the DSP block | | | | | | | | | | | | | | | | | | |

**Note:** This register area can be accessed after PLL is activated and STDSP is set to 1.

**Caution: Register accesses except for the above addresses are prohibited.**

### 5.1.3 Register map for CPU control

**Table 5.1.3 Register Map for CPU Control**

| Address | W/R | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Contents | Register Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 300H : 3FEH | W/R | Registers for the internal CPU block | | | | | | | | | | | | | | | | | | |

**Note:** This register area can be accessed after PLL is activated and STCPU is set to 1.

**Caution: Register accesses except for the above addresses are the prohibited.**

### 5.1.4 Register map for SD interface control

**Table 5.1.4 Register Map for SD Interface Control**

| Address | W/R | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | Contents | Register Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 400H : 5FEH | | Registers for SD intreface | | | | | | | | | | | | | | | | | | |

**Note:** This register area can be accessed after PLL is activated and STSD is set to 1.

**Caution: Register accesses except for the above addresses are the prohibited.**

## 5.2 Chip Control Registers

### 5.2.1 Power domain control register: PWSW (Address: 000H)

**(1) PWFNC**

This is a bit that controls inside the DVDD2 domain.
PWFNC = 1 enables power supply to the DVDD2 domain.
The values of DSP registers, RAM and DSP will not be kept during PWFNC = 0. After setting PWFNC to 1, a hardware reset must be applied (RSTBFNC register) to DVDD2 domain.

**PWFNC**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 0 | Internal power supply to DVDD2 domain is cut off. |
| 1 | ON | | Normal operation |

**(2) PWSD**

This is a bit that controls inside the DVDD3 domain.
PWSD = 1 enables power supply to the DVDD3 domain.
The values of SD registers and SD interface core will not be kept during PWSD = 0. After setting PWSD to 1, a hardware reset must be applied (RSTBSD register) to the DVDD3 domain.

**PWSD**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 0 | Internal power supply to DVDD3 domain is cut off. |
| 1 | ON | | Normal operation |

### 5.2.2 Async RESET for power domains register: RSTB (Address: 002H)

The RSTB register initializes the internal states of the DVDD2 and DVDD3 domains. This register must be asserted after power-on for each domain.

**(1) RSTBFNC**

This is a hardware reset bit for the DVDD2 domain. This bit must be set to 0, if PWFNC is changed.

**RSTBFNC**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Reset | 0 | Hardware async reset for DVDD2 domain |
| 1 | Active | | Normal operation |

**(2) RSTBSD**

This is a hardware reset bit for the DVDD3 domain. This bit must be set to 0, if PWSD is changed.

**RSTBSD**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Reset | 0 | Hardware async reset for DVDD3 domain |
| 1 | Active | | Normal operation |

### 5.2.3 Standby setting register: STNBY (Address: 004H)

This is a register that controls internal functional blocks and controls clock supply to the specific block.
The register does not initialize each block.

**(1) STPLL**

This is a bit that controls PLL standby. This controls PLL on/off.

**STPLL**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Standby | 0 | Sets PLL block to standby |
| 1 | ON | | Normal operation |

**Remark:** The PLL output clock is stopped during PLL standby mode (power down).

**Note:** Since the clock is not supplied to internal blocks during PLL standby, the block does not operate even if the STxx bit is set to 1.

**(2) STDSP**

This is a bit that controls an audio processor standby. The audio processor block enters the standby when this bit is set to 0. The DSP registers cannot be accessed because no clock is supplied. The DSP block is not initialized by setting this bit, but by hardware reset using RESET_B, RSTBFNC, or a DSP command.

**STDSP**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Standby | 0 | Sets DSP block to standby |
| 1 | ON | | Normal operation |

**(3) STCPU**

This is a bit that controls internal CPU standby. The internal CPU block enters the standby when this bit is set to 0. The CPU registers cannot be accessed because no clock is supplied. The CPU block is not initialized by setting this bit, but by hardware reset using RESET_B, RSTBFNC, or a CPU command.

**STCPU**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Standby | 0 | Sets CPU block to standby |
| 1 | ON | | Normal operation |

**(4) STSD**

This is a bit that controls the SD interface core standby. The SD interface core block enters the standby when this bit is set to 0. The SD register cannot be accessed because no clock is supplied. The SD interface core block. The block is not initialized by setting this bit, but by hardware reset using RESET_B or RSTBSD.

**STSD**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Standby | 0 | Sets SD block to standby |
| 1 | ON | | Normal operation |

### 5.2.4 Master clock setting register: MCLK (Address: 006H)

The MCLK register controls the master clock on the LSI side.

#### (1) PLLOSC

These are PLL output control register bits.

**PLLOSC[5:0]**

| PLLOSC[5:0] | Initial Value | Oscillation Frequency [MHz] |
|---|---|---|
| 1DH | 27H | 122.880 |
| 1EH | | 126.976 |
| 1FH | | 131.072 |
| 20H | | 135.168 |
| 21H | | 139.264 |
| 22H | | 143.360 |
| 23H | | 147.456 |
| 24H | | 151.552 |
| 25H | | 155.648 |
| 26H | | 159.744 |
| 27H | | 163.840 |

**Caution: 00 to 1C and 28H to 3F are invalid. These setting are prohibited.**

#### (2) DSPCKDIV

This is a register that sets the division ratio of the clock supplied to the DSP domain.

**DSPCKDIV[1:0]**

| DSPCKDIV[1:0] | Initial Value | Division Ratio |
|---|---|---|
| 0H | 0H | 1/2 |
| 1H | | 1/3 |
| 2H | | 1/4 |

**Caution: 3H is invalid and is prohibited.**

#### (3) CPUCKDIV

This is a register that sets the division ratio of the clock supplied to the CPU domain.

**CPUCKDIV[1:0]**

| CPUCKDIV[1:0] | Initial Value | Division Ratio |
|---|---|---|
| 0H | 2H | 1/2 |
| 1H | | 1/3 |
| 2H | | 1/4 |

**Caution: 3H is invalid and prohibited.**

**(4) SDCKDIV**

This is a register that sets the division ratio of the clock supplied to the SD domain.

**SDCKDIV[1:0]**

| SDCKDIV[1:0] | Initial Value | Division Ratio |
|---|---|---|
| 0H | 0H | 1/2 |
| 1H | | 1/3 |
| 2H | | 1/4 |

**Caution: 3H is invalid and prohibited.**

**(5) CPULPMD**

This is a register that sets the division ratio of the clock supplied to the CPU domain.

**CPULPMD[1:0]**

| CPULPMD[1:0] | Initial Value | Division Ratio |
|---|---|---|
| 0H | 0H | 1/1 |
| 1H | | 1/2 |
| 2H | | 1/4 |

**Caution: 3H is invalid and prohibited.**
**These registers must be changed when STCPU = 0 or STPLL = 0.**

### 5.2.5 ASIO control register: ASIOCNT (Address: 00AH)

**(1) ASI1EN, ASI2EN, ASO1EN, ASO2EN**

These bits control the ASI1, ASI2, ASO1 and ASO2 pin statuses.

**ASI1EN**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 1 | Disables ASI1 |
| 1 | ON | | Enables ASI1 |

**ASI2EN**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 1 | Disables ASI2 |
| 1 | ON | | Enables ASI2 |

**ASO1EN**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 1 | Disables ASO1 (ASO1 will be Hi-Z when ASO1EN = 0.) |
| 1 | ON | | Enables ASO1 |

**ASO2EN**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | OFF | 1 | Disables ASO2 (ASO2 will be Hi-Z when ASO2EN = 0.) |
| 1 | ON | | Enables ASO2 |

**Note: 1.** When ASI1EN = ASO1EN = 0, both LRCLK1 and BCLK1 pins become Hi-Z.
When ASI2EN = ASO2EN = 0, both LRCLK2 and BCLK2 pins become Hi-Z.

**2.** ASO1 will be Hi-Z when ASO1EN = 0.
ASO2 will be Hi-Z when ASO2EN = 0.

**3.** ASI1 and ASI2 must be low or high after reset regardless of ASI1EN/ASI2EN. Unexpected current may flow if ASI1 or ASI2 is in the Hi-Z state.

**(2) ASMODE**

These bits control synchronous operation. They control the master/slave operation for the ASIO1 and ASIO2 blocks. The LRCLK and BCLK inputs of the slave mode ASIO will be output to ones of the master mode ASIO, so the LSI cannot be the original master.

**ASMODE[1:0]**

| Data | Initial Value | ASIO1 | ASIO2 | Description |
|---|---|---|---|---|
| 0H | 2H | Slave | Slave | Setting prohibited |
| 1H | | Slave | Master | The LRCLK and BCLK of ASIO2 are the same as those of ASIO1. |
| 2H | | Master | Slave | The LRCLK and BCLK of ASIO1 are the same as those of ASIO2. |
| 3H | | Master | Master | Setting prohibited |

**Pin directions**

| Data | LRCLK1 | BCLK1 | LRCLK2 | BCLK2 |
|---|---|---|---|---|
| 1H | IN | IN | OUT | OUT |
| 2H | OUT | OUT | IN | IN |

**(3) TPMODE**

These are register bits that control the transparency mode. Other than TPMODE = 0H, ASI1/ASI2 and ASO1/ASO2 are disconnected from internal circuits, and connected directly to each other in the DVDD1 domain.

**TPMODE[1:0]**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0H | Normal | 1H | Connects ASI1/ASI2 and ASO1/ASO2 to internal circuits |
| 1H | TPMODE2 | | Connects ASO1 to ASI2 and ASO2 to ASI1. |
| 2H | TPMODE2 | | Connects ASO1to ASI1, and ASO2 to ASI2. |
| 3H | – | | Setting prohibited |

### 5.2.6 General-purpose output port setting register: POUT (Address: 020H)

The PO0 to PO7 pins output the POUT register value written from the host.

This register is placed into the DVDD1 domain. This is therefore not related to the ON/OFF state of the DVDD2 domain and can control the PO0 to PO7 pins while the DVDD2 domain is OFF.

**POUT[7:0]**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Low | 0 | Low-level output from corresponding pins to PO0 to PO7 |
| 1 | High | | High-level output from corresponding pins to PO0 to PO7 |

**Note:** The PO0 to 07 pins output 0 (low) during RESET_B = Low, and POUT values after reset.

### 5.2.7 Interrupt source register: INTSRC (Address: 030H)

This register is used to distinguish sources of interrupts generated by some function blocks. This register is set to 1 when an internal function block requests interruption.

**INTSRC[7:0]**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 15 to 8 | R | 0 | Reserved |
| 7 to 0 | R | | 0: No interrupt request<br>1: Interrupt request |

**Note:** This register is controlled by the API software on the host.

### 5.2.8 Timer interrupt clear register: ITIM (Address: 032H)

This register clears the timer interrupts. When this register is set to 1, the interrupt request is cleared. When this register is set to 0, the interrupt state is held.

**ITIM[2:0]**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Keep | 0 | Holds interrupt request state |
| 1 | Clear | | Clears interrupt requests |

**Note:** This register is controlled by the API software on the host..

### 5.2.9 Interrupt mask register: INTM (Address: 034H)

This register masks interrupt requests issued by function blocks.

**INTM[7:0]**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 15 to 8 | R | 0 | Reserved |
| 7 to 0 | R/W | | Mask of interrupt request input<br>0: Masks interrupt requests<br>1: Does not mask interrupt requests |

**Note:** This register is controlled by the API software on the host.

### 5.2.10 PLL activation enable flag register: ENFLG (Address: 040H)

This register indicates whether the PLL operation is active.

This register is set to 1 after PLL is stabilized.

**ENFLG**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Inactive | 0 | The PLL operation is active. |
| 1 | Active | | The PLL operation is inactive. |

### 5.2.11 Continuous data access control registers: CSTA (Address: 042H), CCLR (Address: 044H)

**(1) CSTDSP**

This register indicates that the host accesses data in the continuous mode for the DSP. This register holds 1 during the continuous data access mode.

This register is reset to 0 when the data access is complete correctly.

This register is reset to 0 when the CCLRDSP register is set to 1.

**CSTDSP**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Normal | 0 | Normal |
| 1 | Continuous | | Keeps continuous mode. |

**(2) CSTCPU**

This register indicates that the host accesses data in the continuous mode for the CPU. This register holds 1 during the continuous data access mode.

This register is reset to 0 when the data access is complete correctly.

This register is reset to 0 when the CCLRCPU register is set to 1.

**CSTCPU**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | Normal | 0 | Normal |
| 1 | Continuous | | Keeps continuous mode. |

**(3) CCLRDSP**

This register forcedly releases the DSP continuous access mode.

While the host accesses data in the continuous mode (CSTDSP indicates 1), the host can release the continuous access mode by writing 1 to CCLRDSP.

The host must write 0 to this register after writing 1. This register is write-only.

**CCLRDSP**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | – | 0 | – |
| 1 | Clear | | Clears continuous mode. |

**(4) CCLRCPU**

This register forcedly releases the CPU continuous access mode.

While the host accesses data in the continuous mode (CSTCUP indicates 1), the host can release the continuous access mode by writing 1 to CCLRCPU.

The host must write 0 to this register after writing 1. This register is write-only.

**CCLRCPU**

| Data | Mode | Initial Value | Description |
|---|---|---|---|
| 0 | – | 0 | – |
| 1 | Clear | | Clears continuous mode. |

## 5.3 DSP Registers

DSP registers are used to control the audio processor (DSP). These registers can be accessed after PLL is activated and the standby mode is released. Furthermore, these registers are initialized by the RESET_B pin or the RSTBFNC bit of the RSTB register.

The setting values of this area and related information are provided with the firmware.

## 5.4 CPU Registers

CPU registers are used to control the internal CPU (CPU). These registers can be accessed after PLL is activated and the standby mode is released. Furthermore, these registers are initialized by the RESET_B pin or the RSTBFNC bit of the RSTB register.

The setting values of this area and related information are provided with the firmware.

## 5.5 SD Registers

SD registers are used to control the SD interface (SD). These registers can be accessed after PLL is activated and standby mode is released. Furthermore, these registers are initialized by the RESET_B pin or the RSTBSD bit of the RSTB register.

## 6. POWER MANAGEMENT

### 6.1 Acceptable Power Supply Combinations

There are six power domains on this LSI. Acceptable combinations thereof are described below. (See Table 6.1).

**Table 6.1 Acceptable Power Supply Combinations**

| No. | Power Supply | | | | | | Function/Mode | | | | | Comment/Restriction |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | EVDD | DVDD | | | PLLVDD | SDVDD | Deep Sleep | Sleep | Transparency | Audio Decode | SD Access | |
| | | DVDD1 | DVDD2 | DVDD3 | | | | | | | | |
| 1 | – | – | – | – | – | – | – | – | – | – | – | Fully OFF |
| 2 | ON | – | – | – | – | – | Available | – | – | – | – | RESET_B = Low level |
| 3 | ON | ON | – | – | ON | – | – | Available | Available | – | – | RSTBFNC = RSTBSD = 0 |
| 4 | ON | ON | ON | – | ON | – | – | Available | Available | Available | – | RSTBSD = 0 |
| 5 | ON | ON | – | ON | ON | ON | – | Available | Available | – | Available | RSTBFNC = 0 |
| 6 | ON | ON | ON | ON | ON | ON | – | Available | Available | Available | Available | |
| 7 | ON | ON | – | – | ON | ON | – | Available | Available | – | – | SD_RSTB = Low level |
| 8 | ON | ON | ON | – | ON | ON | – | Available | Available | Available | – | SD_RSTB = Low level |
| 9 | ON | – | – | – | – | ON | Available | – | – | – | – | RESET_B = Low level, SD_RSTB = Low level |
| 10 | – | – | – | – | – | ON | Available | – | – | – | – | SD_RSTB = Low level |

**Note:** DVDD2 and DVDD3 are internal power domains. They are controllable by the command registers (PWFNC, PWSD).

**Caution: DVDD and PLLVDD must be supplied from the same source.**

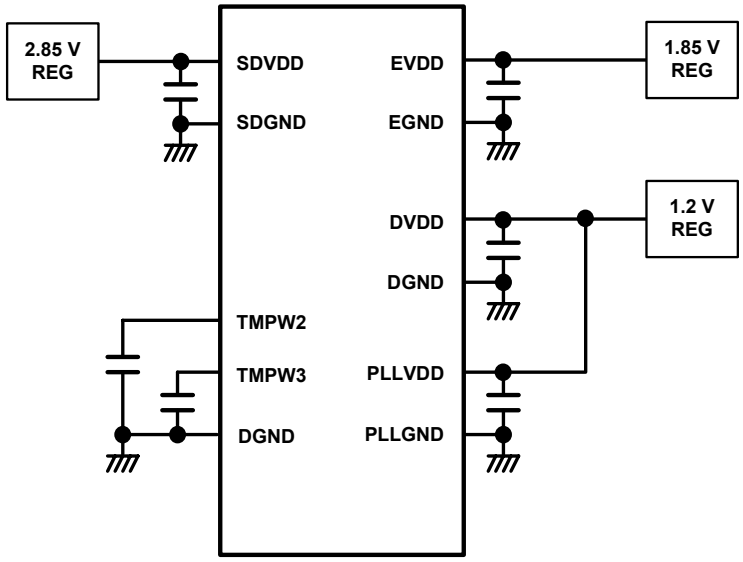



**Figure 6.1 Power Supply Connection**

**Note: 1.** It is recommended to minimize common impedance between pins DVDD and PLLVDD.

**2.** Connect capacitors as close as possible to the pins.

**3.** The capacitors of TMPW2 and TMPW3 are decoupling capacitors for pins DVDD2 and DVDD3.

## 6.2 Standby Modes

### 6.2.1 Sleep mode

This mode is used to reduce the time to return from the standby mode while power is being supplied. Data values of command registers and memory are kept during this mode, so it is not necessary to rewrite command registers or to re-download firmware.

The internal clock must be stopped by the command register during this mode, and power supply to the internal power domains must be kept on during this mode.

**Caution: Data will be lost if the power domain is turned off.**

### 6.2.2 Transparency mode

In this mode, ASIO1 and ASIO2 are connected directly each other.

This mode is controlled by the command register.

Since this mode does not require DVDD2 and DVDD3 activation, power consumption can be kept low.

Note that data in all registers will be lost, except for the DVDD1 domain data, when DVDD2 is turned off.

Be sure to rewrite data after turning on the DVDD2 domain. The same applies to DVDD3.

General-purpose output ports (PO0 to PO7) may be used during this mode.

### 6.2.3 Deep sleep mode

Power supplies (DVDD, PLLVDD and SDVDD) except EVDD can be cut off in this mode. This mode is used to provide the lowest power consumption. EVDD must be kept on for protecting CPU bus communication.

Note that all data written to registers and memory will be lost, so be sure to rewrite data after the operation returns to normal mode).

Follow the steps described below when setting hardware power saving.

<1> Turn off DVDD, PLLVDD and SDVDD with the RESET_B pin set to Low.

<2> Continue supplying EVDD since it is used to protect the CPU bus line.

<3> Be sure to fix the RESET_B and SD_RSTB pins to Low during a deep sleep mode operation.

Follow the steps described below to return to normal operation.

<1> Turn on DVDD and PLLVDD with the RESET_B and SD_RSTB pins set to Low.

<2> Set the RESET_B and SD_RSTB pins to High.

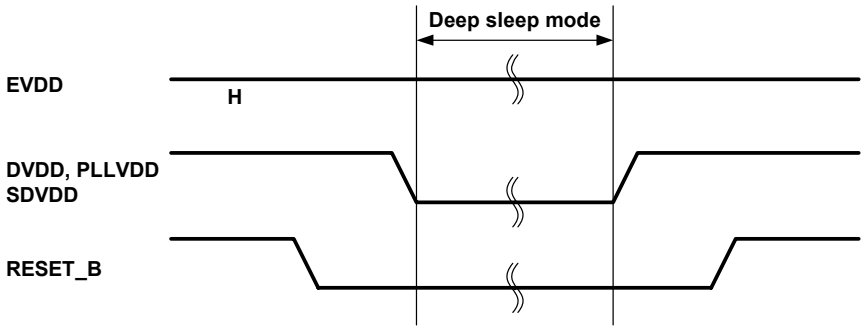



**Figure 6.2 Deep Sleep Mode**

**Caution: All pins, including the data bus pins, may output invalid data if the RESET_B pin level is High during the deep sleep mode, so a bus conflict may occur.**

**Unexpected sink current may flow to all pins including the data bus pins if the EVDD is turned off during the deep sleep mode. So a bus conflict may occur.**

## 7. POWER STARTUP PROCEDURE

From the power supply point of view, it is important to control the RESET_B pin, the SD_RSTB pin, and the hardware reset register for the DVDD2 domain (RSTBFNC) and the DVDD3 domain (RSTBSD). They are used to control different power domains. They must therefore be set to Low (0) whenever the power supply is switched.

### 7.1 Wakeup Sequence

#### 7.1.1 Basic sequence

The power-on control must be performed when the RESET_B pin is set to Low. After the power supply voltage has reached the recommended value, the internal DVDD1 domain can operate when the RESET_B pin is set to High. It is recommended to turn on EVDD first when the RESET_B pin is set to Low.

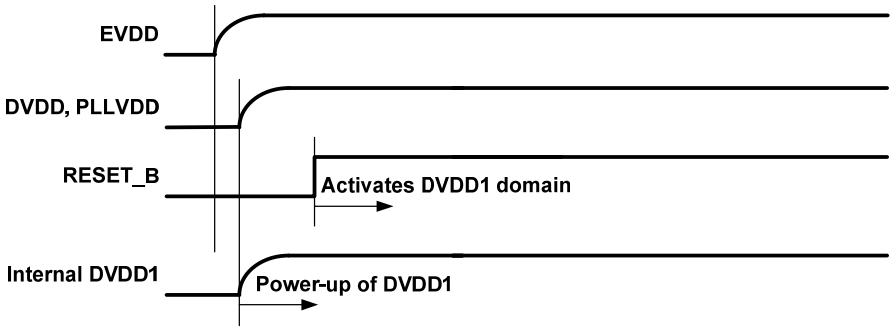



**Figure 7.1.1 Wakeup Sequence**

**Setting sequence**

(1) Set the RESET_B pin to Low (EGND).
(2) Supply EVDD.
(3) Supply DVDD and PLLVDD.
(4) After (3), internal DVDD1 is supplied automatically.
(5) Wait until all power supplies become stable.
(6) Set the RESET_B pin to High (EVDD level).
(7) Start operating the DVDD1 domain

**Note:** Supplying EVDD before DVDD is recommended.

**Caution: 1. Unexpected power supply current may flow if DVDD is supplied before EVDD.**
**2. Unexpected power supply current may flow during switching at all power supplies if the RESET_B pin is not set to Low.**
**3. All pins, including the host bus pins, become undefined if all the power supplies are turned on and the RESET_B pin level is High, so a bus conflict may occur.**

### 7.1.2 Wakeup sequence of DVDD2

The wakeup of DVDD2 is performed by command register PWFNC. The control sequence is as follows.

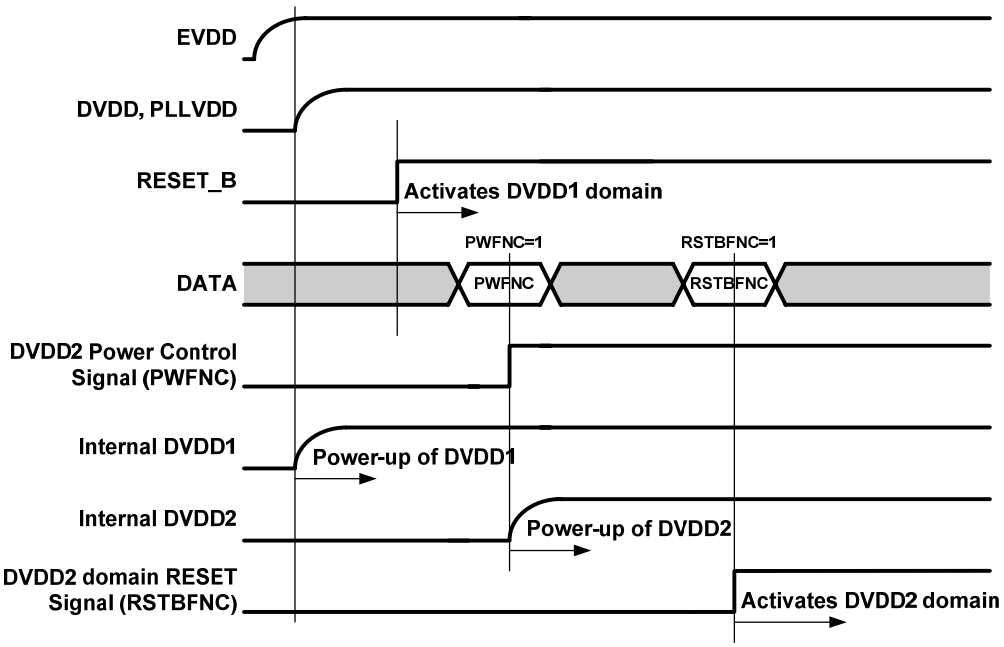



**Figure 7.1.2 Wakeup Sequence of DVDD2**

**Setting sequence**

(1) The DVDD1 domain operates after setting of the basic sequence.
(2) Set the PWFNC register to 1.
DVDD2 is turned on by writing 1 to the PWFNC register.
(3) Wait until DVDD2 becomes stable. (Wait 1 ms)
(4) Set the RSTBFNC register to 1.
Hardware reset for the DVDD2 domain is released by writing 1 to the RSTBFNC register.
(5) Start operating the DVDD2 domain.

**Caution: The DVDD2 domain cannot be initialized by RESET_B pin while DVDD2 is off. The domain must therefore be reset with hardware reset by the RSTBFNC register after DVDD2 has reached the recommended value.**

### 7.1.3 Wakeup sequence of DVDD3 and SDVDD

The wakeup of DVDD3 is performed by command register PWSD. The control sequence is as follows.

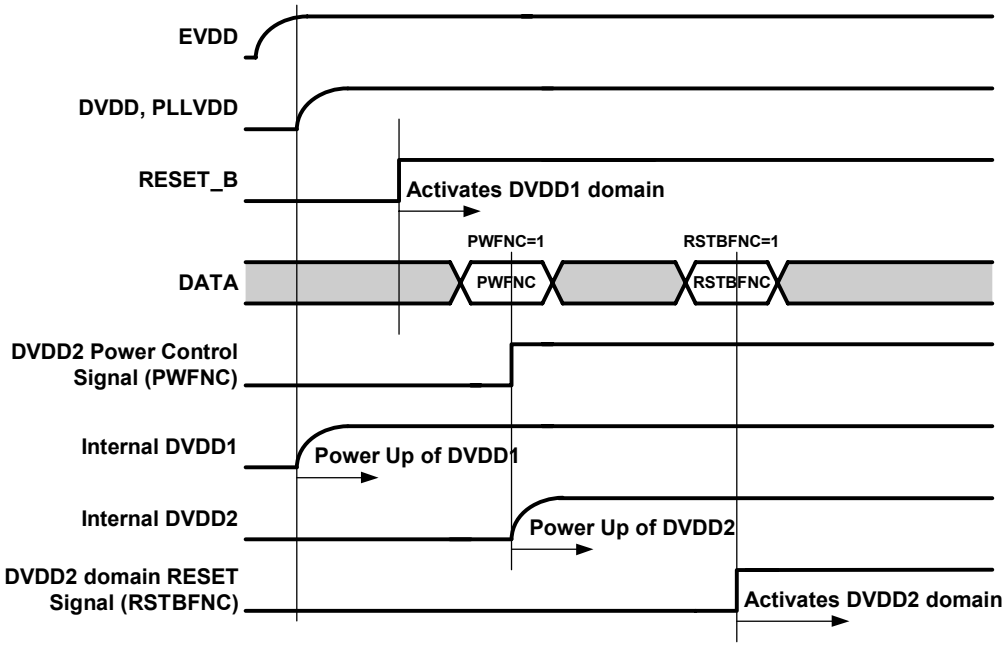



**Figure 7.1.3 Wakeup Sequence of DVDD3**

**Setting sequence**

(1) Set the RESET_B and SD_RSTB pins to Low.
(2) Supply EVDD.
(3) Supply DVDD and PLLVDD.
(4) After (3), internal DVDD1 is supplied automatically.
(5) Wait until all power supplies become stable.
(6) Set the RESET_B pin to High (EVDD level). Start operating the DVDD1 domain.
(7) Supply SDVDD.
(8) Set the PWSD register to 1. DVDD3 is turned to on by writing 1 to the PWSD register.
(9) Wait until DVDD3 becomes stable. (Wait 1ms)
(10) Set the RSTBSD register to 1. Hardware reset is released by writing 1 to the RSTBSD register.
(11) Set the SD_RSTB pin to High (SDVDD level).
(12) Start operating the DVDD3 domain.

**Caution: 1. DVDD3 domain cannot be initialized by the RESET_B pin when DVDD3 is off. The domain must therefore be reset with hardware reset by the RSTBSD register after DVDD3 has reached the recommended value.**

**2. SD_RSTB is used to protect pin conditions for the SD Card interface. It cannot be controlled when SDVDD is OFF. The SD_RSTB pin must therefore be set to Low before SDVDD becomes ON.**

**3. RSTBSD is also used to protect the input gates of the DVDD3 domain.**

### 7.2 Shut-down Sequence

Shut-down of this LSI is performed in the following sequence.

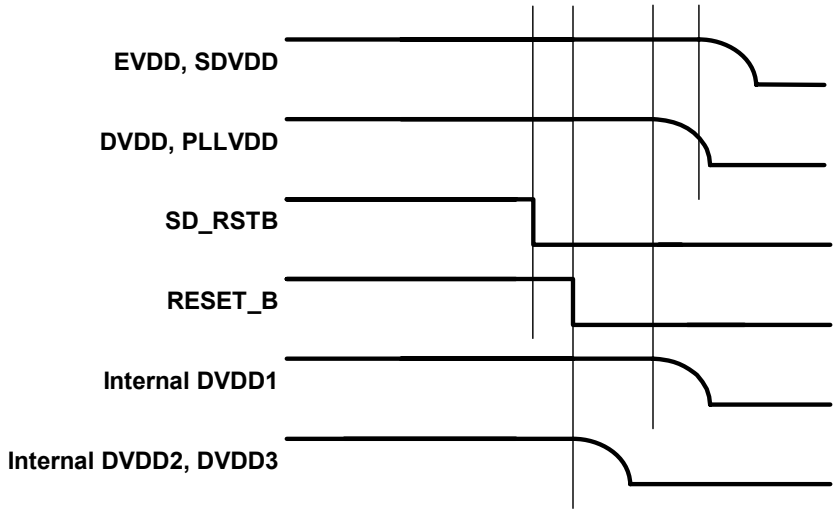



**Figure 7.2.1 Shut-down Sequence**

**Setting sequence**

(1) Set the SD_RSTB pin to Low (SDGND).
(2) Set the RESET_B pin to Low (EGND).
(3) Shut down DVDD and PLLVDD.
(4) Shut down EVDD and SDVDD.

**Caution: 1. EVDD and SDVDD must be shut down after DVDD shuts down.**
**2. The states of all pins become undefined after power shutdown, so a bus conflict may occur if the data bus is active during shutdown.**

## 7.3 Power Control During Operation

### 7.3.1 DVDD2 control

The internal DVDD2 domain may be turned ON/OFF by the PWFNC register while DVDD is supplied, to save power. The control sequence is as follows.

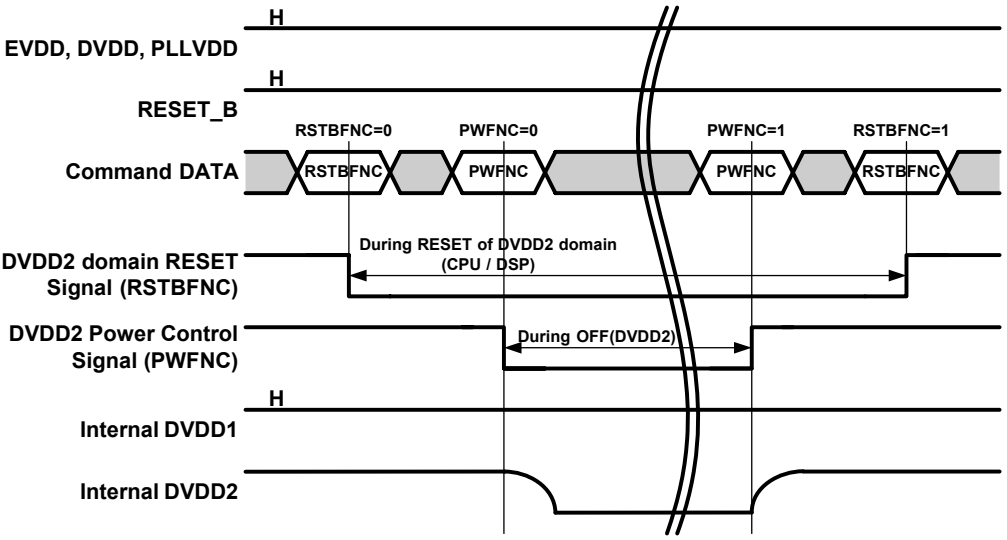



**Figure 7.3.1 DVDD2 Control**

**Setting sequence**

**Shutdown**

(1) Set the RSTBFNC register to 0.

(2) Set the PWFNC register to 0.
DVDD2 is turned off by writing 0 to the PWFNC register.

**Power up**

(1) Set the PWFNC register to 1.
DVDD2 is turned on by writing 1 to the PWFNC register.

(2) Wait until DVDD2 becomes stable.

(3) Set the RSTBFNC register to 1.
Hardware reset of the DVDD2 domain is released by writing 1 to RSTBFNC register.

(4) Start operating the DVDD2 domain

**Caution: Set the RSTBFNC register to 0 while DVDD2 is off. Otherwise, an unexpected current may flow through the DVDD1 domain.**

### 7.3.2 DVDD3 and SDVDD control

SDVDD and the internal DVDD3 domain may be turned ON/OFF by the PWSD register while DVDD is supplied, to save power. The control sequence is as follows.

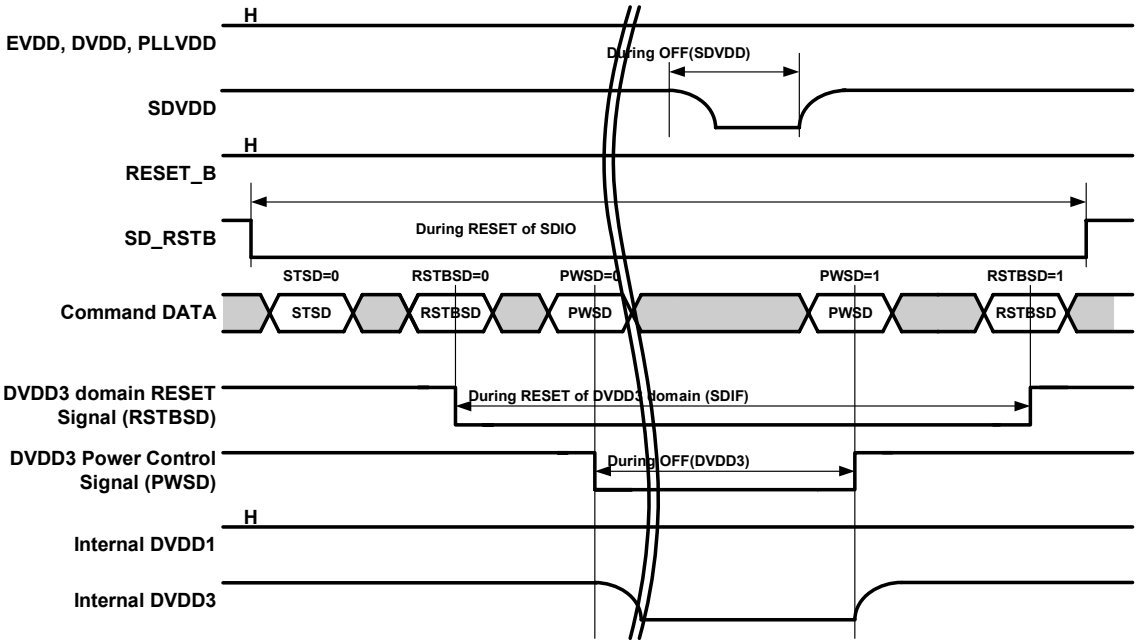



**Figure 7.3.2 Control of DVDD3 and SDVDD**

**Setting sequence**

**Shutdown**

(1) Set the SD_RSTB pin to Low. (SDGND)
(2) Set the STSD register to 0.
(3) Set the RSTBSD register to 0.
(4) Set the PWSD register to 0. DVDD3 is turned off by writing 0 to the PWSD register.
(5) Turn off SDVDD.

**Power up**

(1) Turn on SDVDD
(2) Set the PWSD register to 1. DVDD3 is turned on by writing 1 to the PWSD register.
(3) Wait until DVDD3 becomes stable.
(4) Set the RSTBSD register to 1.
Hardware reset of DVDD3 domain is released by writing 1 to the RSTBSD register.
(5) Set the SD_RSTB pin to High.
(6) Start operating DVDD3 domain

**Caution: 1. Set the RSTBSD register to 0 while DVDD3 is off. Otherwise, an unexpected current may flow through the DVDD1 domain.**

**2. For SD Card protection, SD_RSTB must be set to Low until DVDD3 reaches the recommended value. Internal DVDD3 must be turned off when SDVDD is off.**

## 8. ELECTRICAL SPECIFICATIONS

### 8.1 Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | DVDD | For digital blocks | –0.5 to +1.6 | V |
| | EVDD | For I/O blocks | –0.5 to +4.0 | V |
| | SDVDD | For SD blocks | –0.5 to +4.0 | V |
| | PLLVDD | For PLL blocks | –0.5 to +1.6 | V |
| Input voltage | $V_I$ | $V_I/V_O$ < EVDD + 0.5 V | –0.5 to +4.0 | V |
| Output voltage | $V_O$ | | –0.5 to +4.0 | V |
| Power dissipation | Pd | | 300 | mW |
| Storage temperature | $T_{stg}$ | | –50 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

### 8.2 Recommended Operating Conditions

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | DVDD | For digital blocks | 1.16 | 1.2 | 1.24 | V |
| | EVDD | For I/O blocks | 1.70 | 1.85 | 2.00 | V |
| | SDVDD | For SD I/O blocks | 1.70 | 1.85 | 3.00 | V |
| | PLLVDD | For PLL blocks | 1.16 | 1.2 | 1.24 | V |
| Input voltage | $V_I$ | | 0 | | EVDD | V |
| Operating ambient temperature | $T_A$ | | –20 | | +85 | °C |

### 8.3 Capacitance

($T_A$ = +25°C, DVDD = 0 V, EVDD = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | CI | f = 1 MHz, pins other than those tested: 0 V | | | 6 | pF |
| Output capacitance | CO | | | | 6 | pF |
| I/O capacitance | CIO | | | | 6 | pF |

**Note:** This condition applies to all pins.

### 8.4 DC Characteristics

($T_A$ = –20 to +85°C, with DVDD and EVDD within the recommended operating condition range)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IHN}$ | | 0.7EVDD | | EVDD | V |
| Input voltage, low | $V_{ILN}$ | | 0 | | 0.3EVDD | V |
| Input voltage, high (SDIO) | $V_{IHNSD}$ | For SD_RSTB, SD_CLKI, SD_CMD, SD_WP, SD_CD, SD_DATA0 to SD_DATA3 pins | 0.7SDVDD | | SDVDD | V |
| Input voltage, low (SDIO) | $V_{ILNSD}$ | For SD_RSTB, SD_CLKI, SD_CMD, SD_WP, SD_CD, SD_DATA0 to SD_DATA3 pins | 0 | | 0.3SDVDD | V |
| Output voltage, high | $V_{OH}$ | $I_{OH}$ = –3 mA | 0.7EVDD | | EVDD | V |
| Output voltage, low | $V_{OL3}$ | $I_{OL}$ = +3 mA | 0 | | 0.3EVDD | V |
| Output voltage, high (SDIO) | $V_{OHSD}$ | $I_{OH}$ = –3 mA for SD_CLKO, SD_CMD, SD_DATA0 to SD_DATA3 pins | 0.7SDVDD | | SDVDD | V |
| Output voltage, low (SDIO) | $V_{OL3SD}$ | $I_{OL}$ = +3 mA for SD_CLKO, SD_CMD, SD_DATA0 to SD_DATA3 pins | 0 | | 0.3SDVDD | V |
| Input leakage current, high | $I_{LHN}$ | $V_I$ = EVDD | 0 | | 20 | μA |
| Input leakage current, low | $I_{LLN}$ | $V_I$ = 0 V | –20 | | 0 | μA |
| High-impedance leakage current | $I_{ZI}$ | 0 V ≤ $V_I$ ≤ EVDD | –20 | | +20 | μA |
| Input leakage current, high (SDIO) | $I_{LHNSD}$ | VI = SDVDD<br>For SD_RSTB, SD_CLKI, SD_WP, SD_CD pins | 0 | | 20 | μA |
| Input leakage current, low (SDIO) | $I_{LLNSD}$ | VI = 0 V<br>For SD_RSTB, SD_CLKI, SD_WP, SD_CD pins | –20 | | 0 | μA |
| High-impedance leakage current (SDIO) | $I_{ZISD}$ | 0 V ≤ VI ≤ SDVDD<br>For SD_CMD, SD_DATA0 to SD_DATA3 pins | –20 | | +20 | μA |

## 8.5 AC Characteristics

(Unless otherwise specified, $T_A$ = –20 to +85°C, with DVDD and EVDD being within the recommended operating condition range)

### 8.5.1 Clock

**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CLKIN input frequency | $f_{CLKIN}$ | | | 32.768 | | kHz |
| Input rise and fall time | Trtf | 20 to 80% level | | | 30 | ns |
| Frequency tolerance | Ftol | | –1000 | | 1000 | ppm |
| Cycle-to-cycle jitter | Jctc | | –30 | | 30 | ns |
| Duty ratio | Dr | | 30 | | 70 | % |

**Notes 1.** The maximum input level for CLKIN should not exceed the power supply (EVDD) potential.

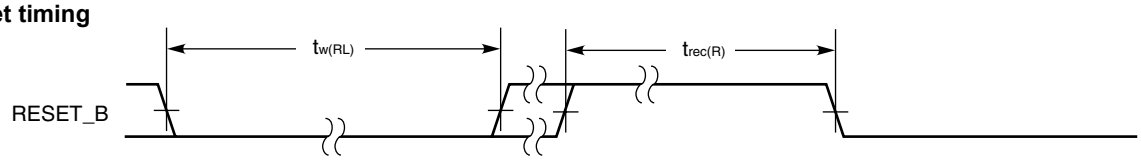
**2.** After PLL activation, normal operation begins after at least 2 ms have elapsed.

### 8.5.2 Reset (RESET_B and SD_RSTB)

**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low-level width | $t_{w(RL)}$ | | 150 | | | ns |
| Recovery time | $t_{rec(R)}$ | | 150 | | | ns |

**Reset timing**




### 8.5.3 Wakeup wait time of internal power supply

**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| DVDD2 wakeup wait time | $t_{upDVDD2}$ | From writing PWFNC register | 1 | | | ms |
| DVDD3 wakeup wait time | $t_{upDVDD3}$ | From writing PWSD register | 1 | | | ms |

### 8.5.4 Host interface

#### (1) Parallel I/F mode for internal CPU (Stand-alone playback mode)

**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| RD_B width | $t_{wRD}$ | | 5T + 30 | | | ns |
| WR_B width | $t_{wWR}$ | | 3T | | | ns |
| RD_B recovery time | $t_{rcRD}$ | | 2T | | | ns |
| WR_B recovery time | $t_{rcWR}$ | | 3T | | | ns |
| Data setup time | $t_{suDI}$ | WR_B↑ | 20 | | | ns |
| Data hold time | $t_{hDI}$ | WR_B↑ | 0 | | | ns |
| A, CS_B setup time | $t_{suAW}$ | WR_B↓ | 0 | | | ns |
| A, CS_B hold time | $t_{hAW}$ | WR_B↑ | 0 | | | ns |
| A, CS_B setup time | $t_{suAR}$ | RD_B↓ | 0 | | | ns |
| A, CS_B hold time | $t_{hAR}$ | RD_B↑ | 0 | | | ns |

**Switching characteristics**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data access time | $t_{accDO}$ | RD_B↓, $I_{sink}$ = 3 mA | | | 5T + 30 | ns |
| Data hold time | $t_{dDO}$ | RD_B↑, $I_{sink}$ = 3 mA | 0 | | 30 | ns |

**Remark** “T” is one period of the CPU block master clock.

#### (2) Parallel I/F mode for audio processor (DSP firmware download and settings)

**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| RD_B width | $t_{wRD}$ | | 5T + 30 | | | ns |
| WR_B width | $t_{wWR}$ | | 3T | | | ns |
| RD_B recovery time | $t_{rcRD}$ | | 2T | | | ns |
| WR_B recovery time | $t_{rcWR}$ | | 4T | | | ns |
| Data setup time | $t_{suDI}$ | WR_B↑ | 20 | | | ns |
| Data hold time | $t_{hDI}$ | WR_B↑ | 0 | | | ns |
| A, CS_B setup time | $t_{suAW}$ | WR_B↓ | 0 | | | ns |
| A, CS_B hold time | $t_{hAW}$ | WR_B↑ | 0 | | | ns |
| A, CS_B setup time | $t_{suAR}$ | RD_B↓ | 0 | | | ns |
| A, CS_B hold time | $t_{hAR}$ | RD_B↑ | 0 | | | ns |

**Switching characteristics**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data access time | $t_{accDO}$ | RD_B↓, $I_{sink}$ = 3 mA | | | 5T + 30 | ns |
| Data hold time | $t_{dDO}$ | RD_B↑, $I_{sink}$ = 3 mA | 0 | | 30 | ns |

**Remark** “T” is one period of the DSP block master clock.

### (3) Parallel I/F for SD Function mode (SD Direct mode)

**Timing requirements**

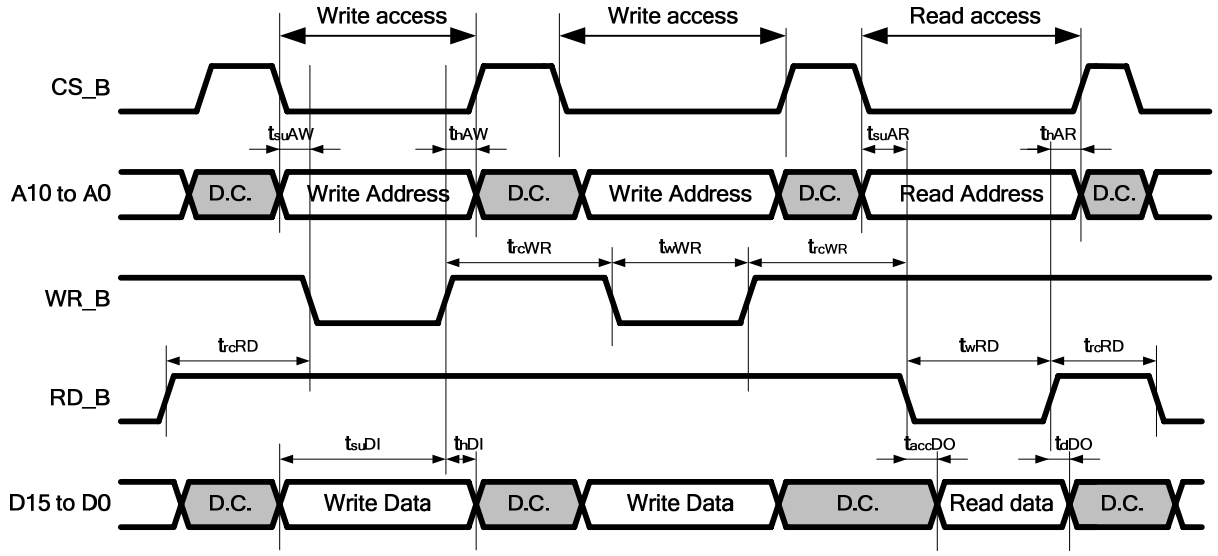
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| RD_B width | $t_{wRD}$ | | 8T + 30 | | | ns |
| WR_B width | $t_{wWR}$ | | 3T | | | ns |
| RD_B recovery time | $t_{rcRD}$ | | 2T | | | ns |
| WR_B recovery time | $t_{rcWR}$ | | 4T | | | ns |
| Data setup time | $t_{suDI}$ | WR_B↑ | 20 | | | ns |
| Data hold time | $t_{hDI}$ | WR_B↑ | 0 | | | ns |
| CS_B setup time | $t_{suAW}$ | WR_B↓ | 0 | | | ns |
| CS_B hold time | $t_{hAW}$ | WR_B↑ | 0 | | | ns |
| CS_B setup time | $t_{suAR}$ | RD_B↓ | 0 | | | ns |
| CS_B hold time | $t_{hAR}$ | RD_B↑ | 0 | | | ns |

**Switching characteristics**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data access time | $t_{accDO}$ | RD_B↓, $I_{sink}$ = 3mA | | | 8T + 30 | ns |
| Data hold time | $t_{dDO}$ | RD_B↑, $I_{sink}$ = 3mA | 0 | | 30 | ns |

**Remark** “T” is one period of the SD block master clock.

**Host interface timing**



### 8.5.5 Audio serial interface

## (1) Slave mode timing

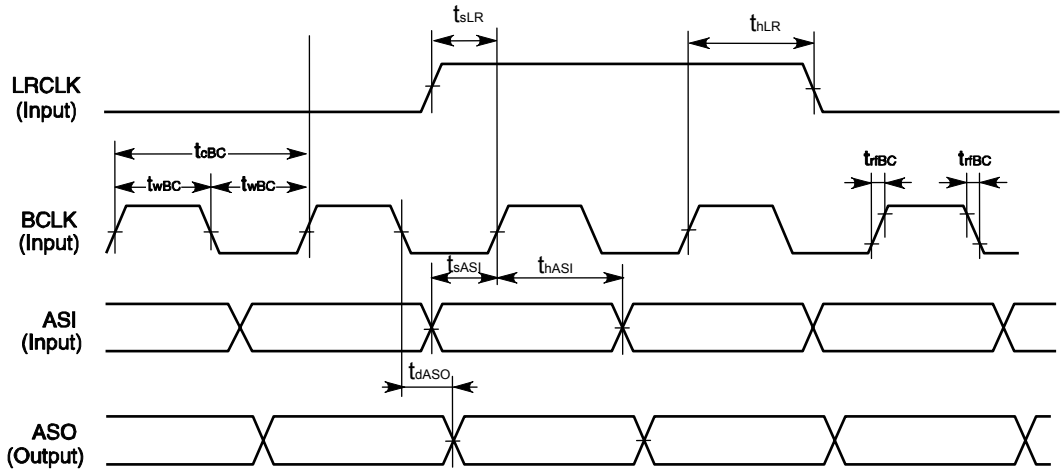
**Timing requirements**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LRCLK cycle time | tcLR | | | 1/fs | | ns |
| BCLK cycle time | tcBC | When set to 64 bits per fs | | 1/(fs × 64) | | ns |
| BCLK high-/low-level width | twBC | | | $t_{cBC}$/2 | | ns |
| BCLK rise/fall time | trfBC | | | | 20 | ns |
| LRCLK input setup time | tsLR | BCLK↑ | 50 | | | ns |
| LRCLK input hold time | thLR | BCLK↑ | 50 | | | ns |
| ASI input setup time | tsASI | BCLK↑ | 50 | | | ns |
| ASI input hold time | thASI | BCLK↑ | 50 | | | ns |

**Switching characteristics**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| ASO output delay time | tdASO | BCLK↓ | –50 | | +50 | ns |

**Audio serial I/O timing (slave mode)**

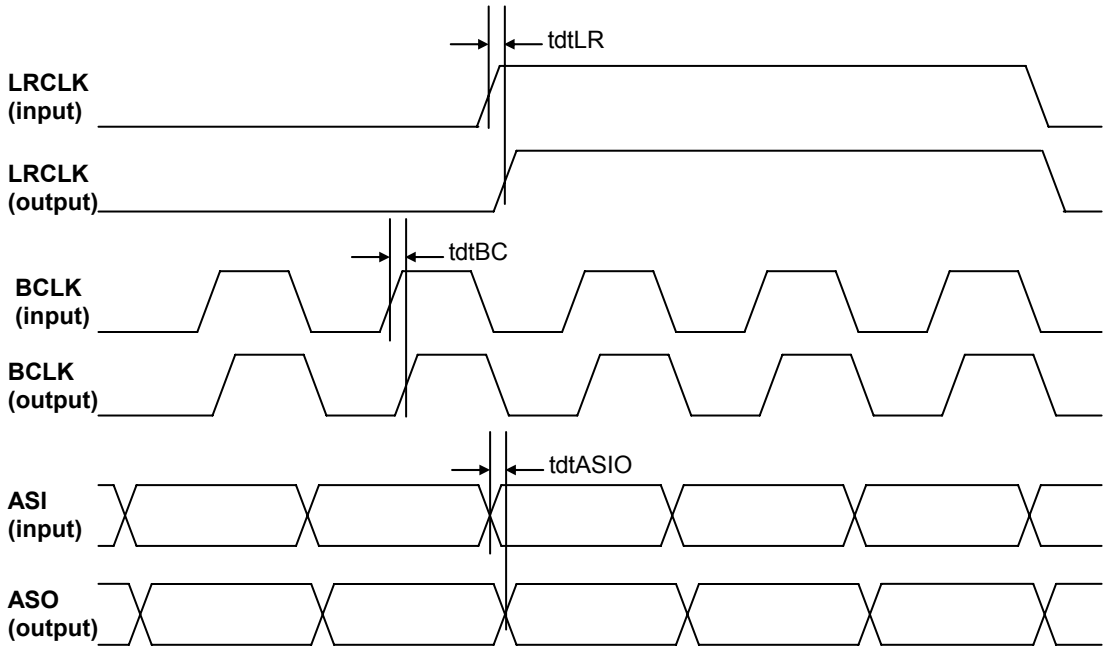


### (2) Synchronous and transparency mode timing

**Switching characteristics**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LRCLK through delay time | tdtLR | LRCLK (input) → LRCLK (output) | | | 20 | ns |
| BCLK through delay time | tdtBC | BCLK (input) → BCLK (output) | | | 20 | ns |
| ASIO through delay time | tdtASIO | ASI (input) → ASO (output) | | | 20 | ns |

**Audio serial I/O timing (synchronous and transparency modes)**



## 9. CURRENT CONSUMPTION

Unless otherwise specified, the following conditions must be met.

CLKIN = 32.768 kHz
Ambient temperature: $T_A$ = 25°C
Power supply voltage DVDD = PLLVDD = 1.2 V, EVDD = 1.85 V, SDVDD = 2.85 V

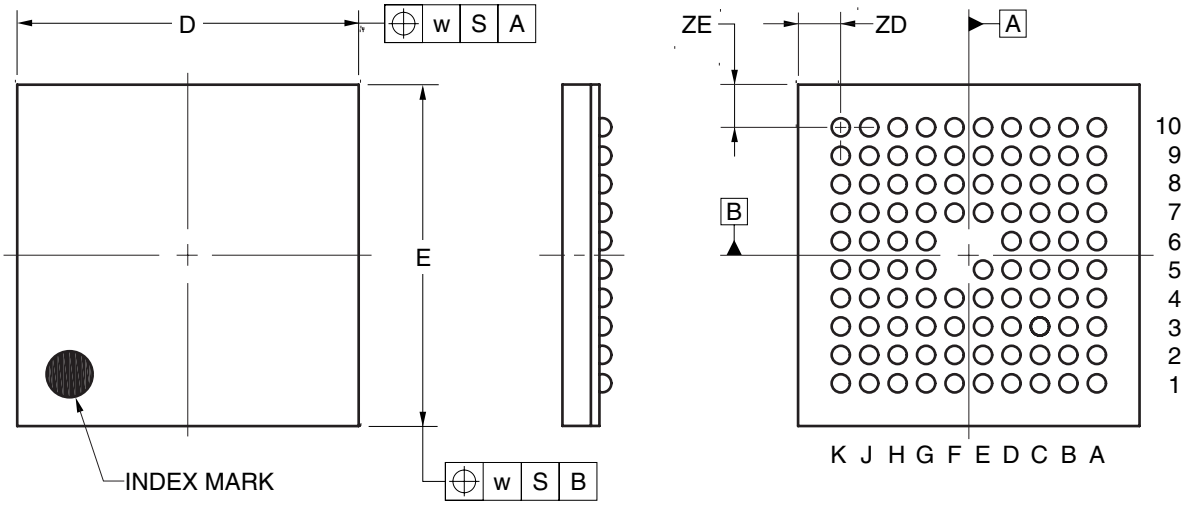
| Parameter | Symbol | Conditions | Power Supply Pin | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Operation mode | IDD1 | DSP test function<br>DSP 52.1 MHz | DVDD | | 16 | 20 | mA |
| | | | PLLVDD | | 0.3 | 0.5 | mA |
| | | | SDVDD[Note 1] | | – | 1 | mA |
| | | | EVDD[Note 1] | | – | 1 | mA |
| Command sleep mode | IDD2 | PWSW = 0011h, STNBY = 0000h,<br>RSTB = 0000h | DVDD | | 0.5 | 1 | mA |
| | | | PLLVDD | | 0.005 | 0.01 | mA |
| | | | SDVDD[Note 1] | | 0.005 | 0.01 | mA |
| | | | EVDD[Note 1] | | 0.005 | 0.01 | mA |
| Transparency mode | IDD3 | PWSW = 0000h, STNBY = 0000h,<br>RSTB = 0000h | DVDD | | 0.1 | 0.2 | mA |
| | | | PLLVDD | | 0.005 | 0.01 | mA |
| | | | SDVDD | | 0.005 | 0.01 | mA |
| | | | EVDD[Note 1] | | 0.005 | 0.01 | mA |
| Deep sleep mode | IDD4 | EVDD = ON; PLLVDD, DVDD,<br>SDVDD = OFF<br>RESET_B = SD_RSTB = Low | EVDD[Note 2] | | 0.005 | 0.01 | mA |

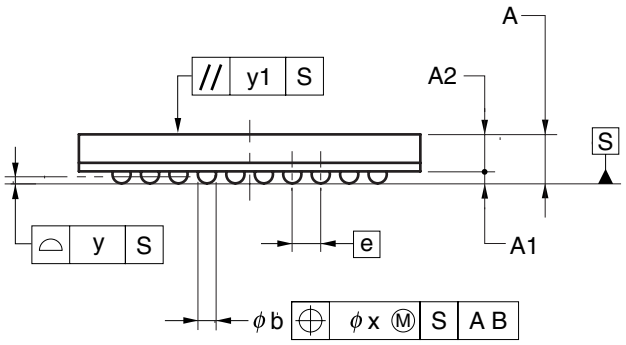
**Notes 1.** The SDVDD and EVDD pin currents are measured when there is no load. During actual operation, the SDVDD and EVDD pin currents differ depending on the external environment such as the clock rate, load capacitance, and load.

**2.** Input pins: Low or High, Output pins: No load.

<R> **10. PACKAGE DRAWING**

## 97-PIN PLASTIC FBGA (6x6)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 6.00±0.10 |
| E | 6.00±0.10 |
| w | 0.20 |
| A | 0.86±0.10 |
| A1 | 0.21±0.05 |
| A2 | 0.65 |
| e | 0.50 |
| b | 0.32±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

P97F1-50-BAC

<R> **11. RECOMMENDED SOLDERING CONDITIONS**

The μPD99911 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

- μPD99911F1-BAC-A: 97-pin plastic FBGA (6 × 6)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 260°C, Time: 60 sec. max. (at 220°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that prebaking is necessary at 125°C for 10 to 72 hours)<br>Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.<br>**<Caution>**<br>**Products packed in a medium other than a heat-resistance tray (such as a magazine, taping, and non-heat-resistance tray) cannot be baked.** | IR60-107-2 |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Remark** A lead-free product.

[MEMO]

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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