Dual, Low Power, Wideband, Low Noise, Rail-to-Rail Output, Operational Amplifiers

ADA4691-2/ADA4692-2

FEATURES

Low power: 200 µA typical, 250 µA maximum
Low distortion: 0.003% THD + N
Low noise: 16 nV/√Hz typical
3.9 MHz bandwidth
Slew rate: 1.4 V/µs typical
Offset voltage: 500 µV typical
Low offset voltage drift: 4 µV/°C maximum
Very low input bias currents: 0.5 pA typical
2.7 V to 5 V single supply or ±1.35 V to ±2.5 V dual supply

APPLICATIONS

Portable audio: MP3, PDA, smart phone, notebook
Portable instrumentation
Portable medical devices
Photodiode amplifiers
Sensor amplifiers
Low-side current sense
ADC drivers
Active filters
Sample-and-hold
Automotive sensors

PIN CONFIGURATIONS

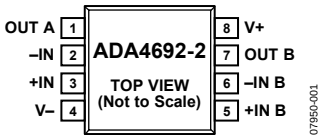

Figure 1. 8-Lead SOIC_N (R-8)

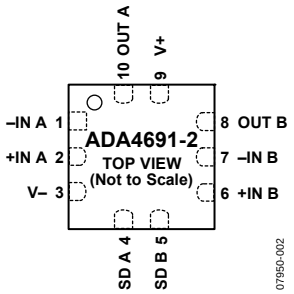

Figure 2. 10-Lead LFCSP (CP-10-11)

GENERAL DESCRIPTION

The ADA4691-2 and ADA4692-2 are dual, rail-to-rail output, single-supply amplifiers featuring low power, wide bandwidth, and low noise. The ADA4691-2 has two independent shutdown pins, allowing further reduction in supply current. These amplifiers are ideal for a wide variety of applications. Audio preamps, filters, IR/photodiode amplifiers, charge amps, and high impedance sensors all benefit from this combination of performance features.

Applications for these amplifiers include consumer audio personal players with low noise and low distortion that provide enough gain and slew rate response over the audio band at low power. Industrial applications with high impedance sensors, such as pyroelectric sensors and other IR sensors, benefit from the high impedance input, low offset drift, and enough bandwidth and response for low gain applications.

The ADA4691-2 and ADA4692-2 are specified over the extended industrial temperature range (−40°C to +125°C). The ADA4691-2 is available in a 10-lead LFCSP package, and the ADA4692-2 is available in an 8-lead SOIC package.

Rev. A

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REVISION HISTORY

ADA4691-2/ADA4692-2 Revision History

6/09—Rev. 0 to Rev. A

Added ADA4691-2 Information Throughout 1
Added Figure 2, Renumbered Subsequent Figures 1
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Added Shutdown Operations Section 15
Updated Outline Dimensions 16
Changes to Ordering Guide 16

ADA4692-2 Revision History

3/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

V_{SY} = 2.7 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = −0.3 V to +1.6 V		0.5	2.5	mV
		V_{CM} = −0.1 V to +1.6 V; −40°C < T_A < +125°C			3.5	mV
Input Bias Current	I_B			0.5	5	pA
ADA4691		−40°C < T_A < +125°C			350	pA
ADA4692		−40°C < T_A < +125°C			325	pA
Input Offset Current	I_{OS}			1	5	pA
		−40°C < T_A < +125°C			225	pA
Input Voltage Range		−40°C < T_A < +125°C	−0.3		+1.6	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.3 V to +1.6 V	70	90		dB
ADA4691		V_{CM} = −0.1 V to +1.6 V; −40°C < T_A < +125°C	62			dB
ADA4692		V_{CM} = −0.1 V to +1.6 V; −40°C < T_A < +125°C	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = 0.5 V to 2.2 V	90	100		dB
ADA4691		−40°C < T_A < +85°C	80			dB
ADA4692		−40°C < T_A < +85°C	85			
ADA4691		−40°C < T_A < +125°C	67			dB
ADA4692		−40°C < T_A < +125°C	73			
		R_L = 600 Ω, V_{OUT} = 0.5 V to 2.2 V	85	95		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.8	3	µV/°C
Input Capacitance	C_{IN}					
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
Logic High Voltage (Enabled)	V_{IH}	−40°C < TA < +125°C	+1.6			V
Logic Low Voltage (Power-Down)	V_{IL}	−40°C < TA < +125°C			0.5	V
Logic Input Current (Per Pin)	I_{IN}	−40°C < TA < +125°C, 0 V ≤ VSD ≤ 2.7 V			1	µA
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	2.65	2.67		V
		−40°C < T_A < +125°C	2.6			V
		R_L = 600 Ω to GND	2.55	2.59		V
		−40°C < T_A < +125°C	2.5			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to V_{SY}		24	30	mV
		−40°C < T_A < +125°C			40	mV
		R_L = 600 Ω to V_{SY}		78	95	mV
		−40°C < T_A < +125°C			125	mV
Short-Circuit Current	I_{SC}	V_{OUT} = V_{SY} or GND		±15		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = −100		372		Ω
Output Pin Leakage Current		−40°C < TA < +125°C, shutdown active, V_{SD} = V_{SS}		1		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	80	90		dB
		−40°C < T_A < +125°C	75			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = V_{SY}/2		165	200	µA
ADA4691-2		−40°C < T_A < +125°C			240	µA
ADA4692-2		−40°C < T_A < +125°C			225	µA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down, $V_{ShutDown}$ = V_{SS}		10		nA
		−40°C < TA < +125°C			2	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 600 Ω, C_L = 20 pF, A_V = +1		1.1		V/µs
Slew Rate	SR	R_L = 2 kΩ, C_L = 20 pF, A_V = +1		1.4		V/µs
Settling Time to 0.1%	t_S	Step = 0.5 V, R_L = 2 kΩ, 600 Ω		1		µs
Gain Bandwidth Product ADA4691	GBP	R_L = 1 MΩ, C_L = 35 pF, A_V = +1		3.6		MHz
Gain Bandwidth Product ADA4692	GBP	R_L = 1 MΩ, C_L = 35 pF, A_V = +1		3.9		MHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 35 pF, A_V = +1		49		Degrees
Turn-on, Turn-off time		R_L = 600 Ω		1		µs
NOISE PERFORMANCE						
Distortion	THD + N	A_V = −1, R_L = 2 kΩ, f = 1 kHz, V_{IN} rms = 0.15 V rms		0.009		%
		A_V = −1, R_L = 600 Ω, f = 1 kHz, V_{IN} rms = 0.15 V rms		0.01		%
		A_V = +1, R_L = 2 kΩ, f = 1 kHz, V_{IN} rms = 0.15 V rms		0.006		%
		A_V = +1, R_L = 600 Ω, f = 1 kHz, V_{IN} rms = 0.15 V rms		0.007		%
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
		f = 10 kHz		13		nV/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = −0.3 V to +3.9 V		0.5	2.5	mV
		V_{CM} = −0.1 V to +3.9 V; −40°C < T_A < +125°C			3.5	mV
Input Bias Current	I_B			0.5	5	pA
		−40°C < T_A < +125°C			360	pA
Input Offset Current	I_{OS}			1	5	pA
		−40°C < T_A < +125°C			260	pA
Input Voltage Range		−40°C < T_A < +125°C	−0.3		+3.9	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.3 V to +3.9 V	75	98		dB
ADA4691-2		V_{CM} = −0.1 V to +3.9 V; −40°C < T_A < +125°C	68			dB
ADA4629-2		V_{CM} = −0.1 V to +3.9 V; −40°C < T_A < +125°C	75			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V, V_{CM} = 0 V	95	110		dB
ADA4691-2		−40°C < T_A < +85°C	80			dB
ADA4692-2		−40°C < T_A < +85°C	90			dB
ADA4691-2		−40°C < T_A < +125°C	75			dB
ADA4692-2		−40°C < T_A < +125°C	80			dB
ADA4691-2 and ADA46920-2		R_L = 600 Ω, V_O = 0.5 V to 4.5 V, V_{CM} = 0 V	90	100		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		1	4	µV/°C
Input Capacitance						
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
Logic High Voltage (Enabled)	V_{IH}	−40°C < TA < +125°C	+2.0			V
Logic Low Voltage (Power-Down)	V_{IL}	−40°C < TA < +125°C			0.8	V
Logic Input Current (Per Pin)	I_{IN}	−40°C < TA < +125°C, 0 V ≤ VSD ≤ 2.7 V			1	µA
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.95	4.97		V
		−40°C ≤ T_A ≤ +125°C	4.90			V
		R_L = 600 Ω to GND	4.85	4.88		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		−40°C ≤ T_A ≤ +125°C	4.80			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		28	35	mV
		−40°C ≤ T_A ≤ +125°C			45	mV
		R_L = 600 Ω		90	110	mV
		−40°C ≤ T_A ≤ +125°C			140	mV
Short-Circuit Limit	I_{SC}	V_{OUT} = V_{SY} or GND		±55		mA
Closed-Loop Output Impedance	Z_{OUT}	ADA4691-2, f = 1 MHz, A_V = −100		364		Ω
Closed-Loop Output Impedance	Z_{OUT}	ADA4691-2, f = 1 MHz, A_V = −100		246		Ω
Output Pin Leakage Current		−40°C < TA < +125°C, shutdown active, V_{SD} = V_{SS}		1		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 5.5 V	80	90		dB
		−40°C ≤ T_A ≤ +125°C	75			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = V_{SY}/2		180	225	µA
ADA4691-2		−40°C ≤ T_A ≤ +125°C			275	µA
ADA4692-2		−40°C ≤ T_A ≤ +125°C			250	µA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shutdown, $V_{ShutDown}$ = V_{SS}		10		nA
		−40°C ≤ T_A ≤ +125°C			2	uA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, 600 Ω, C_L = 20 pF, A_V = +1		1.3		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 2 V step, R_L = 2 kΩ or 600 Ω		1.5		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 35 pF, A_V = +1		3.6		MHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 35 pF, A_V = +1		52		Degrees
Turn-on, Turn-off time		R_L = 600 Ω		1		µs
NOISE PERFORMANCE						
Distortion	THD + N	A_V = −1, R_L = 2 kΩ, f = 1 kHz, V_{IN} rms = 0.8 V rms		0.008		%
		A_V = −1, R_L = 600 Ω, f = 1 kHz, V_{IN} rms = 0.8 V rms		0.006		%
		A_V = +1, R_L = 2 kΩ, f = 1 kHz, V_{IN} rms = 0.8 V rms		0.003		%
		A_V = +1, R_L = 600 Ω, f = 1 kHz, V_{IN} rms = 0.8 V rms		0.001		%
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3.2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
	e_n	f = 10 kHz		13		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{SS} – 0.3 V to V_{DD} +0.3 V
Input Current[1]	±10 mA
Shutdown Pin Rise/Fall times	50 μs maximum
Differential Input Voltage[2]	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Input pins have clamp diodes to the supply pins. Limit the input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.3 V.

[2] Differential input voltage is limited to 5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages and measured using a standard 4-layer board, unless otherwise specified.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	155	45	°C/W
10-Lead LFCSP (CP-10-11)	88	32	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

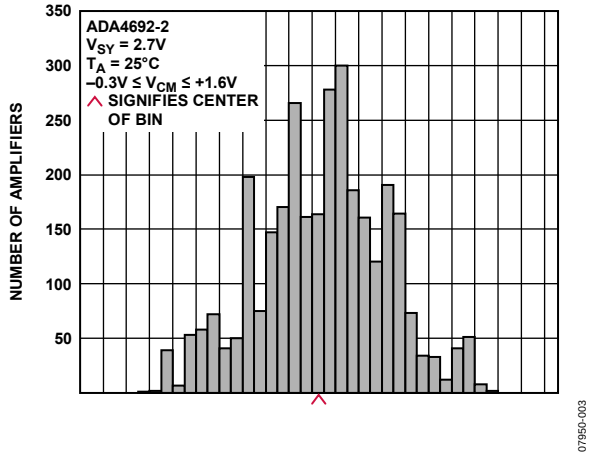

Figure 3. Input Offset Voltage Distribution

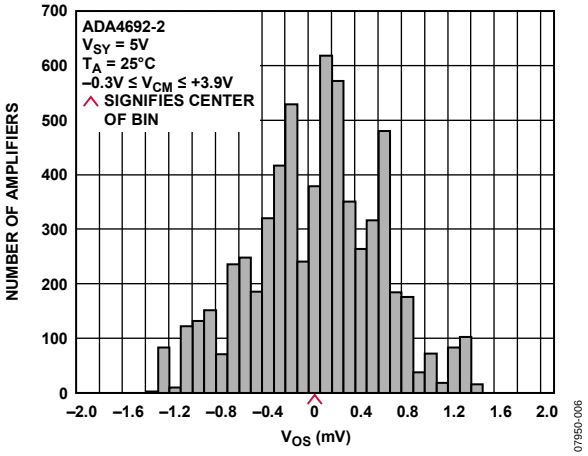

Figure 6. Input Offset Voltage Distribution

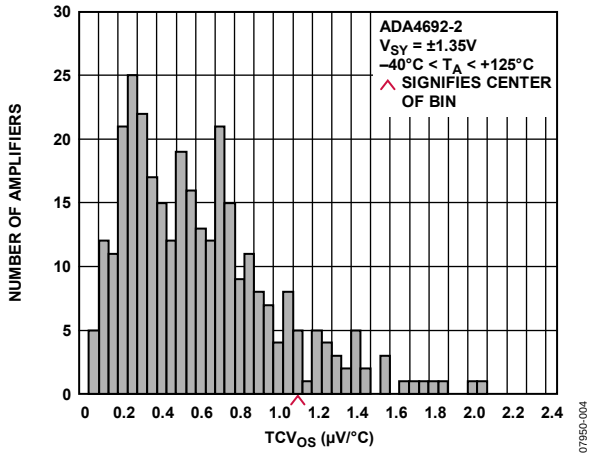

Figure 4. Input Offset Voltage Drift Distribution

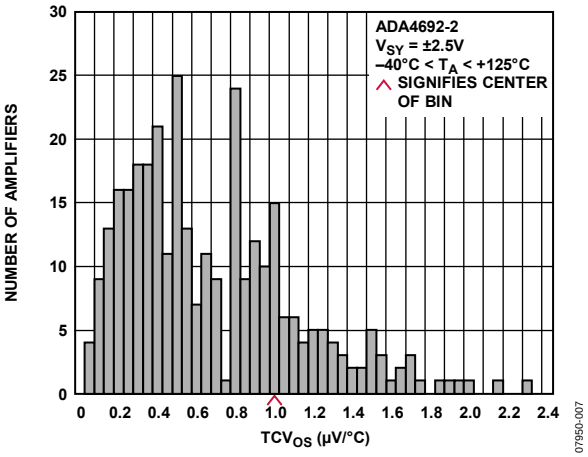

Figure 7. Input Offset Voltage Drift Distribution

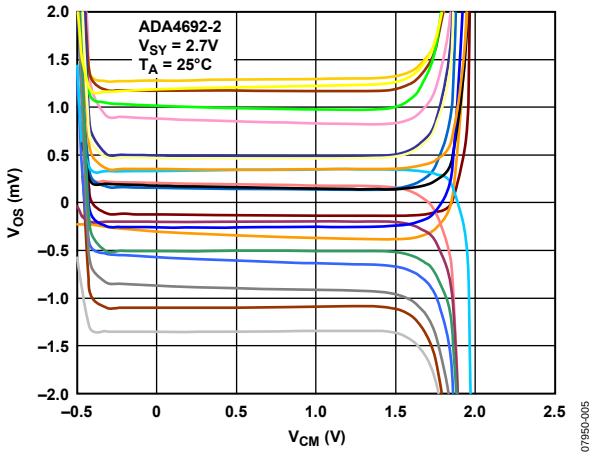

Figure 5. Input Offset Voltage vs. Common-Mode Voltage

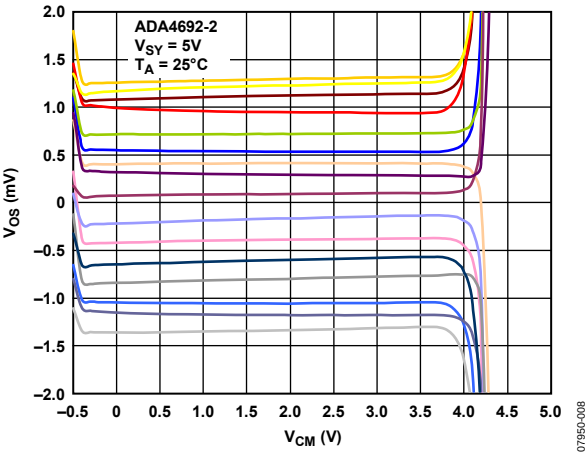

Figure 8. Input Offset Voltage vs. Common-Mode Voltage

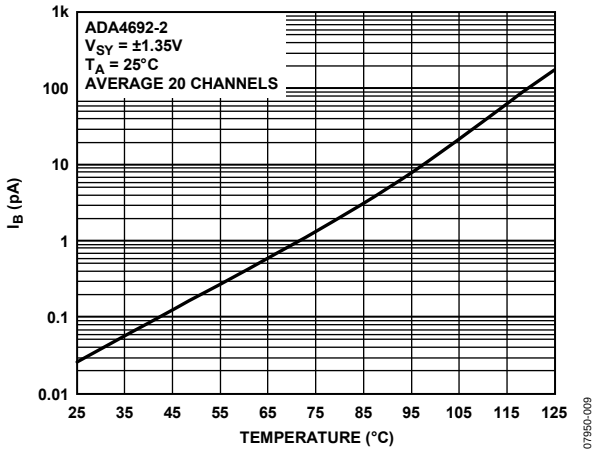

Figure 9. Input Bias Current vs. Temperature

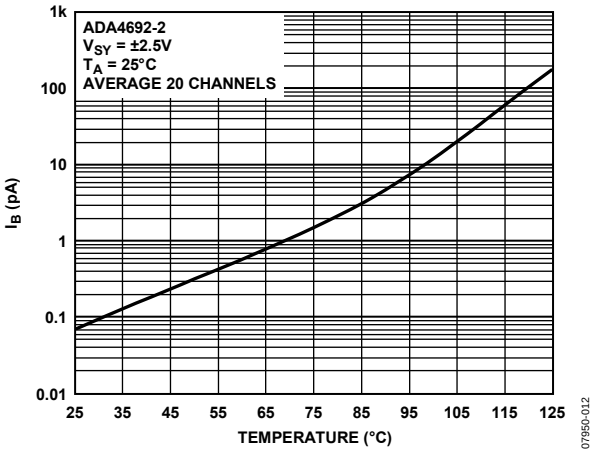

Figure 12. Input Bias Current vs. Temperature

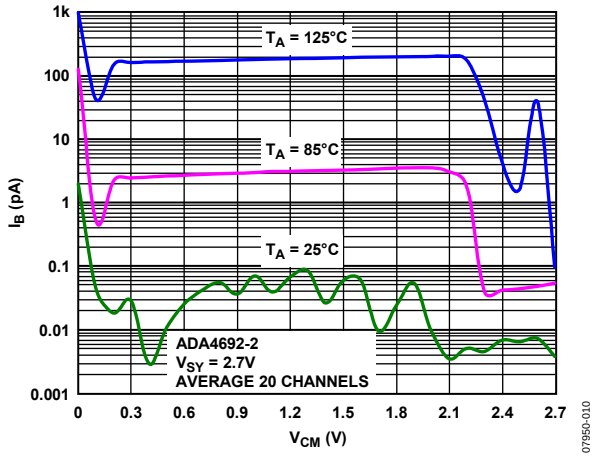

Figure 10. Input Bias Current vs. Common-Mode Voltage

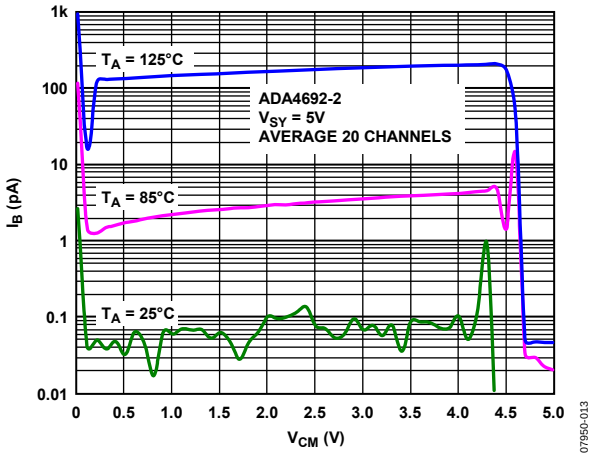

Figure 13. Input Bias Current vs. Common-Mode Voltage

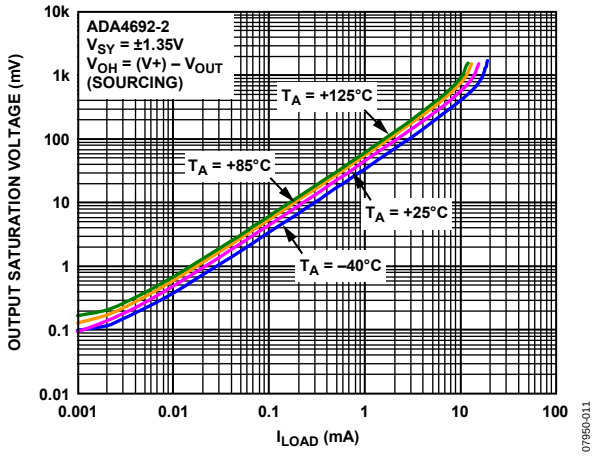

Figure 11. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

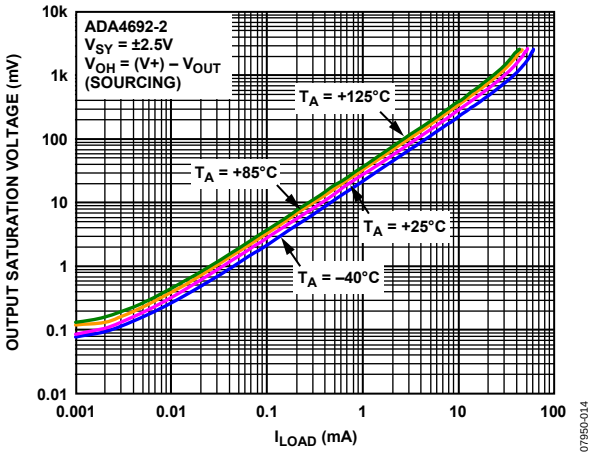

Figure 14. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

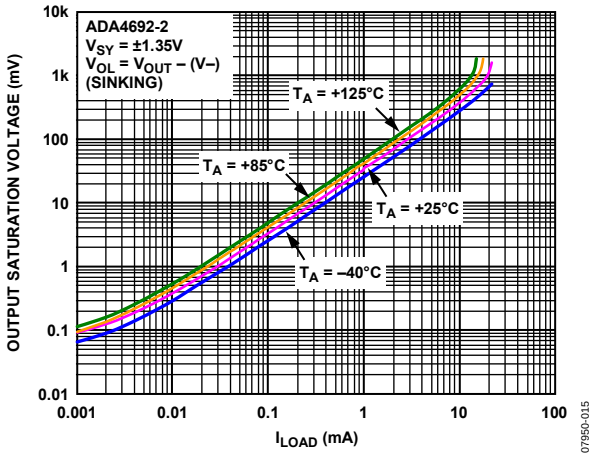

Figure 15. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

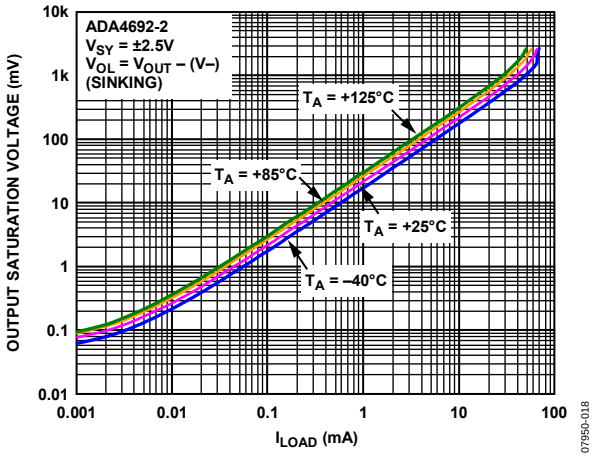

Figure 18. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

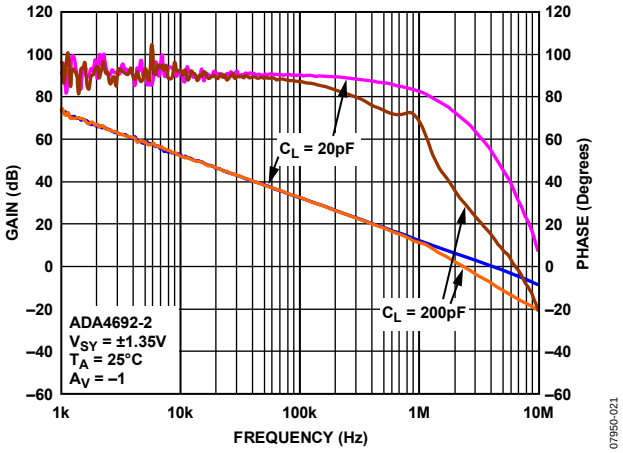

Figure 16. Open-Loop Gain and Phase vs. Frequency

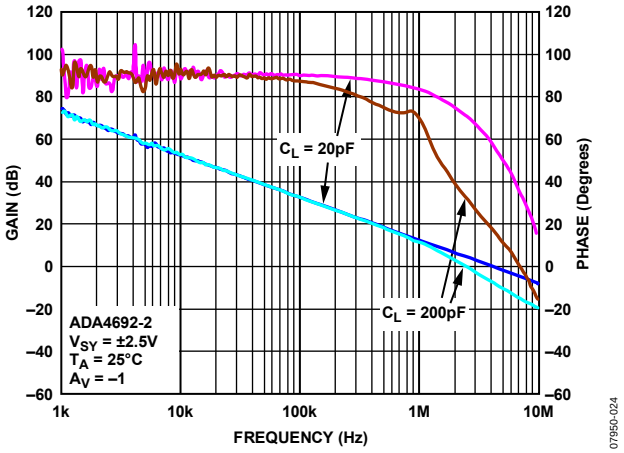

Figure 19. Open-Loop Gain and Phase vs. Frequency

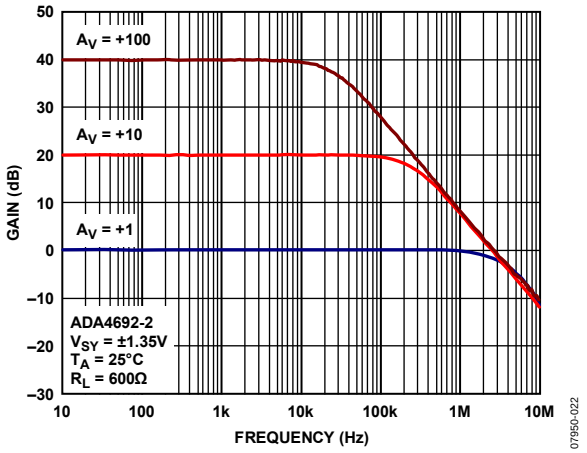

Figure 17. Closed-Loop Gain vs. Frequency

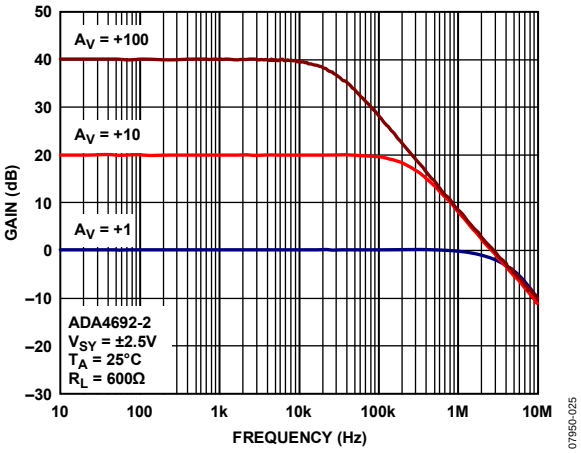

Figure 20. Closed-Loop Gain vs. Frequency

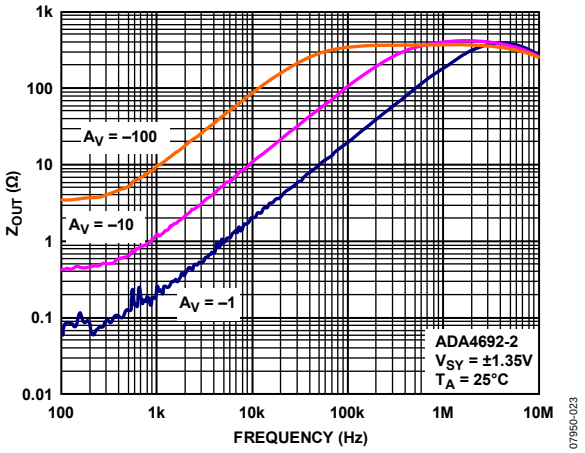

Figure 21. Output Impedance vs. Frequency

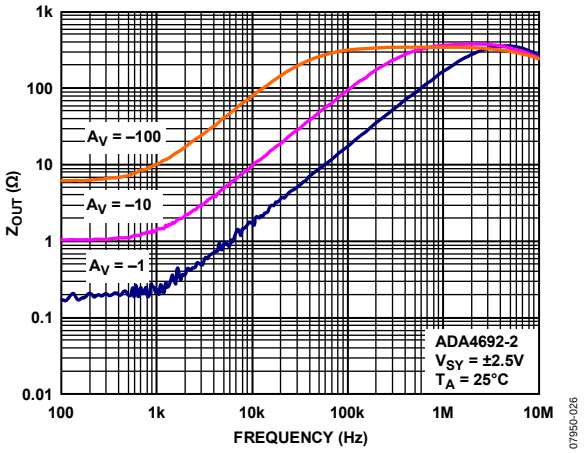

Figure 24. Output Impedance vs. Frequency

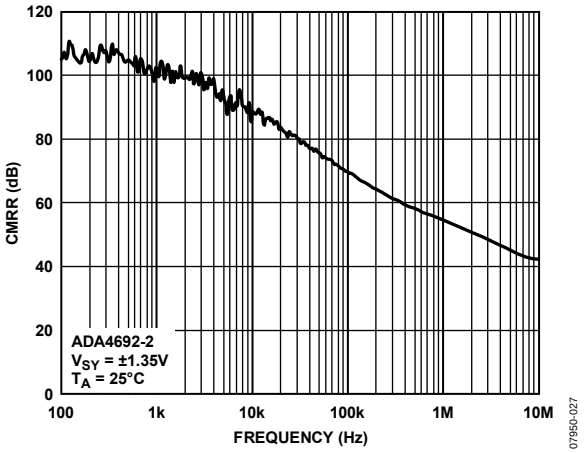

Figure 22. CMRR vs. Frequency

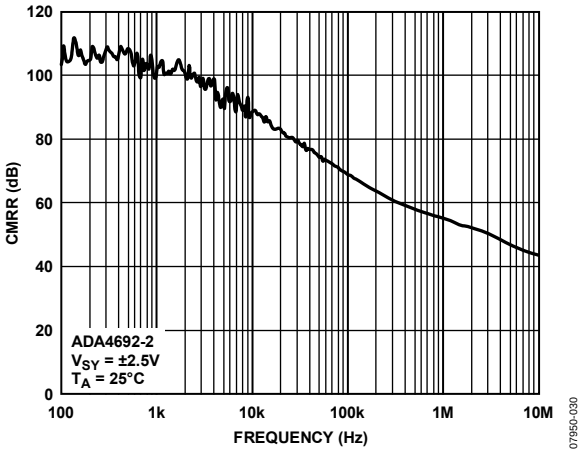

Figure 25. CMRR vs. Frequency

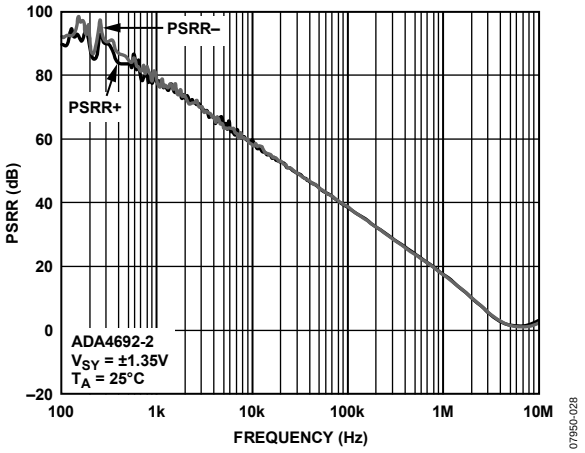

Figure 23. PSRR vs. Frequency

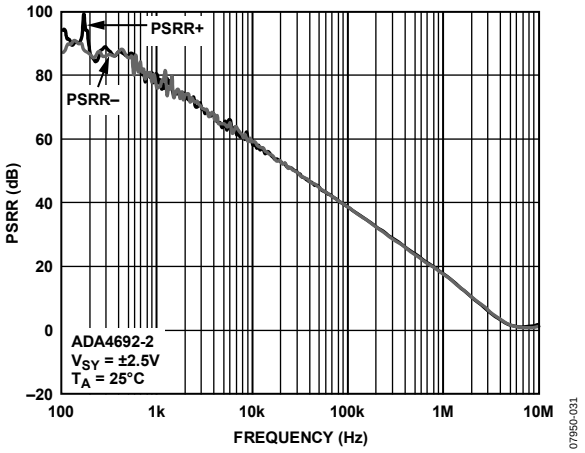

Figure 26. PSRR vs. Frequency

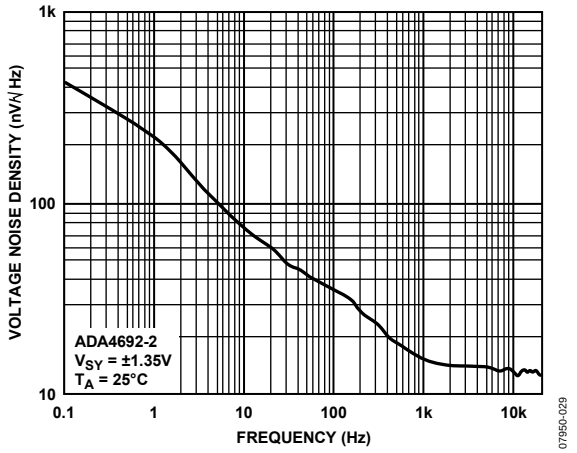

Figure 27. Voltage Noise Density vs. Frequency

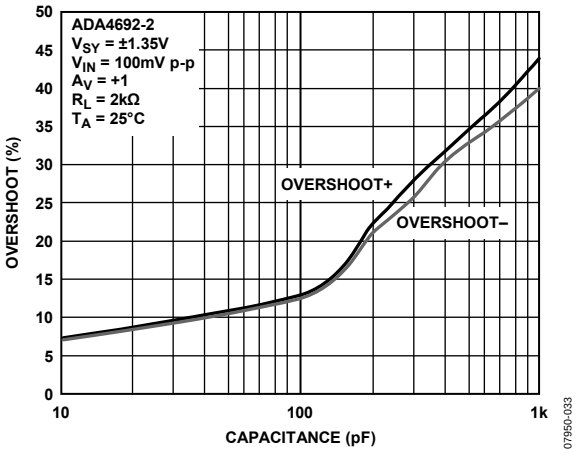

Figure 28. Small Signal Overshoot vs. Load Capacitance

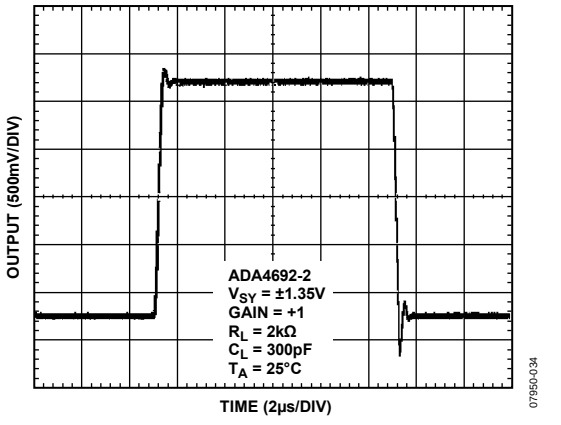

Figure 29. Large Signal Transient Response

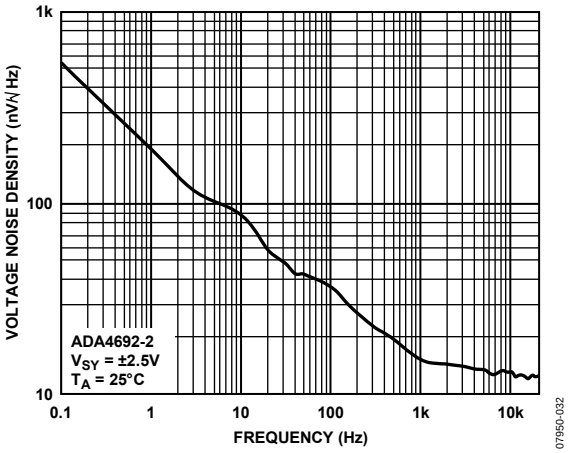

Figure 30. Voltage Noise Density vs. Frequency

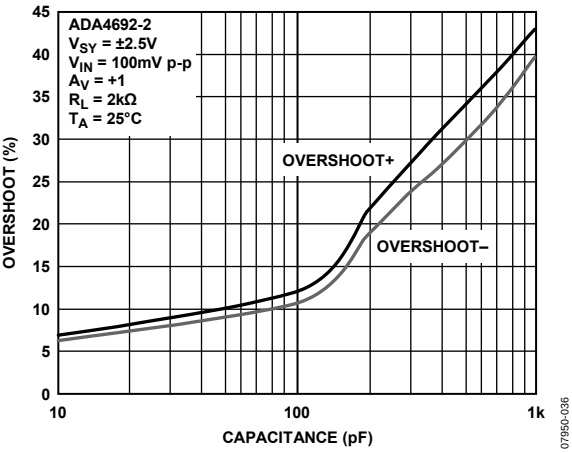

Figure 31. Small Signal Overshoot vs. Load Capacitance

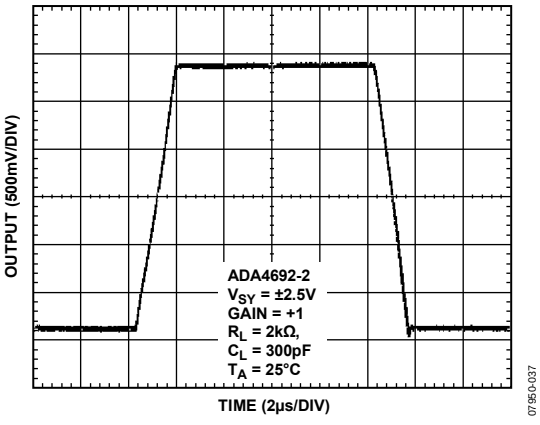

Figure 32. Large Signal Transient Response

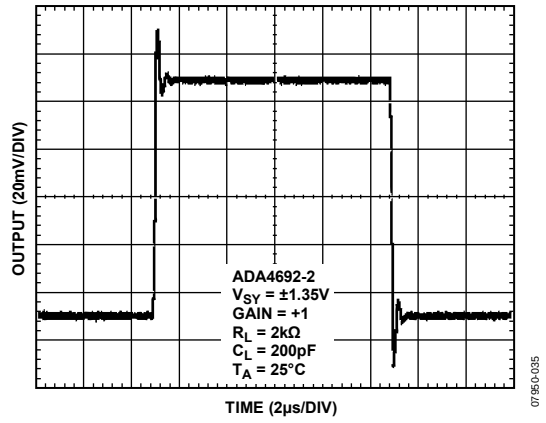

Figure 33. Small Signal Transient Response

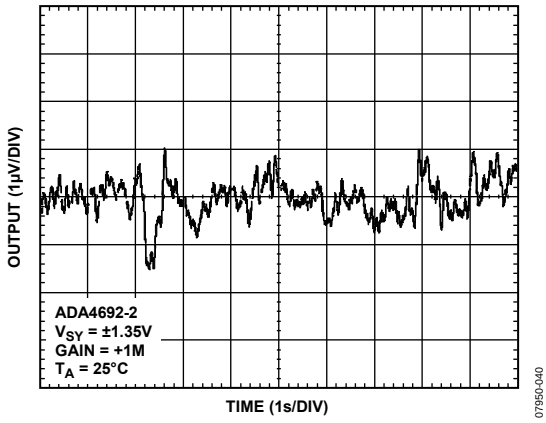

Figure 34. 0.1 Hz to 10 Hz Noise

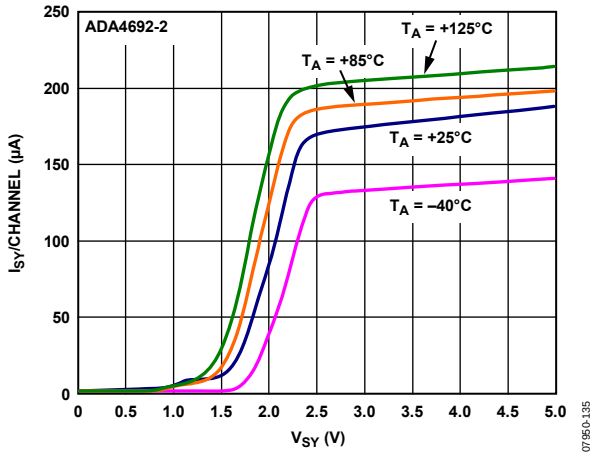

Figure 35. Supply Current per Amplifier vs. Supply Voltage

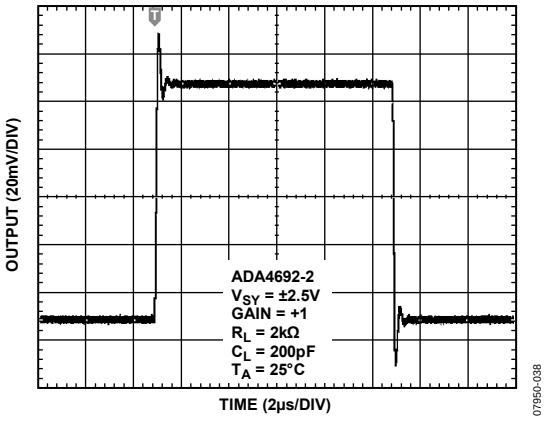

Figure 36. Small Signal Transient Response

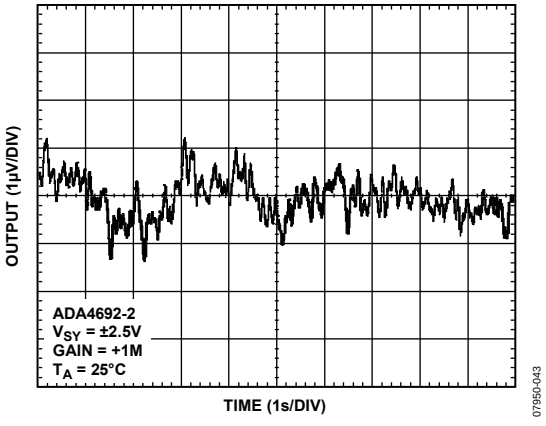

Figure 37. 0.1 Hz to 10 Hz Noise

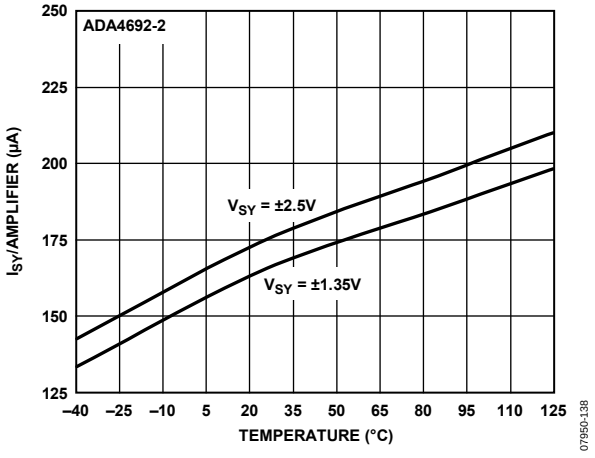

Figure 38. Supply Current per Channel vs. Temperature

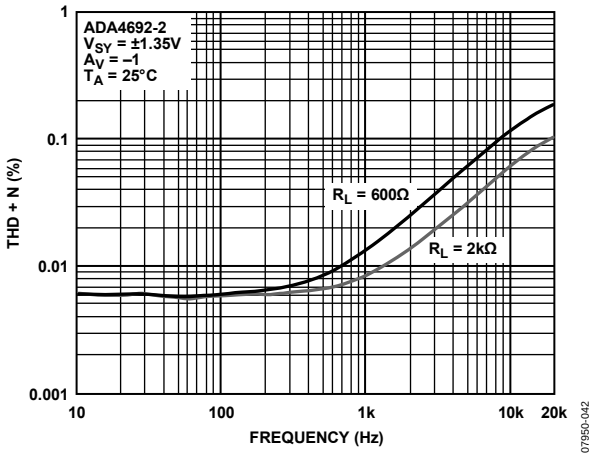

Figure 39. THD + Noise vs. Frequency

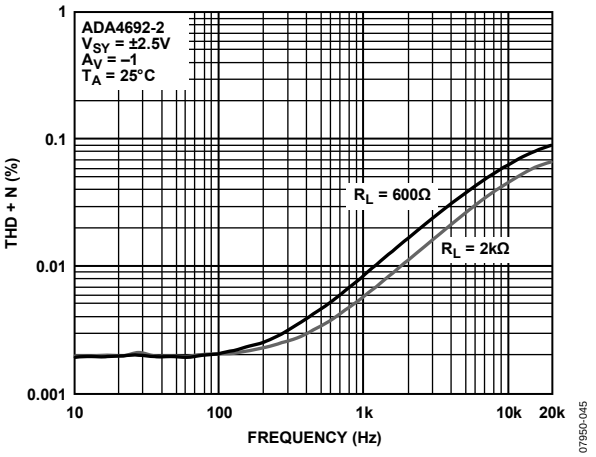

Figure 42. THD + Noise vs. Frequency

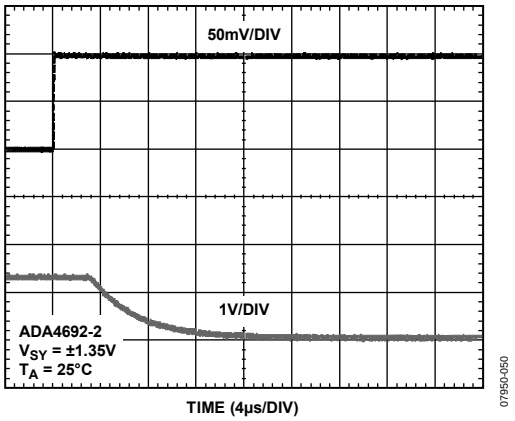

Figure 40. Positive Overload Recovery

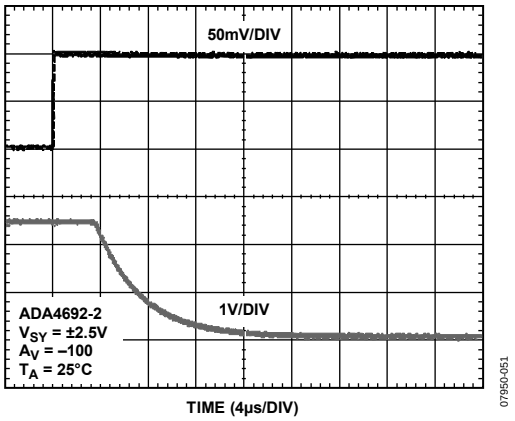

Figure 43. Positive Overload Recovery

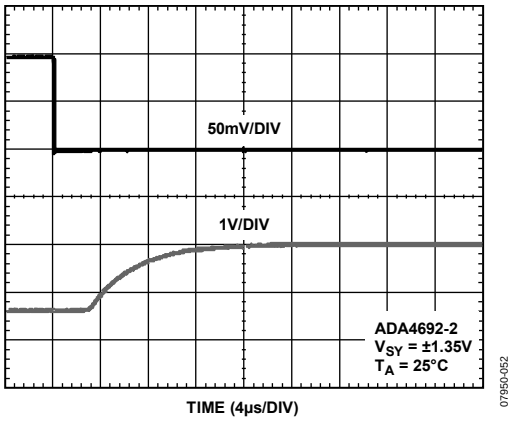

Figure 41. Negative Overload Recovery

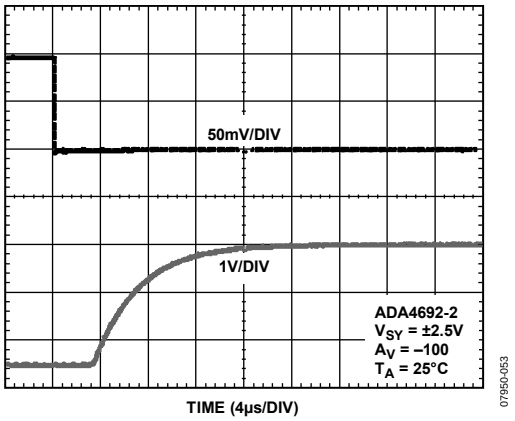

Figure 44. Negative Overload Recovery

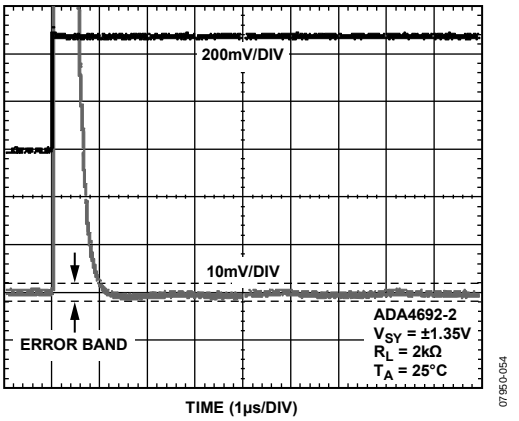

Figure 45. Positive Settling Time to 0.1%

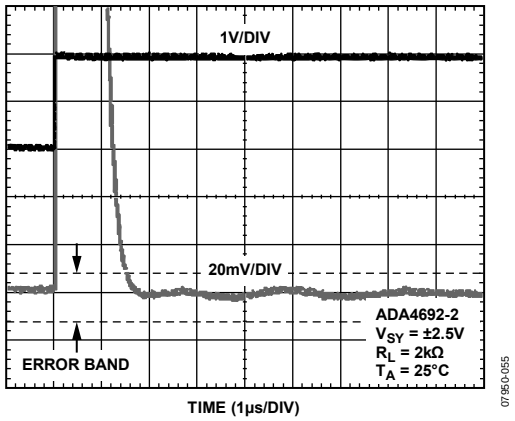

Figure 48. Positive Settling Time to 0.1%

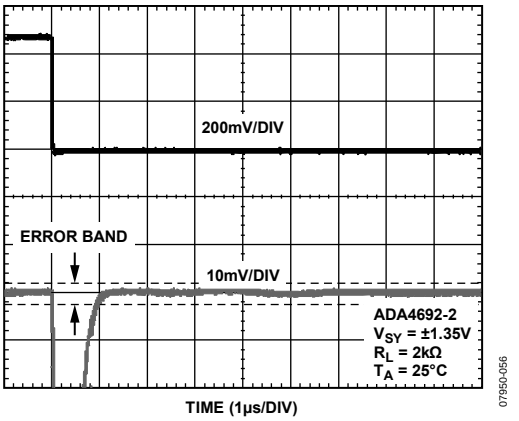

Figure 46. Negative Settling Time to 0.1%

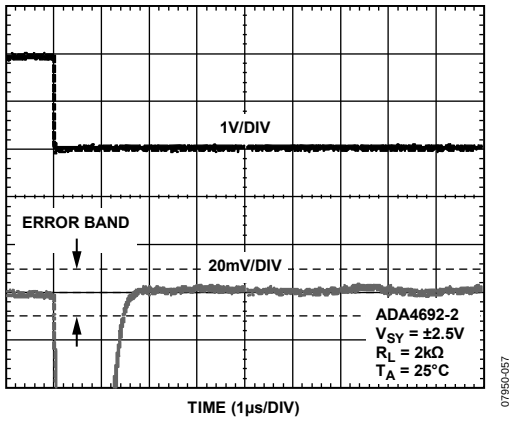

Figure 49. Negative Settling Time to 0.1%

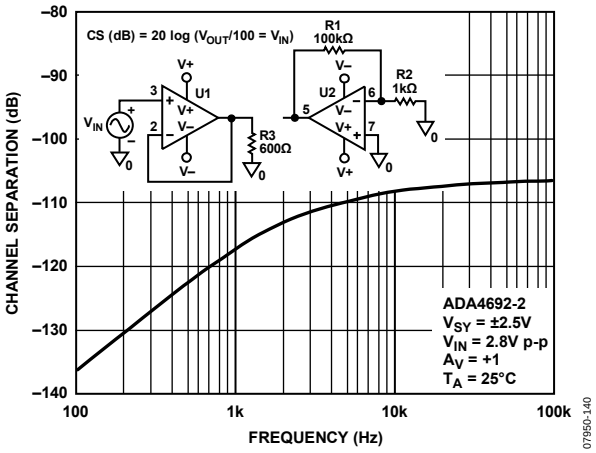

Figure 47. Channel Separation vs. Frequency

SHUTDOWN OPERATION

INPUT PIN CHARACTERISTICS

The ADA4691-2 has a classic CMOS logic inverter input for each shutdown pin, as shown in Figure 50.

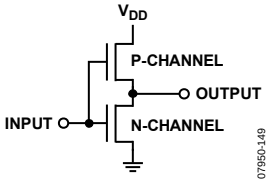

Figure 50. CMOS Inverter

With slowly changing inputs, the top transistor and bottom transistor may be slightly on at the same time, increasing the supply current. This can be avoided by driving the input with a digital logic output having fast rise and fall times. Figure 51 through Figure 53 show the supply current for both sections switching simultaneously with rise times of 1 µs, 10 µs, and 1 ms. Clearly, the rise and fall times should be faster than 10 us. Using an RC time constant to enable/disable shutdown is not recommended.

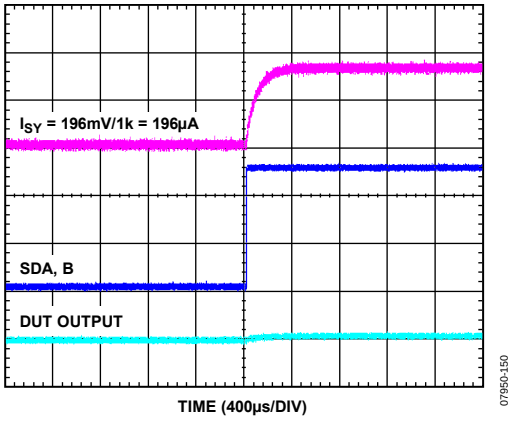

Figure 51. Shutdown Pin Rise Time = 1 µs

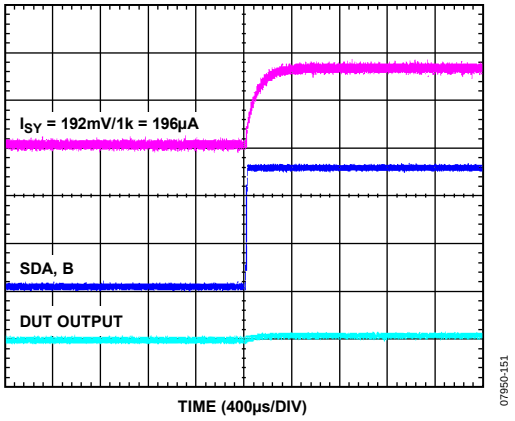

Figure 52. Shutdown Pin Rise Time = 10 µs

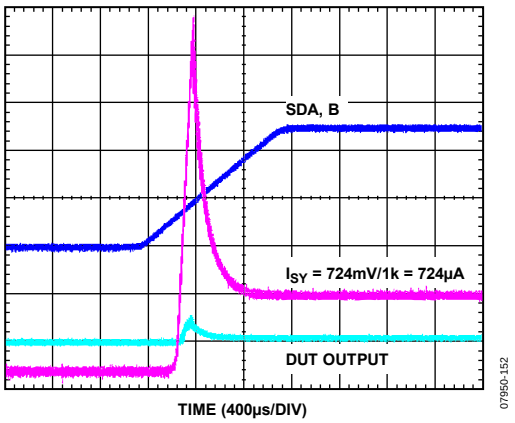

Figure 53. Shutdown Pin Rise Time = 1 ms

INPUT THRESHOLD

The input threshold is approximately 1.2 V above the V− pin when operating on ground and +5 V, and 0.9 V when operating on 2.7 V (see Figure 54 and Figure 55). The threshold is relatively stable over temperature. For operation on split supplies, the logic swing may have to be level shifted.

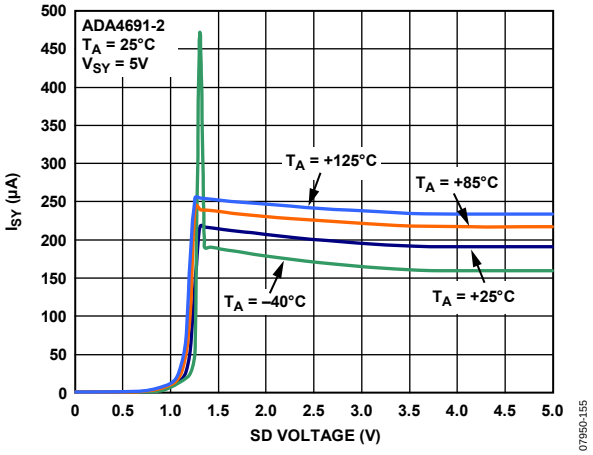

Figure 54. Supply Current vs. Temperature, V_{SY} = 5 V

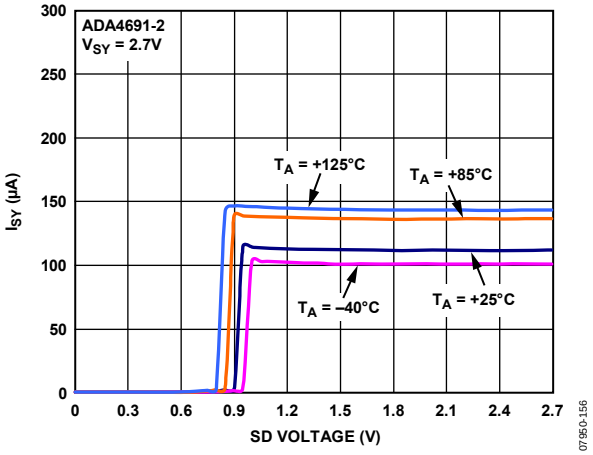

Figure 55. Supply Current vs. Temperature, V_{SY} = 2.7 V

OUTLINE DIMENSIONS

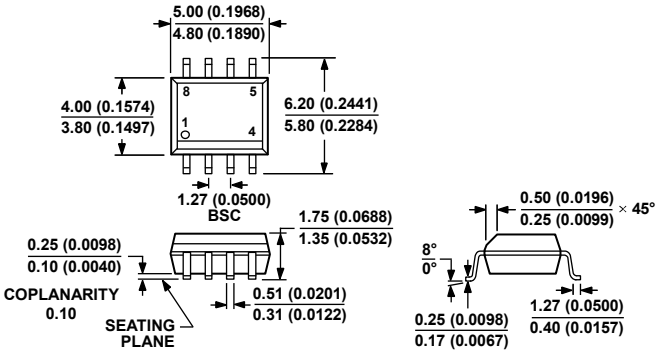

Figure 56. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

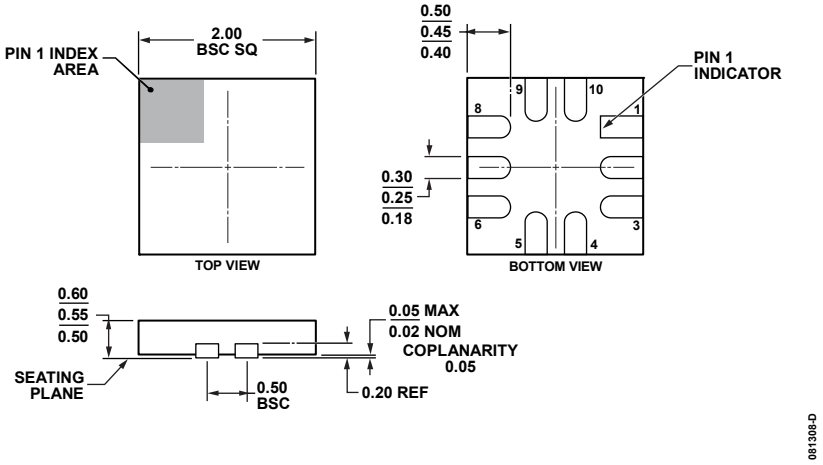

Figure 57. 10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
2 mm × 2 mm Body, Ultra Thin Quad
(CP-10-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Code
ADA4691-2ACPZ-R7[1]	−40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4691-2ACPZ-RL[1]	−40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4691-2ACPZ-R2[1]	−40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4692-2ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

D07950-0-6/09(A)