

# AS1360

## 1.5µA Low-Power, Positive Voltage Regulator

### 1 General Description

The AS1360 low-power, positive voltage regulator was designed to deliver up to 250mA while consuming only 1.5µA of quiescent current. The device is available in fixed output voltages of 1.8, 2.1, 2.5, 3.0, 3.3, and 5.0V.

The device features integrated short-circuit and overcurrent protection.

The wide input voltage range, low-dropout voltage, and high-accuracy output voltage makes the device perfectly suited for 2- and 3-cell battery-powered and portable applications.

The low dropout voltage (650mV) prolongs battery life and allows high current in small applications when operated with minimum input-to-output voltage differentials.

The device features very stable output voltage (using only 1µF tantalum or aluminum-electrolytic capacitors), strict output voltage regulation tolerances ( $\pm 0.5\%$ ), and excellent line-regulation.

The AS1360 is available in a 3-pin SOT23 package.

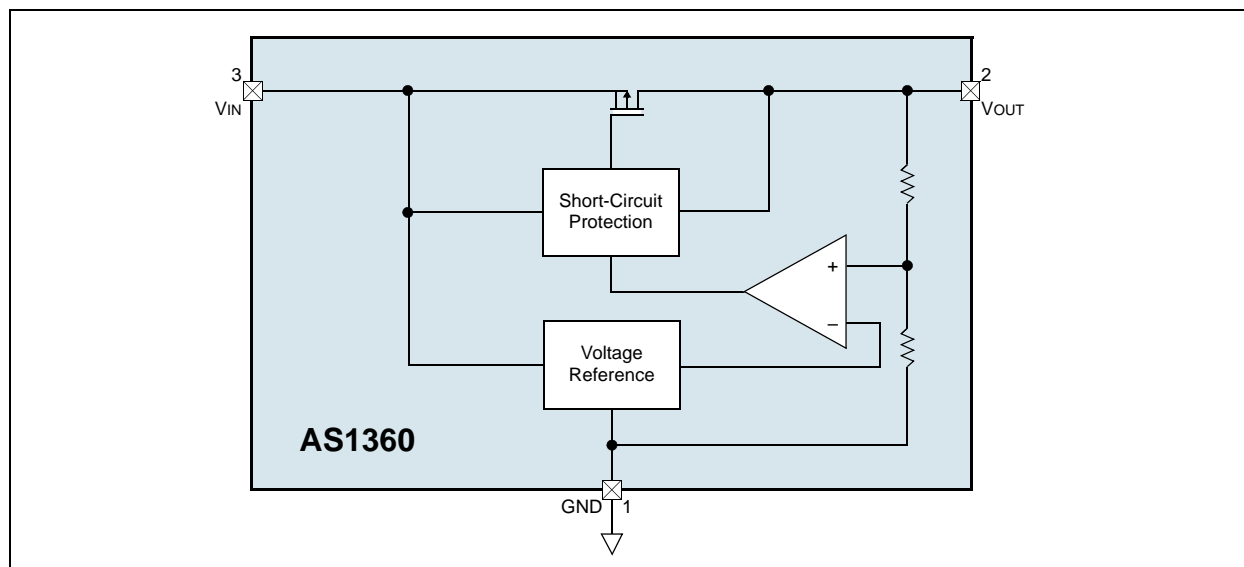
### 2 Key Features

- Low Quiescent Current: 1.5µA
- Input Voltage Range: Up to 20V
- Low Dropout Voltage
  - 250mV @ 100mA
  - 400mV @ 200mA
- Fixed Output Voltages: 1.8, 2.1, 2.5, 3.0, 3.3, 5.0V
- High Output Current: 250mA ( $V_{OUT} = 5.0V$ )
- High-Accuracy Output Voltage:  $\pm 1.5\%$
- Exceptional Line Regulation: 0.1%/V
- Low Temperature Drift:  $\pm 100\text{ppm}/^\circ\text{C}$
- Integrated Short-Circuit and Overcurrent Protection
- 3-pin SOT23 Package

### 3 Applications

The device is ideal for mobile phones, PDAs, digital cameras, smart battery packs, battery-powered alarms, solar-powered instruments, intelligent instruments, CO2 and smoke detectors, CPU power supplies, and any battery-powered application.

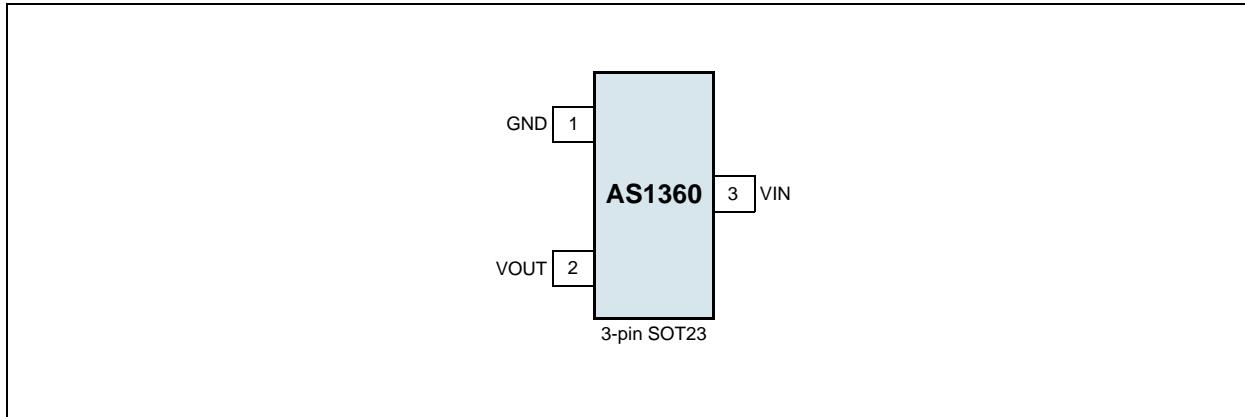
Figure 1. AS1360 - Block Diagram



## 4 Pinout and Packaging

### Pin Assignments

Figure 2. Pin Assignments (Top View)



### Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	GND	<p><b>Ground.</b> This pin should be connected to the negative side of the output and the negative terminal of the input capacitor. No high-current flows out of this pin, only bias current (1.5<math>\mu</math>A, typ).</p> <p><b>Note:</b> Voltage drops between this pin and the negative side of the load should be minimized.</p>
2	VOUT	<p><b>Regulated Output Voltage.</b> This pin should be connected to the positive side of the load and the positive terminal of the output capacitor. Current flowing out of this pin is equivalent DC load current.</p> <p><b>Note:</b> The positive side of the output capacitor should be mounted as close as is practical to this pin.</p>
3	VIN	<p><b>Unregulated Input Voltage.</b> This pin should be connected to the positive terminal of the input capacitor.</p> <p><b>Note:</b> The input capacitor should be mounted as close as is practical to this pin.</p>

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Section 6 Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Input Voltage		+30	V	
Continuous Output Current		PD/ (V <sub>IN</sub> - V <sub>OUT</sub> )	mA	
Peak Output Current		500	mA	
Output Voltage	- 0.3V	V <sub>IN</sub> + 0.3V or +7V	V	Minimum of the two values
Thermal Resistance $\Theta_{JA}$		230	°C/W	Typical FR4, 4-layer application
Operating Temperature Range	-40	+85	°C	
Storage Temperature Range	-40	+125	°C	
Electrostatic Discharge (ESD) Protection Level	1		kV	HBM - Norm: MIL 883 E methode 3015
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in compliance with IPC/JEDEC J-STD-020D "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".

## 6 Electrical Characteristics

$T_{AMB} = +25^{\circ}\text{C}$  (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IN}$	Input Voltage				20	V
$V_{OUT}$	Output Voltage	$I_{OUT} = 40\text{mA}^1$ , $I_{OUT} = 15\text{mA}$ if $V_{OUT} = 1.8\text{V}$	$V_{OUTNOM} - 1.5\%$	$V_{OUTNOM} \pm 0.5\%$	$V_{OUTNOM} + 1.5\%$	V
$I_{OUT(MAX)}$	Maximum Output Current	$V_{OUT} = 5.0\text{V}$ ( $V_{IN} = V_{OUTNOM} + 1.0\text{V}$ )	250			mA
		$V_{OUT} = 3.3\text{V}$	150			
		$V_{OUT} = 3.0\text{V}$	150			
		$V_{OUT} = 2.5\text{V}$	125			
		$V_{OUT} = 2.1\text{V}$	115			
$\Delta V_{OUT}/V_{OUT}$	Load Regulation <sup>2</sup>	$V_{OUT} = 5.0\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 100\text{mA}$	-1.60	$\pm 0.8$	+1.60	%
		$V_{OUT} = 3.3\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 80\text{mA}$	-2.72	$\pm 1.3$	+2.72	
		$V_{OUT} = 3.0\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 80\text{mA}$	-3.00	$\pm 1.5$	+3.00	
		$V_{OUT} = 2.5\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 60\text{mA}$	-3.60	$\pm 1.8$	+3.60	
		$V_{OUT} = 2.1\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 40\text{mA}$	-2.60	$\pm 1.6$	+2.60	
$V_{OUT} = 1.8\text{V}$ , $1\text{mA} \leq I_{OUT} \leq 30\text{mA}$	-1.60	$\pm 0.8$	+1.60			
$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT}}$	Line Regulation	$I_{OUT} = 40\text{mA}$ , ( $V_{OUTNOM} + 1.0$ ) $\leq V_{IN} \leq 10.0\text{V}$		0.1	0.25	%/V
$V_{IN} - V_{OUT}$	Dropout Voltage	$I_{OUT} = 200\text{mA}$ , $V_{OUTNOM} = 5.0\text{V}$		400	630	mV
		$I_{OUT} = 160\text{mA}$ , $V_{OUTNOM} = 3.3\text{V}$		400	700	
		$I_{OUT} = 160\text{mA}$ , $V_{OUTNOM} = 3.0\text{V}$		400	700	
		$I_{OUT} = 120\text{mA}$ , $V_{OUTNOM} = 2.5\text{V}$		400	700	
		$I_{OUT} = 60\text{mA}$ , $V_{OUTNOM} = 2.1\text{V}$		200	500	
$I_{OUT} = 20\text{mA}$ , $V_{OUTNOM} = 1.8\text{V}$		180	300			
$I_Q$	Input Quiescent Current	$V_{IN} = V_{OUTNOM} + 1.0\text{V}$		1.5	3.0	$\mu\text{A}$
$TCV_{OUT}$	Temperature Coefficient of $V_{OUT}$ <sup>3</sup>	$I_{OUT} = 40\text{mA}$ , $-40^{\circ}\text{C} \leq T_{AMB} \leq +85^{\circ}\text{C}$		$\pm 100$		ppm/ $^{\circ}\text{C}$
$t_R$	Output Rise Time	10% $V_{OUTNOM}$ to 90% $V_{OUTNOM}$ , $V_{IN} = 0\text{V}$ to $V_{OUTNOM} + 1\text{V}$ , $R_{LOAD} = 25\Omega$ resistive		150		$\mu\text{s}$

1.  $V_{OUTNOM}$  is the nominal device output voltage.
2. Measured at a constant junction temperature using low duty cycle pulse testing.
3.  $TCV_{OUT} = (V_{OH} - V_{OL}) \times 10^6 / (V_{OUTNOM} \times \text{Temperature})$ .

**Where:**

$V_{OH}$  is the highest voltage measured over the device temperature range.

$V_{OL}$  is the lowest voltage over the device temperature range.

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

## 7 Typical Operating Characteristics

$V_{OUT} = 3.3V$ ,  $I_{LOAD} = 100\mu A$ ,  $V_{IN} = 4.3V$ ,  $C_{IN} = 1\mu F$  (tantalum),  $C_{OUT} = 1\mu F$  (tantalum),  $T_{AMB} = +25^\circ C$  (unless otherwise specified).

Figure 3. Supply Current vs. Input Voltage

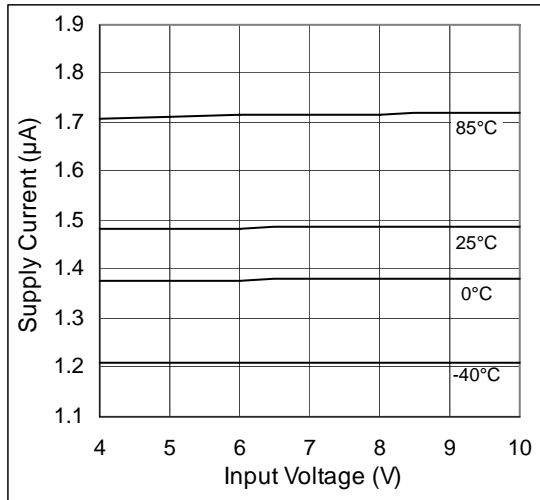


Figure 4. Supply Current vs. Load Current

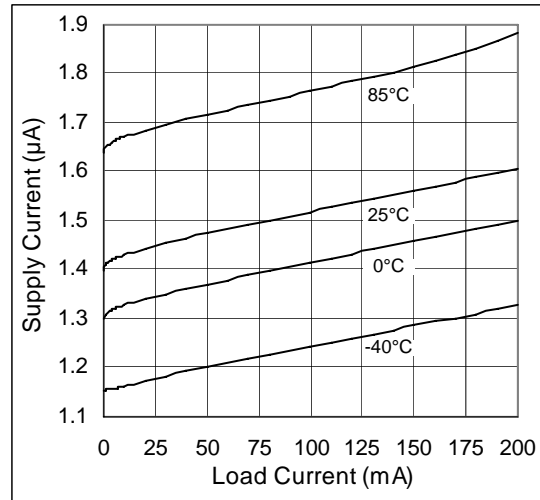


Figure 5. Supply Current vs. Temperature

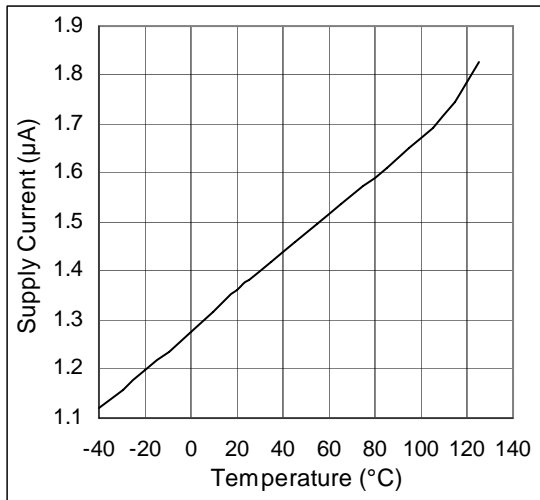


Figure 6. Output Voltage vs. Input Voltage

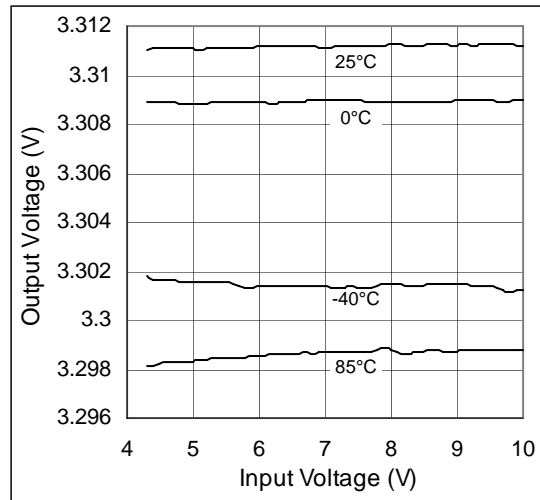


Figure 7. Output Voltage vs. Load Current

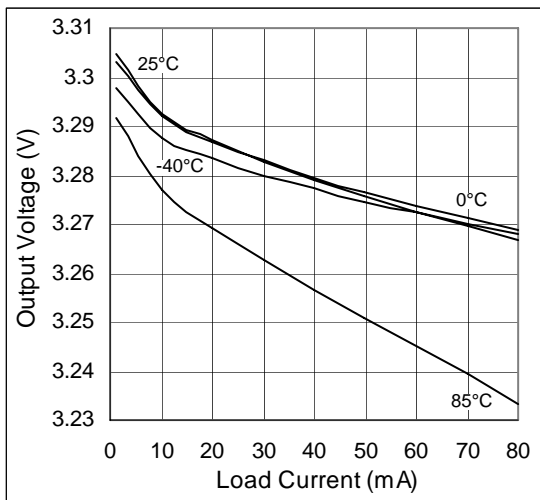


Figure 8. Dropout Voltage vs. Load Current

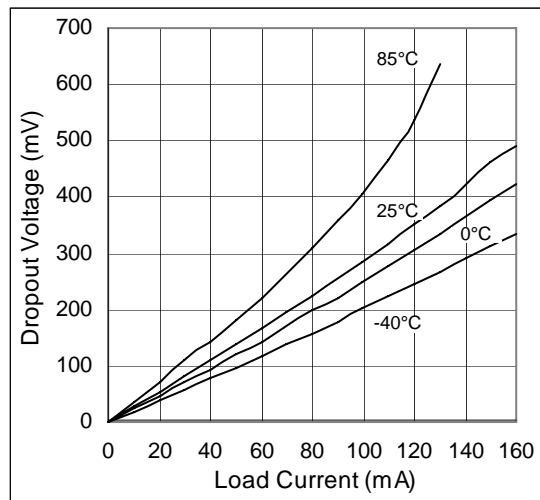


Figure 9. Load Regulation vs. Temperature

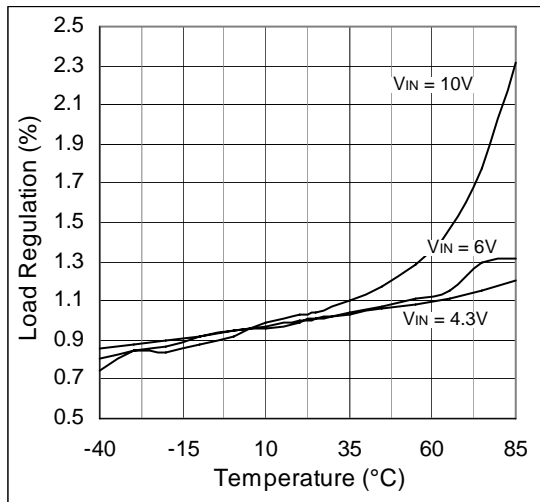


Figure 10. Line Regulation vs. Temperature

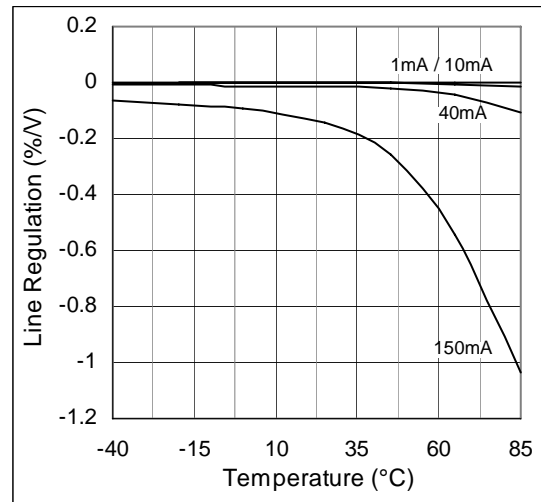


Figure 11. Output Voltage vs. Input Voltage; Dropout

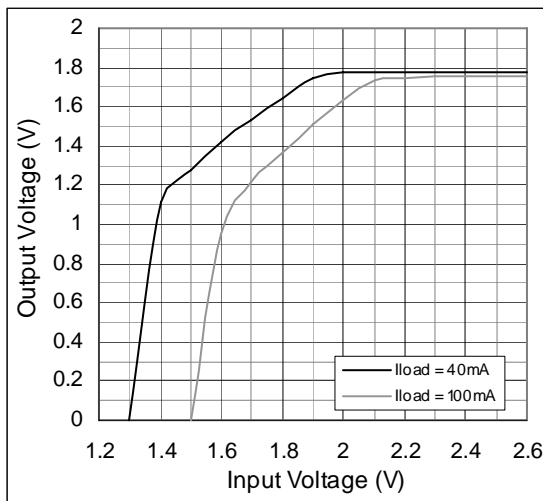


Figure 12. Startup Rise Time

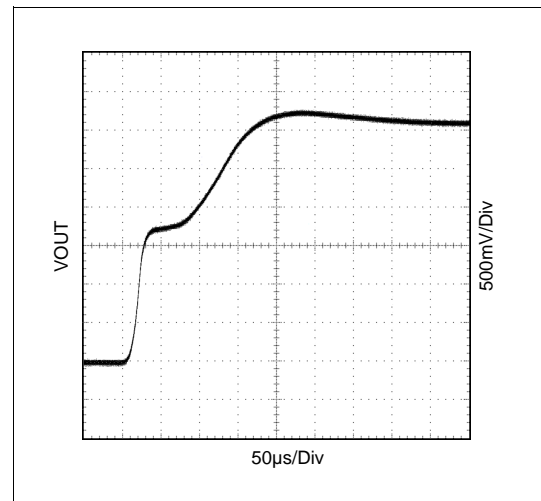
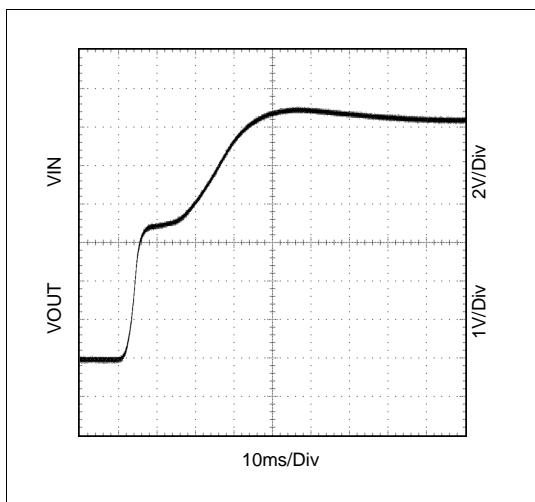


Figure 13. Startup Delay



**Note:** All graphs were measured without additional heat sinks, with the SOT23 package mounted on a 4-layer PCB. Adding additional heat sinks will improve performance in high temperature environment.

## 8 Detailed Description

The AS1360 is a low-power, positive voltage regulator designed in such a way that the supply current is independent from the load current. The device regulates the output by comparing the output voltage to an internally generated reference voltage.

The device is available in fixed output voltages of 1.8, 2.5, 3.0, 3.3, and 5.0V. Fixed output voltages are generated using the internal resistor divider network (see [Figure 1 on page 1](#)).

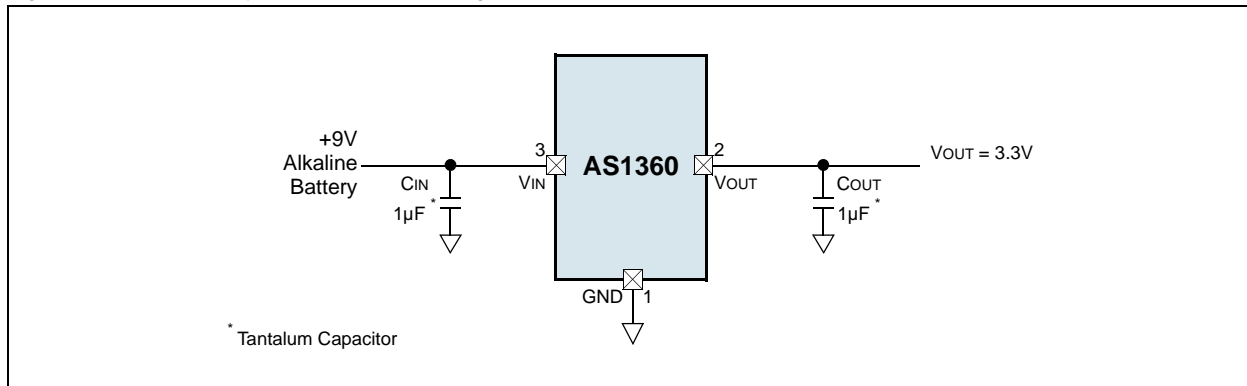
### Short Circuit/Overcurrent Protection

The AS1360 monitors current flow through the p-channel MOSFET. In short-circuit or overcurrent conditions, the integrated short-circuit protection circuitry will limit output current.

**Note:** Thermal Dissipation according to [Absolute Maximum Ratings on page 3](#) must be considered.

## 9 Application Information

Figure 14. AS1360 - Typical Application Diagram



### Power Dissipation

Power dissipation (PD) of the AS1360 is the sum of the power dissipated by the p-channel MOSFET and the quiescent current required to bias the internal voltage reference and the internal power amplifier, and is calculated as:

$$PD \text{ (P-Channel MOSFET)} = (V_{IN} - V_{OUT})I_{OUT} \quad (\text{EQ 1})$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD \text{ (Bias)} = V_{IN}I_{GND} \quad (\text{EQ 2})$$

Total AS1360 power dissipation is calculated as:

$$PD(\text{Total}) = PD \text{ (P-Channel MOSFET)} + PD \text{ (Bias)} \quad (\text{EQ 3})$$

The internal quiescent bias current (2µA, typ) is such that the PD(Bias) term of (EQ 3) can be disregarded and the maximum power dissipation can be estimated using  $V_{IN(\text{MAX})}$  and  $V_{OUT(\text{MIN})}$  to obtain a maximum voltage differential between  $V_{IN}$  and  $V_{OUT}$ , and multiplying the maximum voltage differential by the maximum output current:

$$PD = (V_{IN(\text{MAX})} - V_{OUT(\text{MIN})})I_{OUT(\text{MAX})} \quad (\text{EQ 4})$$

#### Where:

$V_{IN} = 3.3$  to  $4.1\text{V}$

$V_{OUT} = 3.0\text{V} \pm 2\%$

$I_{OUT} = 1$  to  $100\text{mA}$

$T_{AMB(\text{MAX})} = 55^\circ\text{C}$

$P_{MAX} = (4.1\text{V} - (3.0\text{V} \times 0.98)) \times 100\text{mA} = 116.0\text{mW}$

### Junction Temperature

The AS1360 junction temperature ( $T_J$ ) can be determined by first calculating the thermal resistance from junction temperature-to-ambient temperature.

**Note:** Thermal resistance is estimated to be the junction temperature-to-air temperature  $R_{\theta JA}$ , and is approximately  $230^\circ\text{C/W}$  or  $335^\circ\text{C/W}$  (when mounted on 1 square inch of copper).  $R_{\theta JA}$  will vary depending on PCB layout, air-flow and application specific conditions.

The AS1360 junction temperature is determined by calculating the rise in  $T_J$  above  $T_{AMB}$ , and then adding the increase of  $T_{AMB}$ :

$$T_J = PD(\text{MAX}) \times R_{\theta JA} + T_{AMB} \quad (\text{EQ 5})$$

From (EQ 5), the value of  $T_J$  can be calculated as:

$$T_J = 116.0\text{mW} \times 230^\circ\text{C/W} + 55^\circ\text{C}$$

Therefore:

$$T_J = 81.68^\circ\text{C}$$



## External Component Selection

### Input Capacitor

In applications where input impedance is approximately  $10\Omega$ , a  $1\mu\text{F}$  capacitor is sufficient for  $C_{\text{IN}}$  (see Figure 14 on page 8).

In cases where the AS1360 is operated from a battery, or when there is significant distance between the input source to the AS1360, larger values for  $C_{\text{IN}}$  may be required for output stability.

**Note:** For values of  $C_{\text{OUT}} > 1\mu\text{F}$ , the value of  $C_{\text{IN}}$  should be increased to prevent high source-impedance oscillations.

### Output Capacitor

In most applications for the AS1360, a  $1\mu\text{F}$  capacitor ( $\text{ESR} > 0.1\Omega < 5\Omega$ ,  $f_{\text{RES}} > 1\text{MHz}$ ) is sufficient for  $C_{\text{OUT}}$  (see Figure 14 on page 8).

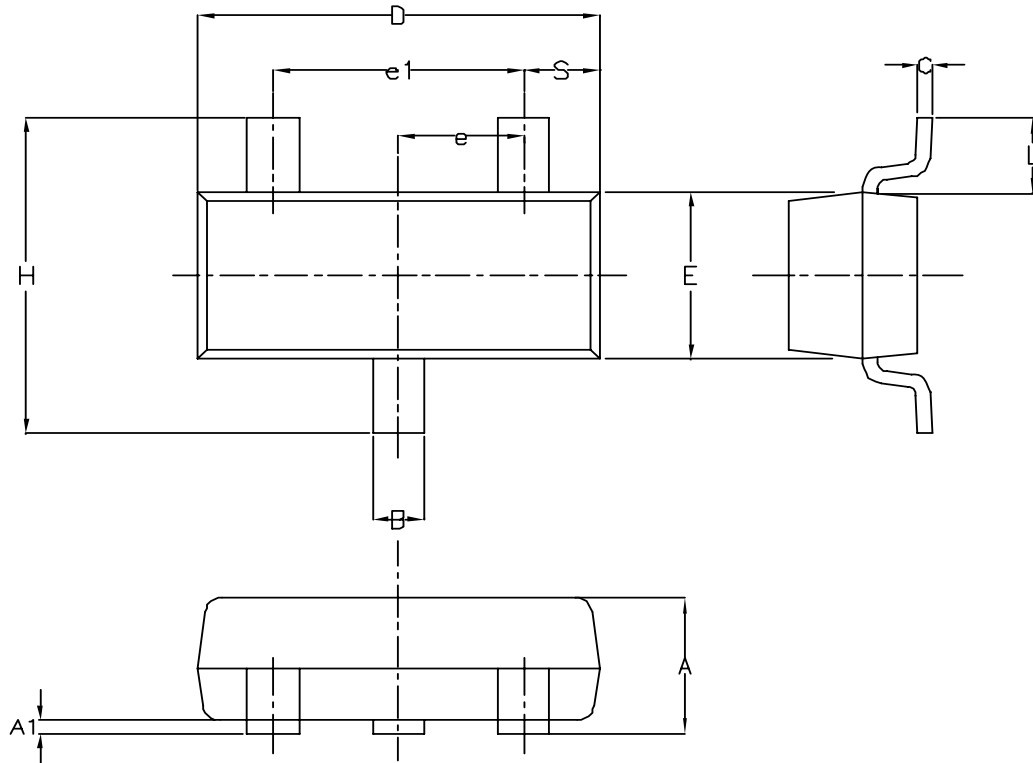
For improved power supply noise rejection and device transient response, larger values can be used for  $C_{\text{OUT}}$ .

**Note:** For values of  $C_{\text{OUT}} > 1\mu\text{F}$ , the input impedance must not be so large that it causes high-input impedance oscillations.

## 10 Package Drawings and Markings

The device is available in an 3-pin SOT23 package.

Figure 15. 3-pin SOT23 Package



### Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004") max.
2. Package surfacing:
  - a. Top: matte (charmillles #18- 30).
  - b. All sides: matte (charmillles #18- 30).
  - c. Bottom: smooth or matte (charmillles #18- 30).
3. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.25mm (.010") per side (D).
4. Details of pin #1 identifier are optional but must be located within the zone indicated.
5. Dimensions are in millimeters.

Symbol	Min	Max
A	0.89	1.12
A1	0.013	0.100
B	0.37	0.51
C	0.085	0.18
D	2.80	3.04
E	1.20	1.40
e	0.89	1.03
e1	1.78	2.05
H	2.10	2.64
L	0.55ref	
A	0.89	1.12
S	0.45	0.60

## 11 Ordering Information

The device is available as the standard products shown in [Table 4](#).

Table 4. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1360-18-T	ASKD	HV low-quiescent current LDO, 1.8V	Tape and Reel	3-pin SOT23
AS1360-21-T	ASRO	HV low-quiescent current LDO, 2.1V	Tape and Reel	3-pin SOT23
AS1360-25-T	ASKE	HV low-quiescent current LDO, 2.5V	Tape and Reel	3-pin SOT23
AS1360-30-T	ASKF	HV low-quiescent current LDO, 3.0V	Tape and Reel	3-pin SOT23
AS1360-33-T	ASKG	HV low-quiescent current LDO, 3.3V	Tape and Reel	3-pin SOT23
AS1360-50-T	ASKH	HV low-quiescent current LDO, 5.0V	Tape and Reel	3-pin SOT23

**Note:** All products are RoHS compliant and Pb-free.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

For further information and requests, please contact us <mailto:sales@austriamicrosystems.com>  
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