

Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	200
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.18
Q_g (Max.) (nC)	70
Q_{gs} (nC)	13
Q_{gd} (nC)	39
Configuration	Single

FEATURES

- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead (Pb)-free Available



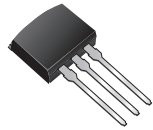
Available
RoHS*
COMPLIANT

DESCRIPTION

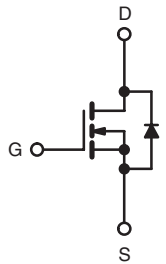
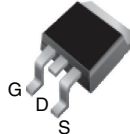
Third generation Power MOSFETs from Vishay provide the designer with the best combinations of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRF640L/SiHF640L) is available for low-profile applications.

I²PAK
(TO-262)



D²PAK
(TO-263)



N-Channel MOSFET

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRF640SPbF SiHF640S-E3	IRF640STRLPbF ^a SiHF6340STL-E3 ^a	IRF640STRRPbF ^a SiHF640STR-E3 ^a	IRF640LPbF SiHF640L-E3
SnPb	IRF640S SiHF640S	IRF640STRL ^a SiHF640STL ^a	IRF640STRR ^a SiHF640STR ^a	IRF640L SiHF640L

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ °C}$	18
		$T_C = 100\text{ °C}$	11
Pulsed Drain Current ^{a, e}			72
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	580	mJ
Avalanche Current ^a	I_{AR}	18	A
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ
Maximum Power Dissipation		$T_C = 25\text{ °C}$	3.1
		$T_A = 25\text{ °C}$	130
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 2.7\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 18\text{ A}$ (see fig. 12).

c. $I_{SD} \leq 18\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ °C}$.

d. 1.6 mm from case.


e. Uses IRF640/SiHF640 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^c$	-	0.29	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 11\text{ A}^b$	-	-	0.18	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 11\text{ A}^d$	6.7	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 ^d	-	1300	-	pF
Output Capacitance	C_{oss}		-	430	-	
Reverse Transfer Capacitance	C_{rss}		-	130	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 18\text{ A}$, $V_{DS} = 160\text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	70	nC
Gate-Source Charge	Q_{gs}		-	-	13	
Gate-Drain Charge	Q_{gd}		-	-	39	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$, $I_D = 18\text{ A}$, $R_G = 9.1\text{ }\Omega$, $R_D = 5.4\text{ }\Omega$, see fig. 10 ^{b, c}	-	14	-	ns
Rise Time	t_r		-	51	-	
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	
Fall Time	t_f		-	36	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	18	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	72	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 18\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 18\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b, c$	-	300	610	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.4	7.1	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Uses IRF640/SiHF640 data and test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

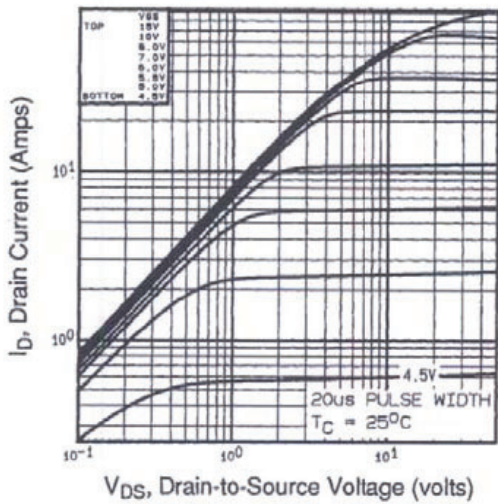


Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ }^\circ\text{C}$

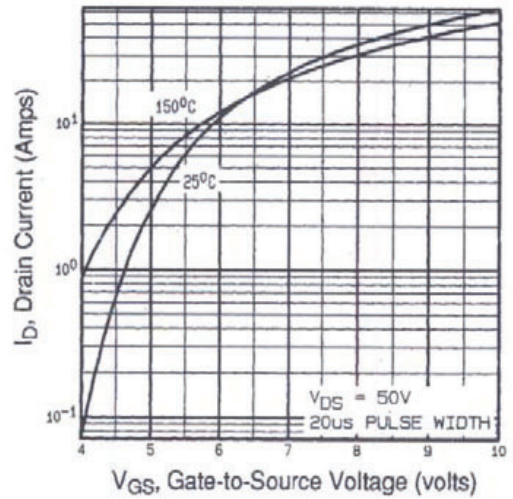


Fig. 3 - Typical Transfer Characteristics

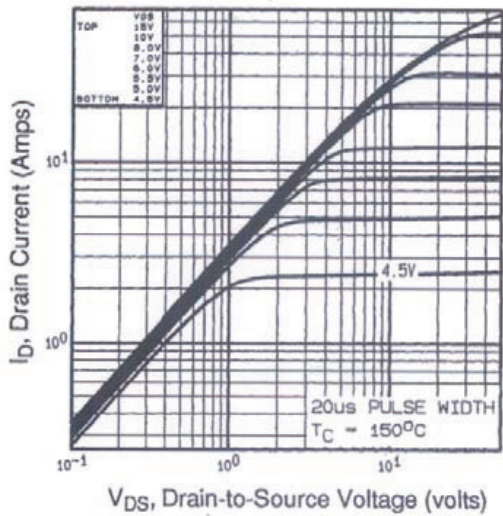


Fig. 2 - Typical Output Characteristics, $T_J = 175\text{ }^\circ\text{C}$

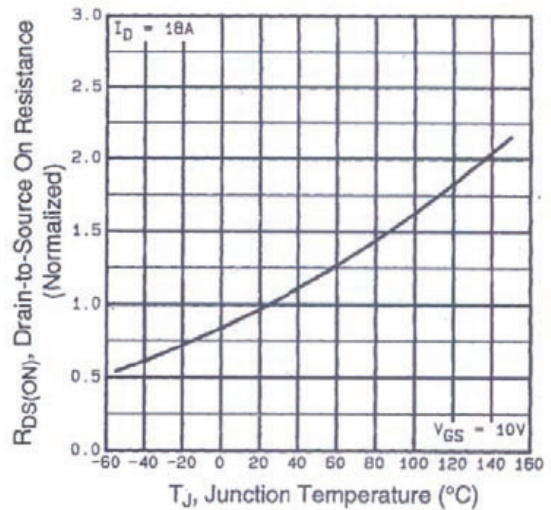


Fig. 4 - Normalized On-Resistance vs. Temperature

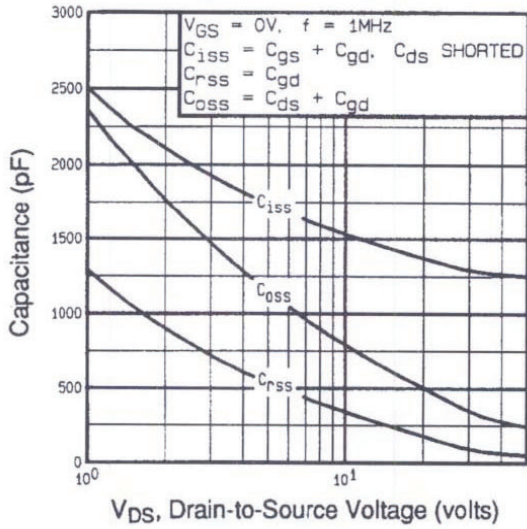


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

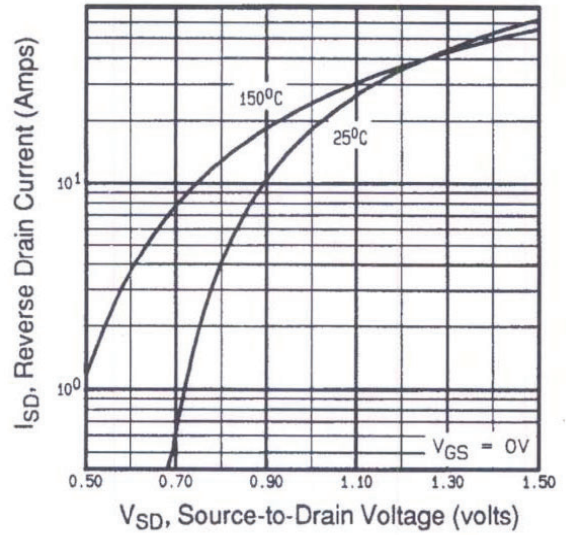


Fig. 7 - Typical Source-Drain Diode Forward Voltage

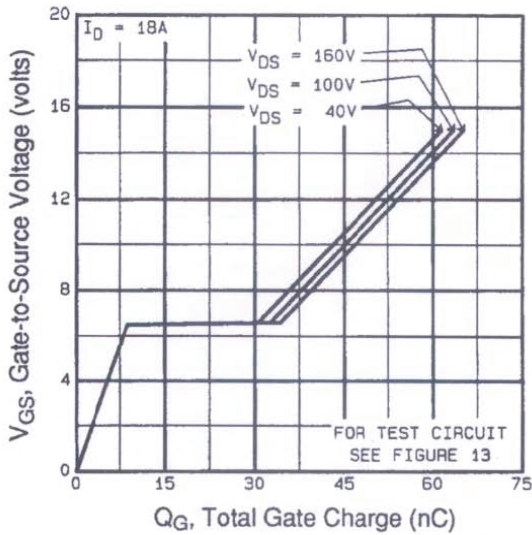


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

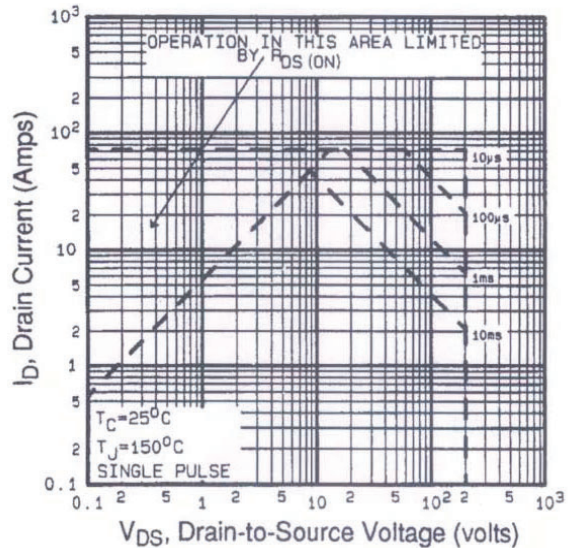


Fig. 8 - Maximum Safe Operating Area

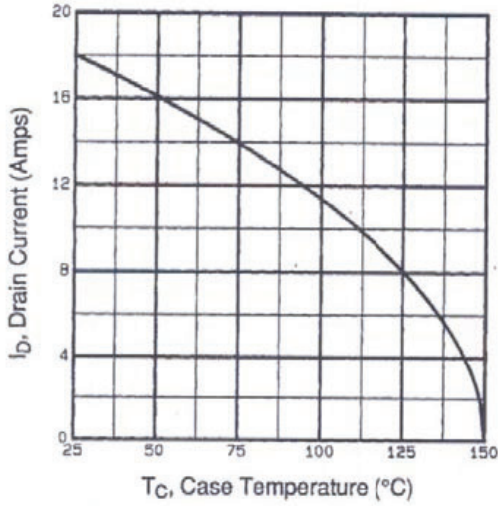


Fig. 9 - Maximum Drain Current vs. Case Temperature

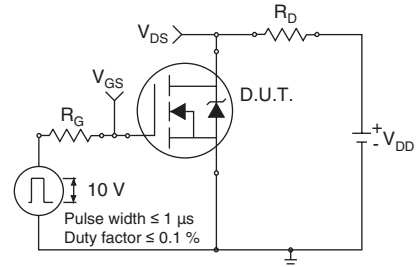


Fig. 10a - Switching Time Test Circuit

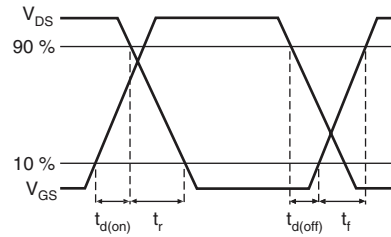


Fig. 10b - Switching Time Waveforms

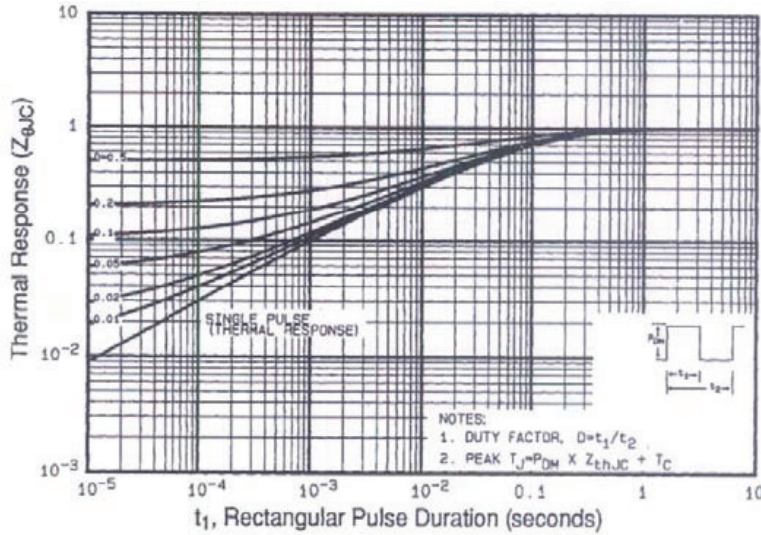


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

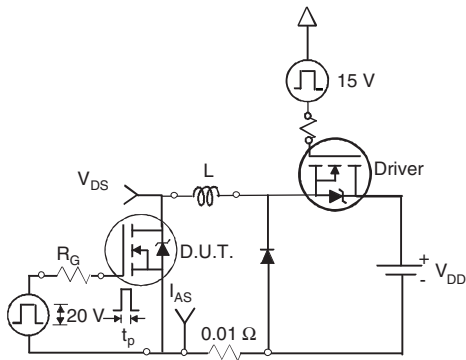


Fig. 12a - Unclamped Inductive Test Circuit

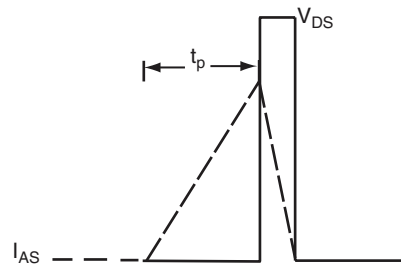


Fig. 12b - Unclamped Inductive Waveforms

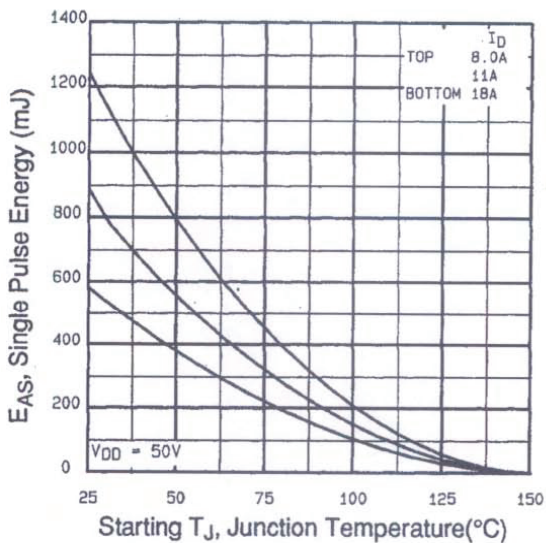


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

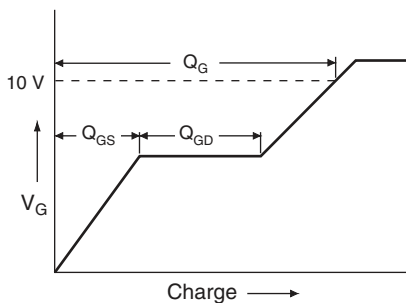


Fig. 13a - Basic Gate Charge Waveform

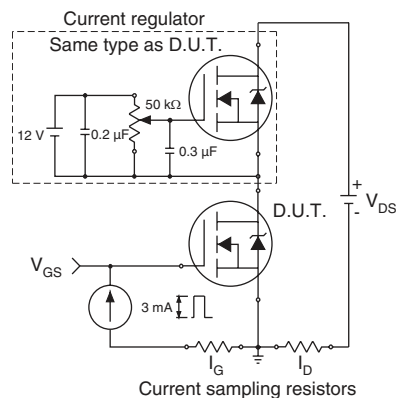


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

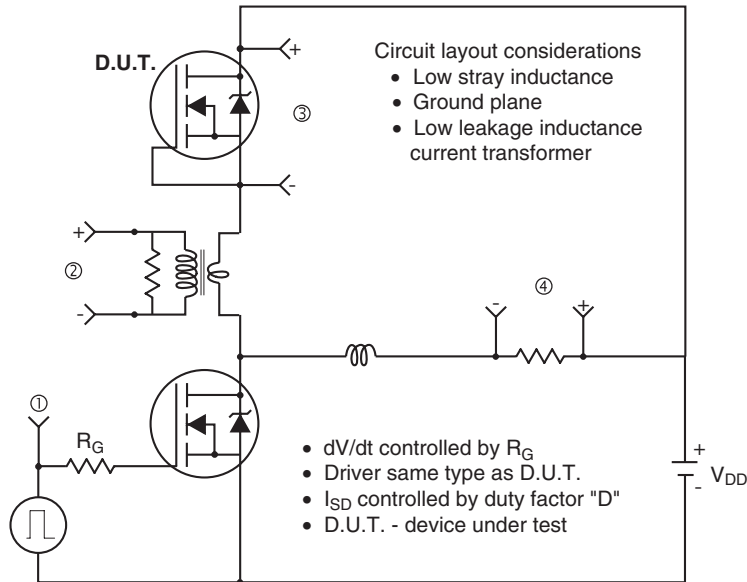


Fig. 14 - For N-Channel

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