FM22LD16

4Mbit F-RAM Memory

Features

4Mbit Ferroelectric Nonvolatile RAM
- Organized as 256Kx16
- Configurable as 512Kx8 Using /UB, /LB
- 10^{14} Read/Write Cycles
- NoDelay™ Writes
- Page Mode Operation to 40MHz
- Advanced High-Reliability Ferroelectric Process

SRAM Compatible
- JEDEC 256Kx16 SRAM Pinout
- 55 ns Access Time, 110 ns Cycle Time

Advanced Features
- Low V_{DD} Monitor Protects Memory against Inadvertent Writes
- Software Programmable Block Write Protect

Superior to Battery-backed SRAM Modules
- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration

Low Power Operation
- 2.7V – 3.6V Power Supply
- Low Standby Current (90µA typ.)
- Low Active Current (8 mA typ.)

Industry Standard Configuration
- Industrial Temperature -40° C to +85° C
- 48-ball "Green"/RoHS FBGA package

Description

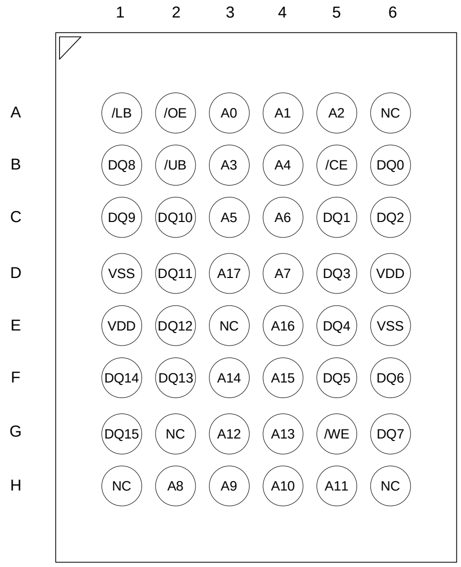
The FM22LD16 is a 256Kx16 nonvolatile memory that reads and writes like a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 10 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

In-system operation of the FM22LD16 is very similar to other RAM devices and can be used as a drop-in replacement for standard SRAM. Read and write cycles may be triggered by /CE or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM22LD16 ideal for nonvolatile memory applications requiring frequent or rapid writes in the form of an SRAM.

The FM22LD16 includes a low voltage monitor that blocks access to the memory array when V_{DD} drops below a critical threshold. The memory is protected against an inadvertent access and data corruption under this condition. The device also features software-controlled write protection. The memory array is divided into 8 uniform blocks, each of which can be individually write protected.

The device is available in a 48-ball FBGA package. Device specifications are guaranteed over industrial temperature range –40°C to +85°C.

Pin Configuration



	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	NC
B	DQ8	/UB	A3	A4	/CE	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	VSS	DQ11	A17	A7	DQ3	VDD
E	VDD	DQ12	NC	A16	DQ4	VSS
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	NC	A12	A13	/WE	DQ7
H	NC	A8	A9	A10	A11	NC

Top View (Ball Down)

Ordering Information	
FM22LD16-55-BG	55 ns access, 48-ball "Green"/RoHS FBGA

This is a product that has fixed target specifications but are subject to change pending characterization results.

Rev. 1.0
Oct. 2008

Ramtron International Corporation
1850 Ramtron Drive, Colorado Springs, CO 80921
(800) 545-FRAM, (719) 481-7000
http://www.ramtron.com

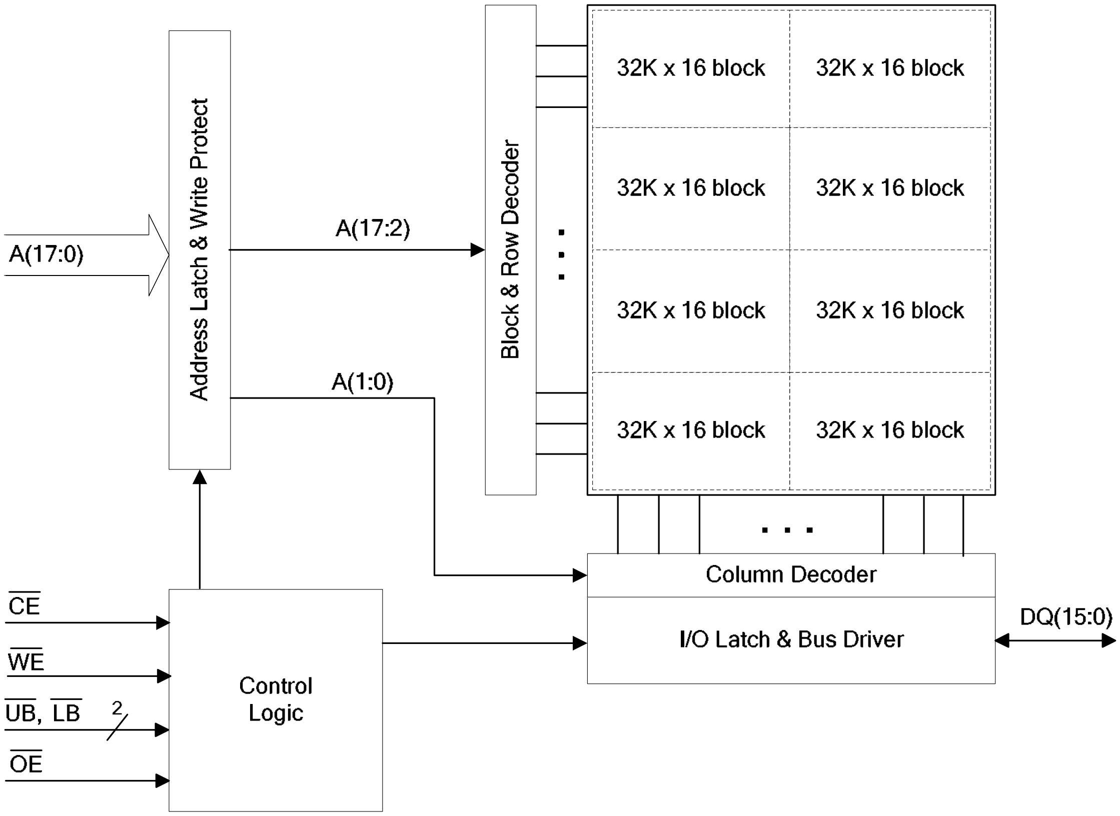


Figure 1. Block Diagram

Pin Description

Pin Name	**Type**	**Pin Description**
A(17:0)	Input	Address inputs: The 18 address lines select one of 262,144 words in the F-RAM array. The lowest two address lines A(1:0) may be used for page mode read and write operations.
/CE	Input	Chip Enable input: The device is selected and a new memory access begins when /CE is low. The entire address is latched internally on the falling edge of /CE. Subsequent changes to the A(1:0) address inputs allow page mode operation when /CE is low.
/WE	Input	Write Enable: A write cycle begins when /WE is asserted. The rising edge causes the FM22LD16 to write the data on the DQ bus to the F-RAM array. The falling edge of /WE latches a new column address for page mode write cycles.
/OE	Input	Output Enable: When /OE is low, the FM22LD16 drives the data bus when valid read data is available. Deasserting /OE high tri-states the DQ pins.
DQ(15:0)	I/O	Data: 16-bit bi-directional data bus for accessing the F-RAM array.
/UB	Input	Upper Byte Select: Enables DQ(15:8) pins during reads and writes. These pins are hi-Z if /UB is high.
/LB	Input	Lower Byte Select: Enables DQ(7:0) pins during reads and writes. These pins are hi-Z if /LB is high.
VDD	Supply	Supply Voltage: 3.3V
VSS	Supply	Ground

Functional Truth Table [1,2]

/CE	/WE	A(17:2)	A(1:0)	Operation
H	X	X	X	Standby/Idle
↓	H	V	V	Read
L	H	No Change	Change	Page Mode Read
L	H	Change	V	Random Read
↓	L	V	V	/CE-Controlled Write
L	↓	V	V	/WE-Controlled Write [2]
L	↓	No Change	V	Page Mode Write [3]
↑	X	X	X	Starts Precharge

Notes:

1) H=Logic High, L=Logic Low, V=Valid Data, X=Don't Care.
2) /WE-controlled write cycle begins as a Read cycle and A(17:2) is latched then.
3) Addresses A(1:0) must remain stable for at least 10 ns during page mode operation.
4) For write cycles, data-in is latched on the rising edge of /CE or /WE, whichever comes first.

Byte Select Truth Table

/OE	/LB	/UB	Operation
H	X	X	Read; Outputs Disabled
X	H	H	
L	H	L	Read; DQ(7:0) Hi-Z
	L	H	Read; DQ(15:8) Hi-Z
	L	L	Read
X	H	L	Write; Mask DQ(7:0)
	L	H	Write; Mask DQ(15:8)
	L	L	Write

Overview

The FM22LD16 is a wordwide F-RAM memory logically organized as 262,144 x 16 and accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation which provides higher speed access to addresses within a page (row). An access to a different page requires that either /CE transitions low or the upper address A(17:2) changes.

Memory Operation

Users access 262,144 memory locations, each with 16 data bits through a parallel interface. The F-RAM array is organized as 8 blocks each having 8192 rows. Each row has 4 column locations, which allows fast access in page mode operation. Once an initial address has been latched by the falling edge of /CE, subsequent column locations may be accessed without the need to toggle /CE. When /CE is deasserted high, a precharge operation begins. Writes occur immediately at the end of the access with no delay. The /WE pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay™ writes.

Read Operation

A read operation begins on the falling edge of /CE. The falling edge of /CE causes the address to be latched and starts a memory read cycle if /WE is high. Data becomes available on the bus after the access time has been satisfied. Once the address has been latched and the access completed, a new access to a random location (different row) may begin while /CE is still low. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM22LD16's /CE-initiated access time is faster than the address cycle time.

The FM22LD16 will drive the data bus when /OE and at least one of the byte enables (/UB, /LB) is asserted low. The upper data byte is driven when /UB is low, and the lower data byte is driven when /LB is low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is deasserted high, the data bus will remain in a high-Z state.

Write Operation

Writes occur in the FM22LD16 in the same time interval as reads. The FM22LD16 supports both /CE- and /WE-controlled write cycles. In both cases, the address A(17:2) is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM22LD16 will not drive the data bus regardless of the state of /OE as long as /WE is low. Input data must be valid when /CE is deasserted high. In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if /OE is low, however it will hi-Z once /WE is asserted low. The /CE- and /WE-controlled write timing cases are shown in the Electrical Specifications section.

Write access to the array begins on the falling edge of /WE after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever comes first. A valid write operation requires the user to meet the access time specification prior to deasserting /WE or /CE. Data setup time indicates the interval during which data cannot change prior to the end of the write access (rising edge of /WE or /CE).

Unlike other truly nonvolatile memory technologies, there is no write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The F-RAM array is organized as 8 blocks each having 8192 rows. Each row has 4 column address locations. Address inputs A(1:0) define the column address to be accessed. An access can start on any column address, and other column locations may be accessed without the need to toggle the /CE pin. For fast access reads, once the first data byte is driven onto the bus, the column address inputs A(1:0) may be changed to a new value. A new data byte is then driven to the DQ pins no later than t_{AAP}, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While /CE is low, a subsequent write pulse along with a new column address provides a page mode write access.

Precharge Operation

The precharge operation is an internal condition in which the state of the memory is being prepared for a new access. Precharge is user-initiated by driving the /CE signal high. It must remain high for at least the minimum precharge time t_{PC}.

Software Write Protection

The 256Kx16 address space is divided into 8 sectors (blocks) of 32Kx16 each. Each sector can be individually software write-protected and the settings are nonvolatile. A unique address and command sequence invokes the write protection mode.

To modify write protection, the system host must issue six read commands, three write commands, and a final read command. The specific sequence of read addresses must be provided in order to access to the write protect mode. Following the read address sequence, the host must write a data byte that specifies the desired protection state of each sector. For confirmation, the system must then write the complement of the protection byte immediately following the protection byte. Any error that occurs including read addresses in the wrong order, issuing a seventh read address, or failing to complement the protection value will leave the write protection unchanged.

The write protect state machine monitors all addresses, taking no action until this particular read/write sequence occurs. During the address sequence, each read will occur as a valid operation and data from the corresponding addresses will be driven onto the data bus. Any address that occurs out of sequence will cause the software protection state machine to start over. After the address sequence is completed, the next operation must be a write cycle. The data byte contains the write-protect settings. This value will not be written to the memory array, so the address is a don't-care. Rather it will be held pending the next cycle, which must be a write of the data complement to the protection settings. If the complement is correct, the write protect settings will be adjusted. If not, the process is aborted and the address sequence starts over. The data value written after the correct six addresses will not be entered into memory.

The protection data byte consists of 8-bits, each associated with the write protect state of a sector. The data byte must be driven to the lower 8-bits of the data bus, DQ(7:0). Setting a bit to 1 write protects the corresponding sector; a 0 enables writes for that sector. The following table shows the write-protect sectors with the corresponding bit that controls the write-protect setting.

Write Protect Sectors – 32K x16 blocks

Sector 7	`3FFFFh – 38000h`
Sector 6	`37FFFh – 30000h`
Sector 5	`2FFFFh – 28000h`
Sector 4	`27FFFh – 20000h`
Sector 3	`1FFFFh – 18000h`
Sector 2	`17FFFh – 10000h`
Sector 1	`0FFFFh – 08000h`
Sector 0	`07FFFh – 00000h`

The write-protect read address sequence follows:

1. 24555h *
2. 3AAAAh
3. 02333h
4. 1CCCCh
5. 000FFh
6. 3EF00h
7. 3AAAAh
8. 1CCCCh
9. 0FF00h
10. 00000h

** If /CE is low entering the sequence, then an address of 00000h must precede 24555h.*

The address sequence provides a very secure way of modifying the protection. The write-protect sequence has a 1 in 3 x 10^{32} chance of randomly accessing exactly the 1st six addresses. The odds are further reduced by requiring three more write cycles, one that requires an exact inversion of the data byte. A flow chart of the entire write protect operation is shown in Figure 2. The write-protect settings are nonvolatile. The factory default: all blocks are unprotected.

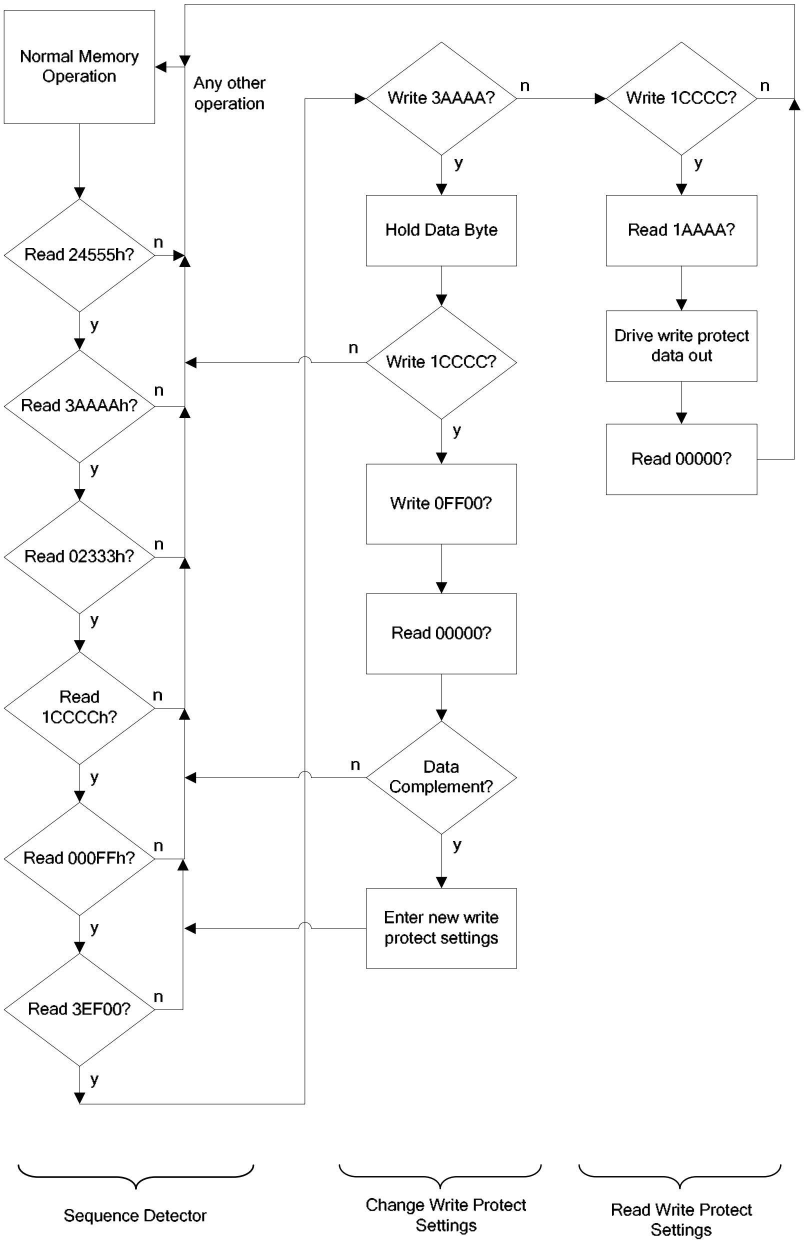
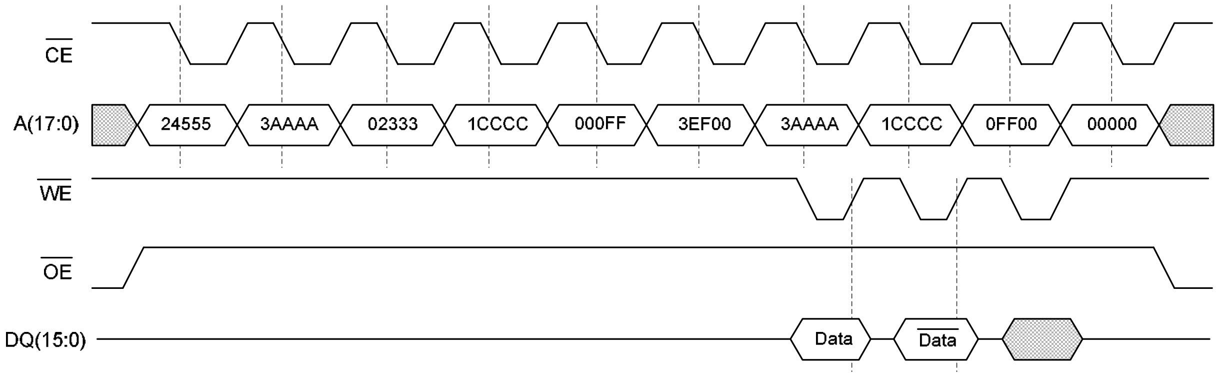


Figure 2. Write-Protect State Machine

For example, the following sequence write-protects addresses from `18000h` to `27FFFh` (sectors 3 & 4):

```
      Address  Data
Read   24555h    -
Read   3AAAAh    -
Read   02333h    -
Read   1CCCCh    -
Read   000FFh    -
Read   3EF00h    -
Write  3AAAAh   18h   ; bits 3 & 4 = 1
Write  1CCCCh   E7h   ; complement of 18h
Write  0FF00h    -    ; Data is don’t care
Read   00000h    -    ; return to Normal Operation
```

Software Write Protect Timing



SRAM Drop-In Replacement

The FM22LD16 has been designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require /CE to toggle for each new address. /CE may remain low indefinitely. While /CE is low, the device automatically detects address changes and a new access is begun. This functionality allows /CE to be grounded as you might with an SRAM. It also allows page mode operation at speeds up to 40MHz. **Note that if /CE is tied to ground, the user must be sure /WE is not low at powerup or powerdown events. If /CE and /WE are both low during power cycles, data corruption will occur. Figure 3 shows a pullup resistor on /WE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /WE pin tracks V_{DD} yet a high enough value that the current drawn when /WE is low is not an issue. A 10Kohm resistor draws 330uA when /WE is low and V_{DD}=3.3V.**

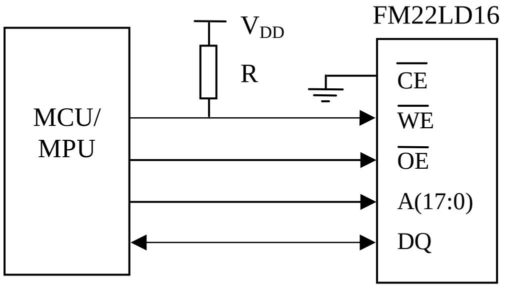


Figure 3. Use of Pullup Resistor on /WE

NOTE: If /CE is tied to ground, the user gives up the ability to perform the software write-protect sequence.

For applications that require the lowest power consumption, the /CE signal should be active only during memory accesses. The FM22LD16 draws supply current while /CE is low, even if addresses and control signals are static. While /CE is high, the device draws no more than the maximum standby current I_{SB}.

The FM22LD16 is backward compatible with the 1Mbit FM20L08 and 256Kbit FM18L08 devices. That is, operating the FM22LD16 with /CE toggling low on every address is perfectly acceptable.

The /UB and /LB byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 512Kx8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte enables or the next higher address line A(18) may be available from the system processor.

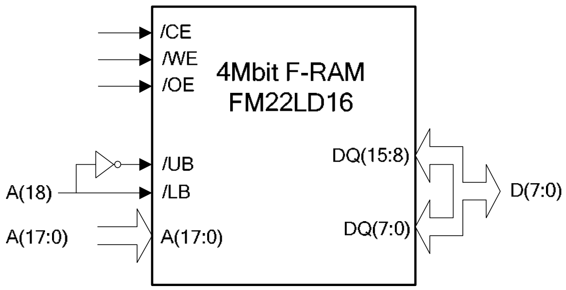


Figure 4. FM22LD16 Wired as 512Kx8

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}+1V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-D) - Charged Device Model (JEDEC Std JESD22-C101-C) - Machine Model (JEDEC Std JESD22-A115-A)	 2.5kV 1.5kV 150V
	Package Moisture Sensitivity Level	MSL-3

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.7	3.3	3.6	V	
I_{DD}	Power Supply Current		8	12	mA	1
I_{SB}	Standby Current @ T_A = 25°C @ T_A = 85°C		 90 -	 150 270	 µA µA	2
V_{TP}	V_{DD} Trip Point to Block Accesses	2.2	-	2.6	V	3
I_{LI}	Input Leakage Current			±1	µA	
I_{LO}	Output Leakage Current			±1	µA	
V_{IH}	Input High Voltage	2.2		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.6	V	
V_{OH1}	Output High Voltage (I_{OH} = -1.0 mA)	2.4			V	
V_{OH2}	Output High Voltage (I_{OH} = -100 µA)	V_{DD}-0.2			V	
V_{OL1}	Output Low Voltage (I_{OL} = 2.1 mA)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 100 µA)			0.2	V	

Notes

1. V_{DD} = 3.6V, /CE cycling at min. cycle time. All inputs toggling at CMOS levels (0.2V or V_{DD}-0.2V), all DQ pins unloaded.
2. V_{DD} = 3.6V, /CE at V_{DD}, All other pins are static and at CMOS levels (0.2V or V_{DD}-0.2V).
3. If $V_{DD} < V_{TP}$, all memory accesses are blocked regardless of input pin conditions.

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{RC}	Read Cycle Time	110	-	ns	
t_{CE}	Chip Enable Access Time	-	55	ns	
t_{AA}	Address Access Time	-	110	ns	
t_{OH}	Output Hold Time	20	-	ns	
t_{AAP}	Page Mode Address Access Time	-	25	ns	
t_{OHP}	Page Mode Output Hold Time	5	-	ns	
t_{CA}	Chip Enable Active Time	55	-	ns	
t_{PC}	Precharge Time	55	-	ns	
t_{BA}	/UB, /LB Access Time	-	20	ns	
t_{AS}	Address Setup Time (to /CE low)	0	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	55	-	ns	
t_{OE}	Output Enable Access Time	-	15	ns	
t_{HZ}	Chip Enable to Output High-Z	-	10	ns	1
t_{OHZ}	Output Enable High to Output High-Z	-	10	ns	1
t_{BHZ}	/UB, /LB High to Output High-Z	-	10	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{WC}	Write Cycle Time	110	-	ns	
t_{CA}	Chip Enable Active Time	55	-	ns	
t_{CW}	Chip Enable to Write Enable High	55	-	ns	
t_{PC}	Precharge Time	55	-	ns	
t_{BHZ}	/UB, /LB High to Output High-Z	5		ns	
t_{PWC}	Page Mode Write Enable Cycle Time	25	-	ns	
t_{WP}	Write Enable Pulse Width	16	-	ns	
t_{AS}	Address Setup Time (to /CE low)	0	-	ns	
t_{ASP}	Page Mode Address Setup Time (to /WE low)	8	-	ns	
t_{AHP}	Page Mode Address Hold Time (to /WE low)	15	-	ns	
t_{WLC}	Write Enable Low to /CE High	25	-	ns	
t_{WLA}	Write Enable Low to A(17:2) Change	25	-	ns	
t_{AWH}	A(17:2) Change to Write Enable High	110	-	ns	
t_{DS}	Data Input Setup Time	14	-	ns	
t_{DH}	Data Input Hold Time	0	-	ns	
t_{WZ}	Write Enable Low to Output High Z	-	10	ns	1
t_{WX}	Write Enable High to Output Driven	10	-	ns	1
t_{WS}	Write Enable to /CE Low Setup Time	0	-	ns	2
t_{WH}	Write Enable to /CE High Hold Time	0	-	ns	2

Notes

1. This parameter is characterized but not 100% tested.
2. The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. The parameters t_{WS} and t_{WH} are not tested.

Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	-	8	pF	
C_{IN}	Input Capacitance	-	6	pF	

Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 2.7V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	Power-Up to First Access Time (after V_{DD} min)	450	-	µs	
t_{PD}	Last Write (/WE high) to Power Down Time (prior to V_{TP})	0	-	µs	
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2

Notes

1 Slope measured at any point on V_{DD} waveform.

2 Ramtron cannot test or characterize all V_{DD} power ramp profiles. The behavior of the internal circuits is difficult to predict when V_{DD} is below the level of a transistor threshold voltage. Ramtron strongly recommends that V_{DD} power up faster than 100ms through the range of 0.4V to 1.0V.

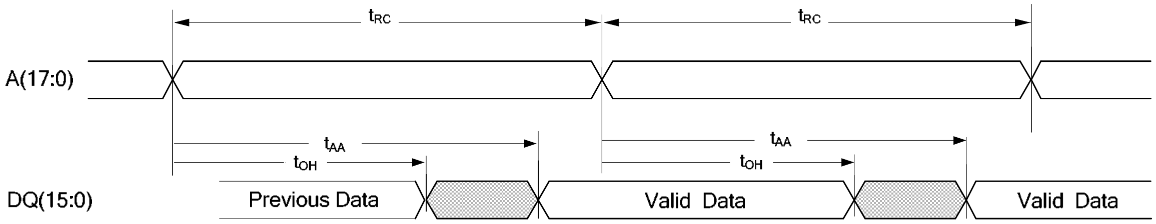
Data Retention (V_{DD} = 2.7V to 3.6V)

Parameter	Min	Units	Notes
Data Retention	10	Years	

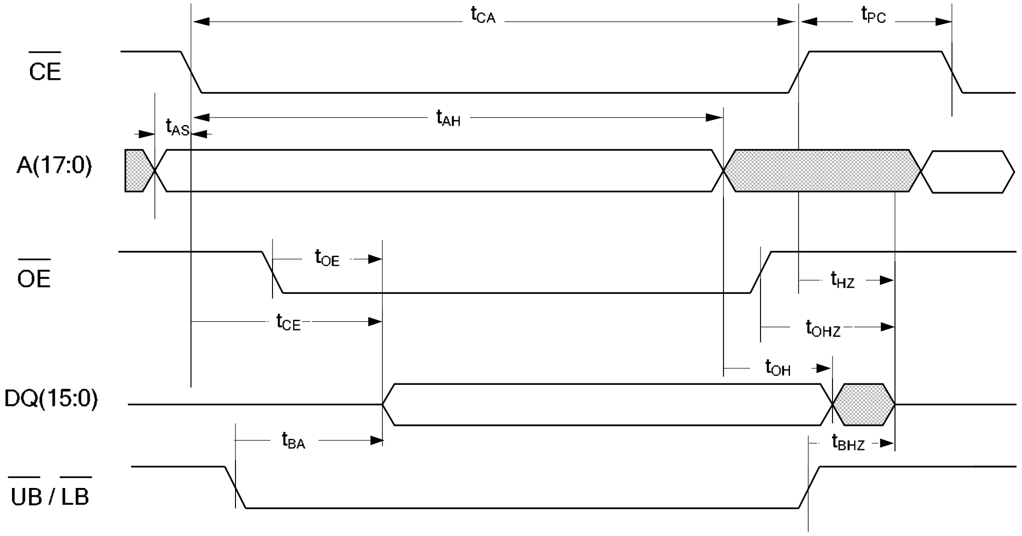
AC Test Conditions

Input Pulse Levels	0 to 3V	Input and Output Timing Levels	1.5V
Input Rise and Fall Times	3 ns	Output Load Capacitance	30pF

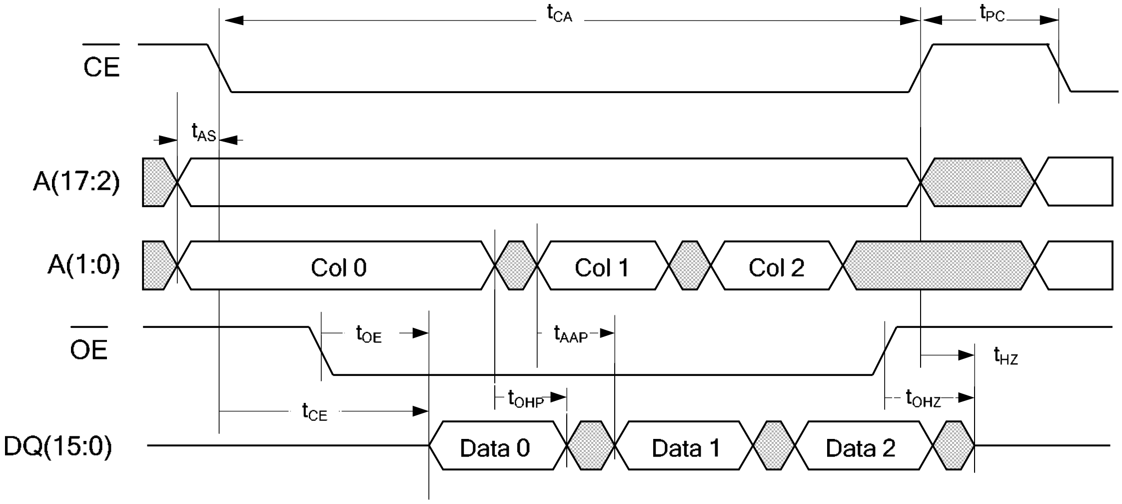
Read Cycle Timing 1 (/CE low, /OE low)



Read Cycle Timing 2 (/CE-controlled)

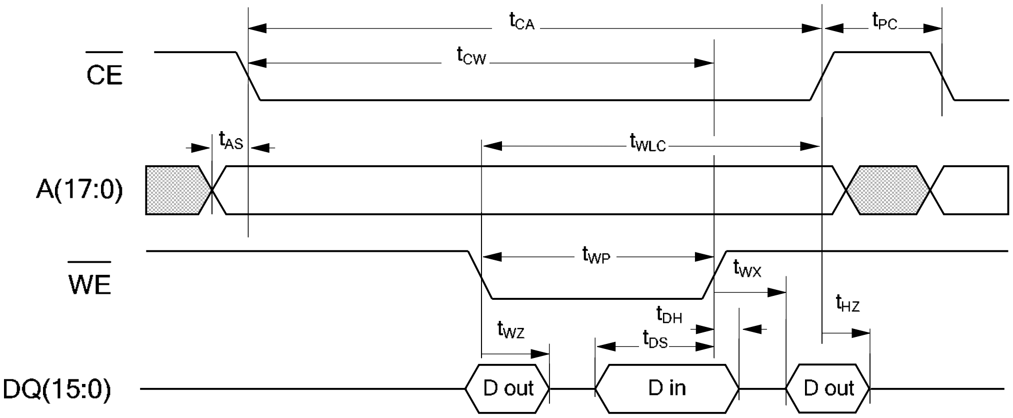


Page Mode Read Cycle Timing

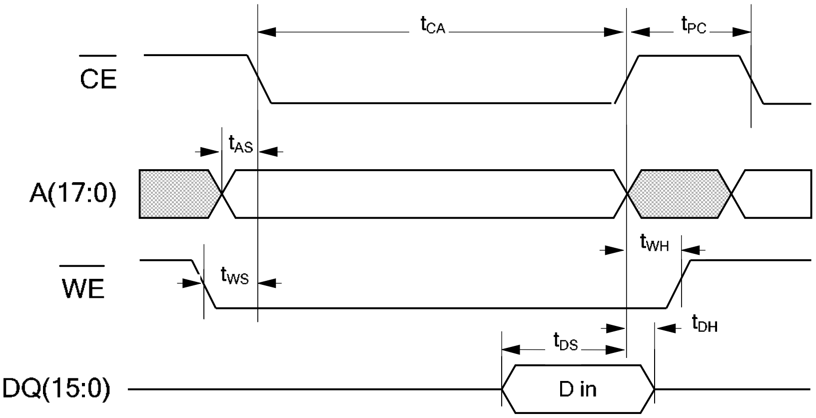


1. Although sequential column addressing is shown, it is not required.

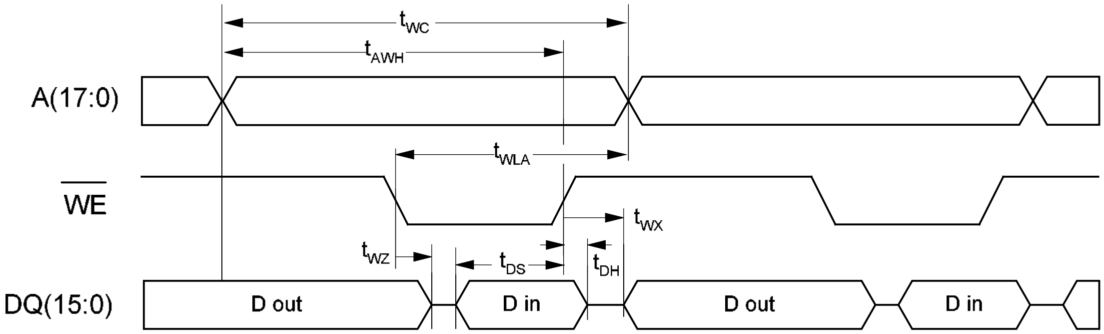
Write Cycle Timing 1 (/WE-Controlled, /OE low)



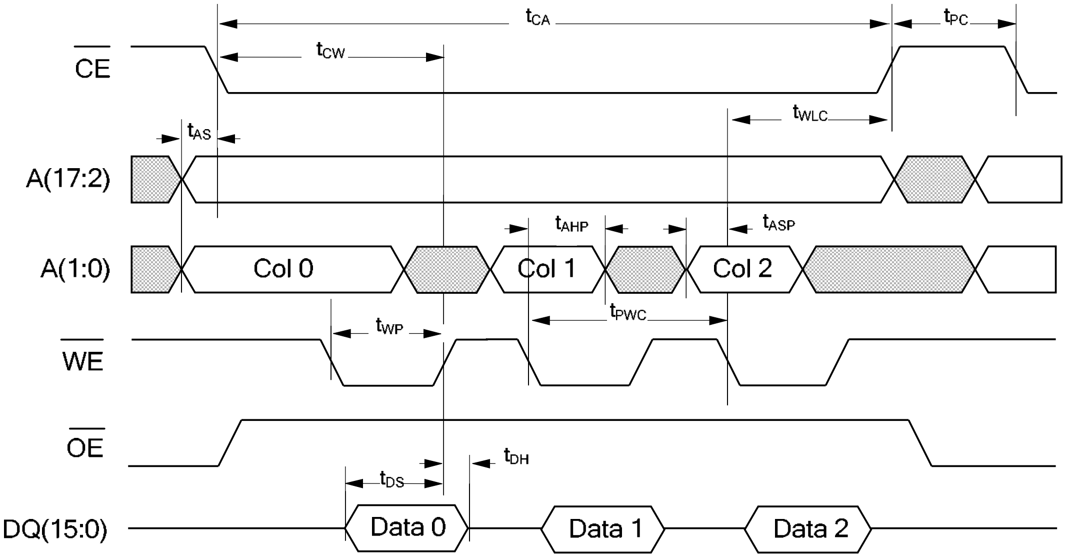
Write Cycle Timing 2 (/CE-Controlled)



Write Cycle Timing 3 (/CE low)



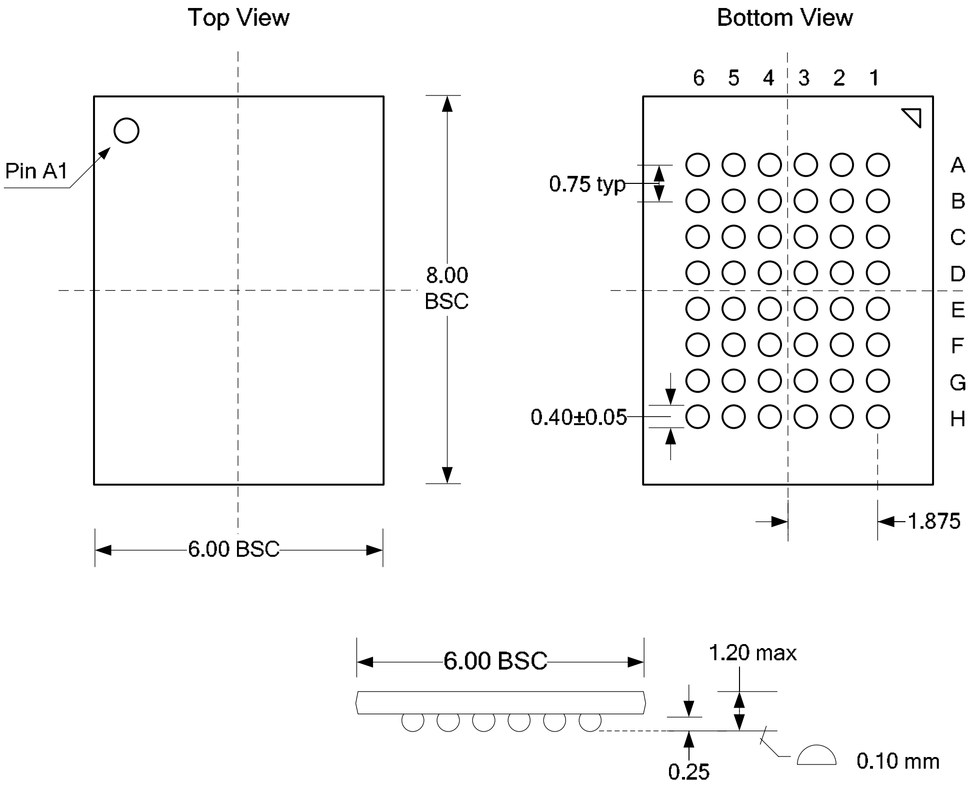
Page Mode Write Cycle Timing



1. Although sequential column addressing is shown, it is not required.

Mechanical Drawing

48-ball FBGA (0.75mm ball pitch)



Note: All dimensions in millimeters.

48 FBGA Package Marking Scheme

RAMTRON
XXXXXXX-S-P
LLLLLLL
YYWW
○

Legend:
XXXXXX= part number, S=speed, P=package
LLLLLL= lot code, YY=year, WW=work week

Examples: FM22LD16, "Green"/RoHS FBGA package,
Lot C8556953BG1, Year 2008, Work Week 44

RAMTRON
FM22LD16-55-BG
C8556953BG1
0844

Revision History

Revision	Date	Summary
1.0	10/2/2008	Initial release.