CS3511

Stereo 10 W High-efficiency Class-D Audio Power Amplifier

Features

- Closed-loop Advanced ΔΣ Architecture
- True Spread Spectrum Modulation
- Premium Quality Audio Amplification
  - 99 dB Dynamic Range - System Level
  - 0.025% THD+N @ 5 W - System Level
  - -96 dB Channel Separation
- Four Selectable Amplifier Gain Settings
- Integrated Protection and Automatic Recovery for Over-current, Under-voltage, and Thermal Overload
- Single-supply Operation (Typ. = 9-12 V)
- No Bootstrap Capacitors Required
- Low-power Standby Mode
- Supports Differential or Single-ended Inputs
- Thermally Enhanced 32-pin, 6 x 6 mm QFN Package Requires No External Heat Sink

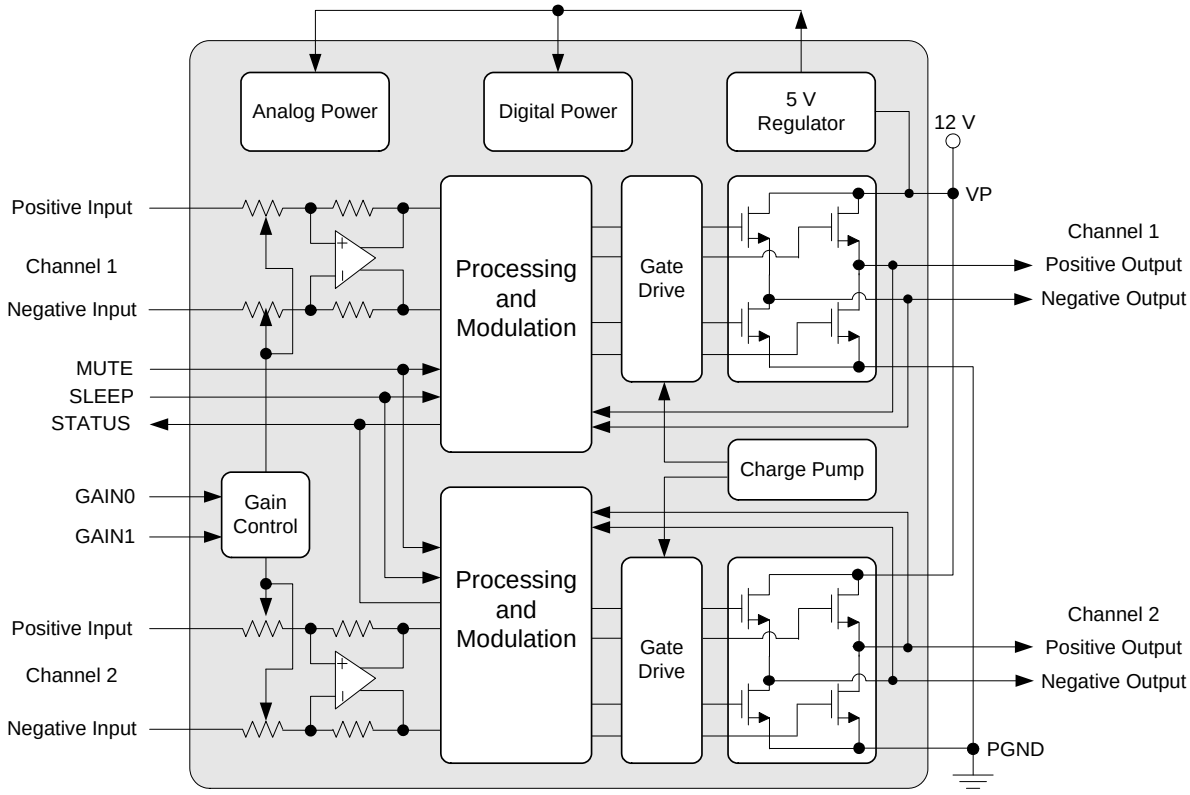
Common Applications

- Active Speakers
- Portable Media Player Docking Stations
- Mini/Micro Shelf Systems
- Digital Televisions

General Description

The CS3511 is a high-efficiency class-D PWM amplifier that integrates on-chip over-current, under-voltage, over-temperature protection, and error reporting. An on-board regulator generates a 5 VDC supply used to power the internal low-voltage analog and digital circuitry. The low $R_{DS(ON)}$ outputs can source peak currents up to 2.7 A, deliver high efficiency, allow a small device package, and lower power supply voltage levels.

The CS3511 is available in a 32-pin QFN package in Commercial grade (-10°C to +70°C). The CRD3511 customer reference design is also available. Please refer to "Ordering Information" on page 24 for complete ordering information.



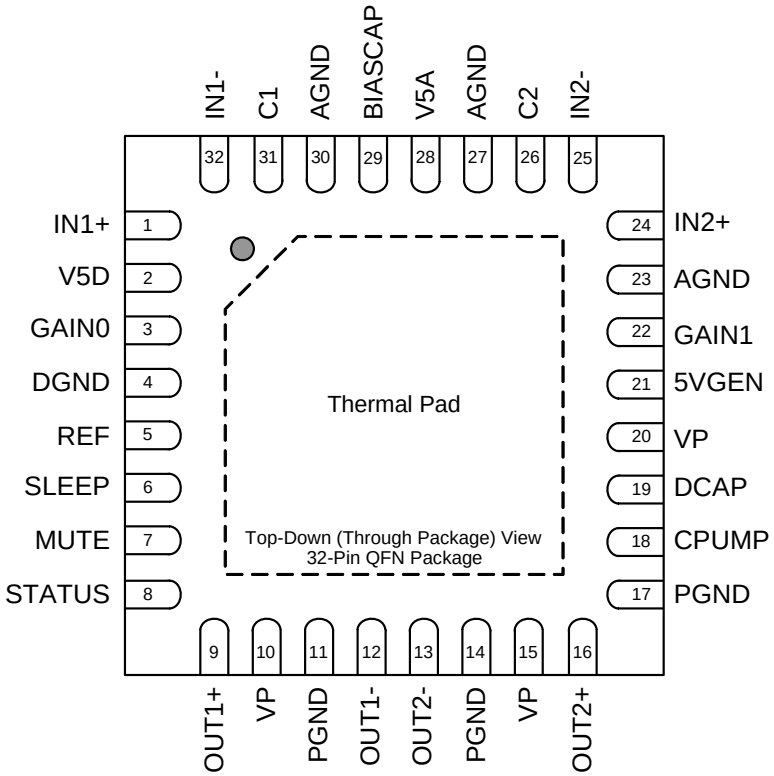
Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
IN1+ IN1- IN2+ IN2-	1 32 24 25	**Differential Analog Input** (*Input*) - Differential Audio Signal Inputs for channel 1 and channel 2.
V5D	2	**Digital Power** (*Input*) - Supply for digital logic. Connect to 5VGEN.
GAIN0 GAIN1	3 22	**Gain** (*Input*) - Gain select bits. GAIN0 is the least significant bit.
DGND	4	**Digital Ground** (*Input*) - Ground reference for the internal logic and digital I/O.
REF	5	**Reference** (*Output*) - Internal reference voltage.
SLEEP	6	**Sleep** (*Input*) - When set to logic high, device enters low power mode. If not used, this pin should be grounded.
MUTE	7	**Mute** (*Input*) - When set to logic high, both amplifiers are muted and in Idle Mode. When low (grounded), both amplifiers are fully operational. If not used, this pin should be grounded.
STATUS	8	**Status** (*Output*) - A logic high output indicates over-current or under-voltage condition, thermal overload, that an output is shorted to ground or to another output, that the device is in low power mode (the SLEEP pin is high), or that the device is in reset. A logic low state indicates that the CS3511 is ready to output audio.

OUT1+ OUT1- OUT2+ OUT2-	9 12 16 13	**Differential PWM Output** (*Output*) - Differential PWM Outputs for channel 1 and channel 2.
VP	10 15 20	**High Voltage Power** (*Input*) - Supply pins for high current H-bridges.
PGND	11 14 17	**Power Ground** (*Input*) - High current ground for analog outputs.
CPUMP	18	**Charge Pump Input** (*Input*) - Input pin for charge pump.
DCAP	19	**Charge Pump Switching Pin** (*Output*) - Free-running 350 kHz square wave between VP and ground.
5VGEN	21	**5 Volt Generator** (*Output*) - Regulated 5 VDC source used to supply power to the input section (pins 2 and 28).
AGND	23 27 30	**Analog Ground** (*Input*) - Connect all pins together directly at the thermal pad of the CS3511.
IN2+ IN2-	24 25	**Negative Analog Input** (*Input*) - Negative Audio Signal for channel 2 and channel 1, respectively.
C2 C1	26 31	**Pop Minimization Capacitor** (*Input*) - External capacitor used to reduce turn on/off pops.
V5A	28	**Analog Power** (*Input*) - Supply for analog circuitry. Connect to 5VGEN.
BIASCAP	29	**Analog Input Bias** (*Input*) - Input stage bias voltage.
Thermal Pad	-	**Thermal Pad** *(Input)* - Thermal relief pad for optimized heat dissipation. Connect to PGND. See "QFN Thermal Pad" on page 16 for more information.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DGND = PGND = 0 V; All voltages with respect to ground. (Note 1)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Supply Voltage	VP	8.5	12	13.2	V
Temperature					
Ambient Temperature	T_A	-10	-	+70	°C
Junction Temperature	T_J	-10	-	+150	°C

Notes:

1. Device functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = PGND = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Outputs Switching and Under Load	(Note 2)	VP	-	13.2	V
No Output Switching		VP	-0.3	14.0	
Inputs					
Input Current	(Note 3)	I_{in}	-	±10	mA
Digital Input Voltage	(Note 4)	V_{IND}	-0.3	V5D + 0.3	V
Temperature					
Ambient Operating Temperature (power applied)		T_A	-20	+85	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Notes:

2. The outputs will stop switching at the VP Under-Voltage Error Falling Trigger Point. See "DC Electrical Characteristics" on page 8.
3. Any pin except supplies. Transient currents of up to ±100 mA on the INxx pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

AC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; T_A = 25°C; VP = 12 V; R_L = 8 Ω full-bridge; GAIN1 = 0, GAIN0 = 1; 10 Hz to 20 kHz Measurement Bandwidth; Performance measurements taken with a differential 997 Hz sine wave and AES17 measurement filter; Stereo Full-Bridge measurements taken through the Full-Bridge Output Filter shown in Figure 4 on page 15.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average/Channel) (Note 5)	P_O	THD+N = 1% R_L = 8 Ω	-	7.5	-	W
		R_L = 6 Ω	-	9.1	-	W
		THD+N = 7% R_L = 8 Ω	-	8.8	-	W
		R_L = 6 Ω	-	10.8	-	W
		THD+N = 10% R_L = 8 Ω	-	9.4	-	W
		R_L = 6 Ω	-	11.4	-	W
Total Harmonic Distortion + Noise (Note 5)	THD+N	P_O = 1 W, R_L = 8 Ω	-	0.019	-	%
		P_O = 5 W, R_L = 8 Ω	-	0.025	-	%
Dynamic Range (Note 6)	DYR	V_{in} = -60 dBi				
		A-Weighted	-	99	-	dB
		Unweighted	-	96	-	dB
Signal to Noise Ratio (Note 6)	SNR	Inputs AC coupled to AGND				
		A-Weighted	-	99	-	dB
		Unweighted	-	96	-	dB
Power Supply Rejection Ratio	PSRR	200 mv p-p from 20 Hz ≤ f ≤ 1 kHz, inputs AC coupled to AGND	-	55	-	dB
IHF Intermodulation Distortion	IHF-IMD	19 kHz, 20 kHz, 1:1 (IHF), P_O = 1 W	-	0.20	-	%
Channel Separation	CS	P_O=1 W, f = 1 kHz	-	104	-	dB
		20 Hz ≤ f ≤ 20 kHz	-	78	-	dB
Output Offset Voltage (Note 7)	V_{OFFSET}	MUTE = low	-	50	-	mV
Efficiency	η	P_O = 2 x 9.4 W, R_L = 8 Ω	-	85	-	%
PWM Output Over-Current Error Trigger Point	I_{CE}		-	2.7	-	A
Junction Thermal Error Rising Trigger Point	T_{TERISE}		-	155	-	°C
Junction Thermal Error Falling Trigger Point	T_{TEFALL}		-	135	-	°C
Turn On Time	t_{on}	SLEEP = V_{IL}	-	155	-	ms
Turn Off Time	t_{off}	SLEEP = V_{IH}	-	3	-	ms
Amplifier Gain		Gain1 = 0, Gain0 = 0	-	13.6	-	dB
		Gain1 = 0, Gain0 = 1	-	19.5	-	dB
		Gain1 = 1, Gain0 = 0	-	23.8	-	dB
		Gain1 = 1, Gain0 = 1	-	27.3	-	dB
Gain Matching		Between output channels	-	0.1	-	%
Input Impedance		Gain1 = 0, Gain0 = 0	36.8	46.0	55.2	kΩ
		Gain1 = 0, Gain0 = 1	18.4	23.0	27.6	kΩ
		Gain1 = 1, Gain0 = 0	11.0	13.8	16.6	kΩ
		Gain1 = 1, Gain0 = 1	7.3	9.2	11.1	kΩ

Notes:

5. See Figure 5 on page 17.
6. dBi is referenced to the input signal amplitude resulting in the specified output power at THD+N<1%. See "Parameter Definitions" on page 21 for more information.
7. See Section 4.2 "Dynamic DC Offset Calibration" on page 12.

DC ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise specified): AGND = DGND = PGND = 0 V; All voltages with respect to ground; T_A = 25°C; VP = 12 V; R_L = 8 Ω full-bridge; GAIN1 = 0, GAIN0 = 1; Stereo Full-Bridge measurements taken through the Full-Bridge Output Filter shown in Figure 4 on page 15.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Sleep Supply Current	$I_{CC(sleep)}$	SLEEP = V_{IH}	-	5.2	-	mA
		SLEEP = V_{IH}; no load, filter, or snubber	-	5.2	-	mA
Mute Supply Current	$I_{CC(mute)}$	MUTE = V_{IH}	-	38	-	mA
		MUTE = V_{IH}; no load, filter, or snubber	-	38	-	mA
Quiescent Current	I_{CC}	V_{IN} = 0 V; SLEEP = V_{IL}, MUTE = V_{IL}	-	68	-	mA
		V_{IN} = 0 V; SLEEP = V_{IL}, MUTE = V_{IL}; no load, filter, or snubber	-	85	-	mA
MOSFET On Resistance (each FET)	$R_{DS(ON)}$	I_d = 0.5 A, T_J = 50°C	-	325	-	mΩ
5VGEN Nominal Voltage			-	5.2	-	V
5VGEN DC current source			-	-	70	mA
REF Nominal Voltage			-	1.2	-	V
BIASCAP Nominal Voltage			-	2.5	-	V
VP Under-Voltage Error Falling Trigger Point	$V_{UVVPFALL}$		-	7.56	-	V
VP Under-Voltage Error Rising Trigger Point	$V_{UVVPRISE}$		-	8.08	-	V
V5A Under-Voltage Error Falling Trigger Point	$V_{UV5VFALL}$		-	4.1	-	V
V5A Under-Voltage Error Rising Trigger Point	$V_{UV5VRISE}$		-	4.3	-	V
Charge Pump Under-Voltage Error Falling Trigger Point	$V_{UVCPFALL}$		-	1.55*VP	-	
Charge Pump Under-Voltage Error Rising Trigger Point	$V_{UVCPRISE}$		-	1.62*VP	-	

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

Parameters		Symbol	Min	Max	Units
High-Level Input Voltage (MUTE, SLEEP)	(Note 8)	V_{IH}	V5D - 2	-	V
High-Level Input Voltage (GAIN1, GAIN0)		V_{IH}	V5D - 0.8	-	V
Low-Level Input Voltage (MUTE, SLEEP, GAIN1, GAIN0)	(Note 8)	V_{IL}	-	1	V
Transition Time Between V_{IH} and V_{IL} (MUTE, SLEEP)	(Note 8)	t_I	-	500	ns
High-Level Output Voltage (STATUS)	I_O = 250 µA	V_{OH}	V5D - 0.5	-	V
Low-Level Output Voltage (STATUS)	I_O = 250 µA	V_{OL}	-	0.5	V
Input Leakage Current (MUTE, SLEEP)		I_{in}	-	±10	µA
Input Leakage Current (GAIN1, GAIN0)		I_{in}	-	±300	µA

Notes:

8. Levels between V_{IH} and V_{IL} are invalid. The transition period between VIH and VIL should not exceed t_I.

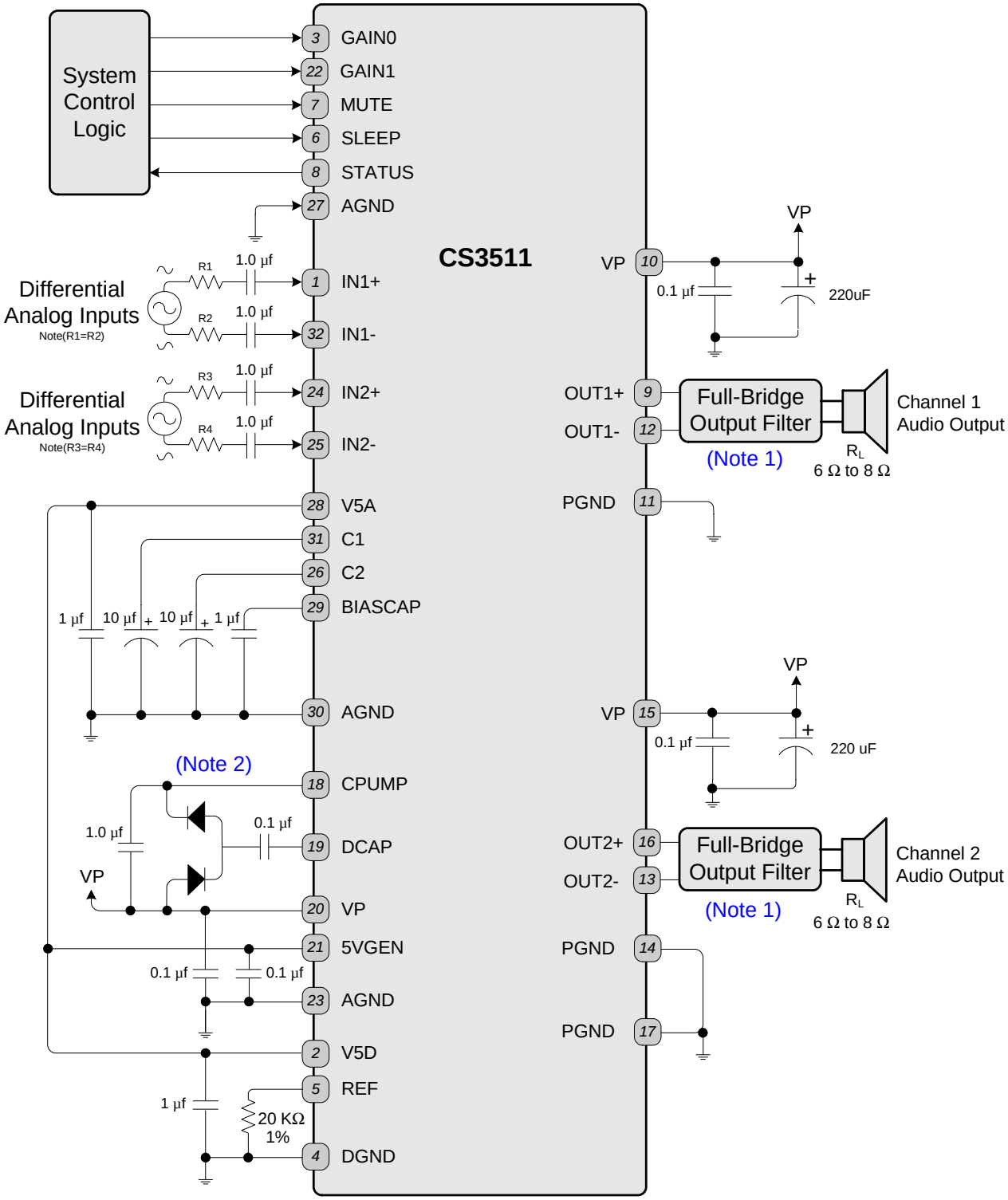
DIGITAL I/O PIN CHARACTERISTICS

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

Power Supply	Pin Number	Pin Name	I/O	Driver	Receiver
5VD	3	GAIN0	Input	-	5.0 V; Internal 50 kΩ pull-down
	22	GAIN1	Input	-	5.0 V; Internal 50 kΩ pull-down
	7	MUTE	Input	-	5.0 V
	6	SLEEP	Input	-	5.0 V
	8	STATUS	Output	5.0 V	-
VP	35	OUT1+	Output	8.5 V - 13.2 V Power MOSFET	-
	32	OUT1-	Output	8.5 V - 13.2 V Power MOSFET	-
	29	OUT2+	Output	8.5 V - 13.2 V Power MOSFET	-
	26	OUT2-	Output	8.5 V - 13.2 V Power MOSFET	-

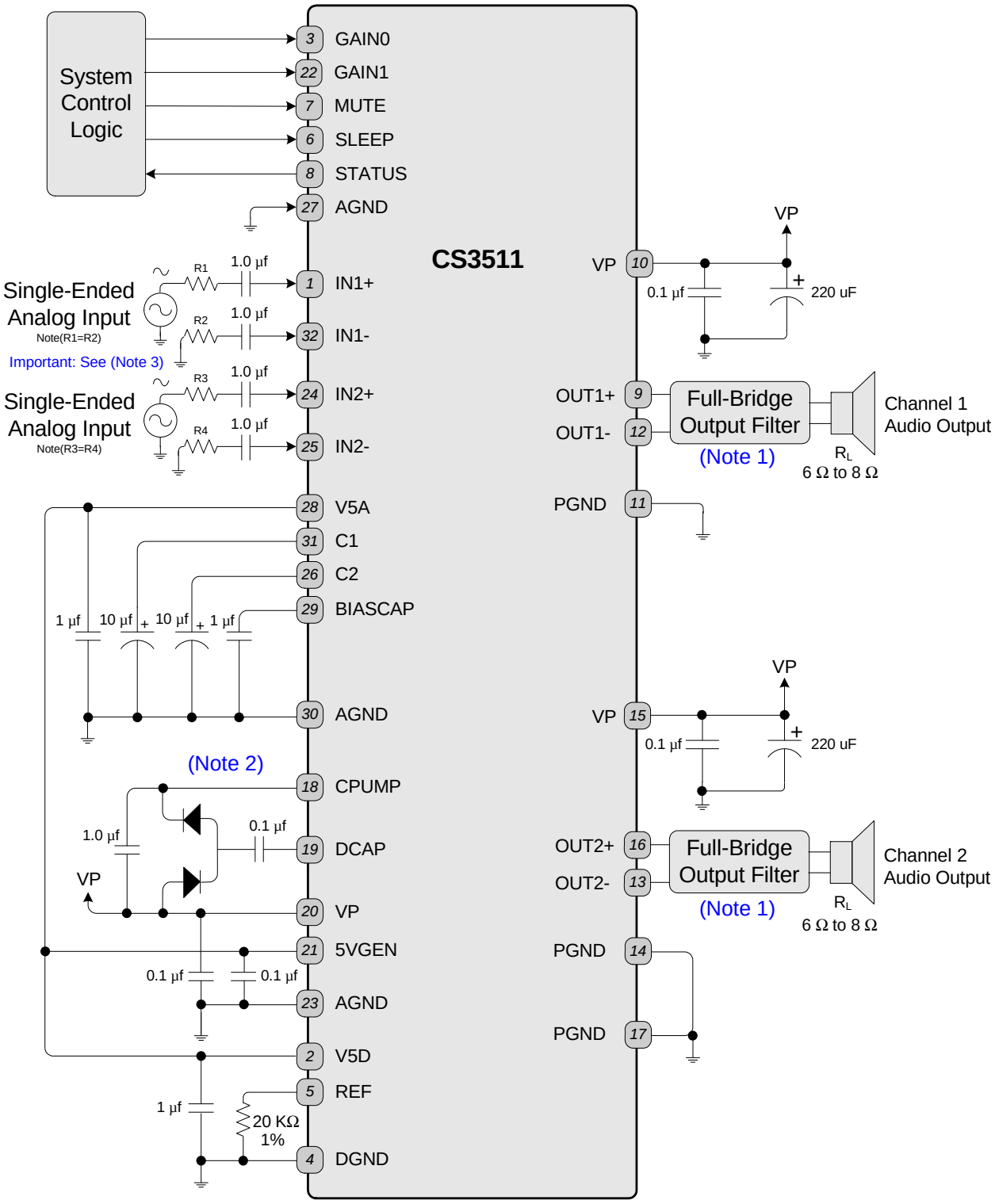
Table 1. I/O Power Rails

3. TYPICAL CONNECTION DIAGRAMS



1. See Section 4.11 for typical full-bridge output filter.
2. Incorrectly connecting the external charge pump circuitry can result in permanent damage to the device.

Figure 1. Typical Connection Diagram - Stereo Amplifier with Differential Inputs



1. See Section 4.11 for typical full-bridge output filter.
2. Incorrectly connecting the external charge pump circuitry can result in permanent damage to the device.
3. See Section 4.1 for important information regarding using Single-Ended inputs with the CS3511.

Figure 2. Typical Connection Diagram - Stereo Amplifier with Single-Ended Inputs

4. APPLICATIONS

4.1 CS3511 Input Stage

The input stage of the CS3511 is configured as a differential receiver to maximize common-mode rejection in typical audio circuits. To maximize this benefit, the INx+ and INx- pins should be driven with differential signals from sources that have the same output impedance. Also, the signals should be routed parallel to one another from their source to the analog inputs of the CS3511.

In some instances, there will be a necessity to drive the CS3511 with a single-ended input signal. In this case, the unused input should be AC coupled to ground using the same value of C_I implemented for the driven channel. Either input, INx+ or INx-, can be used for the signal input. To minimize the effects of ground noise in the system, C_I should be terminated at the ground connection through a resistor, R_I. Please refer to Figure 3. The value of the resistor should match the output impedance of the audio source.

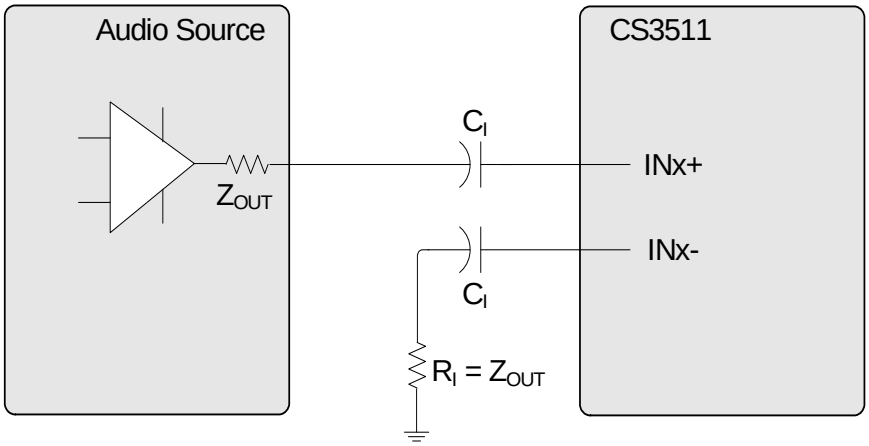


Figure 3. CS3511 Input Stage

4.2 Dynamic DC Offset Calibration

Abrupt changes in DC output offset level are a known cause of audible turn-on and turn-off pops. Typically, when a system turns on (begins switching), the potential across the speaker changes abruptly from 0 V to the steady-state DC offset voltage of the system. Similarly, when the system turns off, the potential changes abruptly from the steady-state DC offset voltage to 0 V. These abrupt changes are heard as a pop.

The CS3511 employs a patented method for reducing this pop. Immediately before the outputs begin to switch, a calibration circuit dynamically minimizes the amplifier's internal offsets. With these offsets at a minimum, the outputs begin to switch and the CS3511 begins to slowly ramp the DC output offset potential to the steady-state DC offset voltage. This ramp is slow enough to keep the speaker movement in the subsonic range. During turn-off, this procedure is reversed. The static DC offset voltage is ramped down to a dynamically minimized DC offset level before output switching is stopped.

Dynamic offset cancellation requires equal impedances on the positive and negative inputs. If a single-ended audio source with a 600 Ω output impedance is connected to the IN1+ (through a DC blocking capacitor), IN1- must be terminated to ground with a 600 Ω resistor (also through a DC blocking capacitor. (See Figure 3).

4.3 CS3511 Amplifier Gain

The closed-loop gain of the CS3511 is externally configured via two input pins, GAIN0 and GAIN1. The "AC Electrical Characteristics" on page 7 shows the four different gain values available based on the pin voltages at GAIN0 and GAIN1. The GAIN0 and GAIN1 input pins have weak internal pull-down resistors; so they should be driven high when set to a logic high. Internally, different input resistor values are used to implement the four gain settings. Thus, the input impedance will change based on the gain setting. The gain tracking is very tightly matched within each device, but the absolute input impedance will vary due to process variations. This variation must be considered when choosing the proper value of C_I. The low-frequency roll-off characteristic is dedicated by the choice of C_I and R_I.

The -3 dB frequency is:

$$f_{c\ -\ 3\ dB} = \frac{1}{2\ \pi\ C_I\ R_I}$$

On the CRD3511, a value of 1.0 µF is used for C_I; this value provides a nearly flat response down to 20 Hz, even for the highest gain setting. In many cases, a lower value of C_I can be used due to a lower gain setting or because the speakers used do not have the ability to reproduce low-frequency signals.

4.4 MUTE Pin

The MUTE pin must be driven to a logic low or logic high state for proper operation. To enable the amplifier, connect the MUTE pin to a logic low. To enable the mute function, connect the MUTE pin to a logic high signal.

When in mute, the internal processor bias voltages remain active in the CS3511. This state maintains the bias on the input coupling capacitor to prevent audible transients which would be caused by the charging and discharging of this capacitor. It is recommended that the MUTE pin be held high during power-up or power-down to eliminate audible transients.

If power-up and/or power-down pops are present with a CS3511 amplifier, the cause may be other circuitry external to the CS3511, such as an audio processor or preamp. If the CS3511 is in the active state (MUTE pin is low), these audible pops will be amplified and output to the speakers. To eliminate this problem, activate the MUTE pin before the power supply collapses during a power-down sequence.

4.5 SLEEP Pin

When pulled high, the SLEEP pin puts the device into a low quiescent current mode. To disable sleep mode, the SLEEP pin should be grounded. While the device is in low power mode the STATUS pin will be in a logic high state to indicate that the device is not ready to produce audio.

4.6 Power Up and Power Down Sequence

To minimize power-on and power-off transients, the device should be held in the MUTE state while powering up or powering down the CS3511. The SLEEP pin can be held in either the logic high state or logic low state during power-up or power-down.

4.6.1 Recommended Power-Up Sequence

1. Apply power to the system.
2. Hold the MUTE pin in the logic high state until the power supply is stable. In this state, all associated outputs are held in a high-impedance state.
3. Set the MUTE pin to a logic low state to begin normal operation. If the SLEEP pin is held high during power-on (optional), it should be set low before the MUTE pin is set low.

4.6.2 Recommended Power-Down Sequence

1. Set the MUTE pin to the logic high state. This will mute the amplifier outputs and hold them in a high-impedance state.
2. Optionally, the SLEEP pin can now be set to a logic high state to place the device into low power mode.
3. The power supplies can now be removed.

4.7 Protection Circuits

The CS3511 is protected against under-voltage, over-current, and over-temperature conditions. If one of these fault conditions are present the amplifier will be muted, the outputs will be tri-stated, and the STATUS pin will remain in a logic high state until the condition clears. The amplifier will automatically attempt to re-cover from a detected fault condition.

4.7.1 Under-Voltage Protection

An under-voltage fault occurs if the voltage sensed on the VP terminals, the charge pump, or on V5A drops below the corresponding falling trigger point seen in the DC Electrical Characteristics table. The under-voltage fault will automatically clear once the voltage exceeds the associated rising trigger point. V5GEN, V5A, and V5D must be connected together in order to properly monitor V5D and V5GEN. (See Figure 1 and Figure 2).

4.7.2 Over-Temperature Protection

An over-temperature fault occurs if the junction temperature of the device exceeds the rising junction thermal error trigger point seen in the AC Electrical Characteristics table. The thermal hysteresis of the device will cause the fault to automatically clear when the junction temperature drops below the falling junction thermal error trigger point.

4.7.3 Over-Current Protection

An over-current fault occurs if more current than the over-current error trigger point flows from any of the amplifier output pins, see AC Electrical Characteristics. Over current can occur if the speaker wires are shorted together, if one side of the speaker is shorted to ground, or if the speaker impedance is too low.

WARNING: The outputs of the CS3511 should never be shorted to VP. Doing so can result in permanent damage to the device.

4.8 Integrated 5 V Regulator

The CS3511 includes an internal 5 V regulator in order to provide a supply to the internal digital and analog circuitry. The output of the regulator is present on the 5VGEN pin. The regulator output pin should have a bypass capacitor connected to AGND and be connected to the digital and analog supply pins as shown in the Typical Connection Diagrams in Section 3. The regulator output can be used to set the SLEEP, MUTE, GAIN0, and GAIN1 pins to a logic high state. The regulator is able to source the maximum current shown in the DC Electrical Characteristics table.

4.9 Power Dissipation De-Rating

As a result of high-efficiency and good package thermal characteristics, the CS3511 can operate at elevated ambient temperatures without having to de-rate the output power, assuming 8 Ω output loads or higher. ***The exposed pad must be soldered to the PC Board*** to increase the maximum power dissipation capability of the CS3511 package. Soldering will minimize the likelihood of an over-temperature fault occurring during

continuous heavy load conditions. There should be vias for connecting the exposed pad to the copper area on the printed circuit board. The pad must be electrically connected to PGND. See Section 5.2 for more information on the thermal pad and Section 9.1 for more information on thermal dissipation for the CS3511.

4.10 Performance Measurements of the CS3511

The CS3511 operates by generating a high-frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the CS3511 amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 100 kHz and 1.0 MHz, which is well above the 10 Hz – 20 kHz audio band. The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components outside of the audio band.

The measurements of certain performance parameters, particularly noise-related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible components introduced by the CS3511 amplifier's switching pattern will degrade the measurement result.

One feature of the CS3511 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. The CRD3511 Evaluation Board uses the filter described in Section 4.11, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

4.11 Full-Bridge Output Filter

Figure 4 shows the output filter for a full-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a resistor (5.6 Ω) and capacitor (680 pF) and should be placed as close as possible to the corresponding PWM output pins to greatly reduce radiated EMI. The inductors, L1 and L2, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 2 shows the component values based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

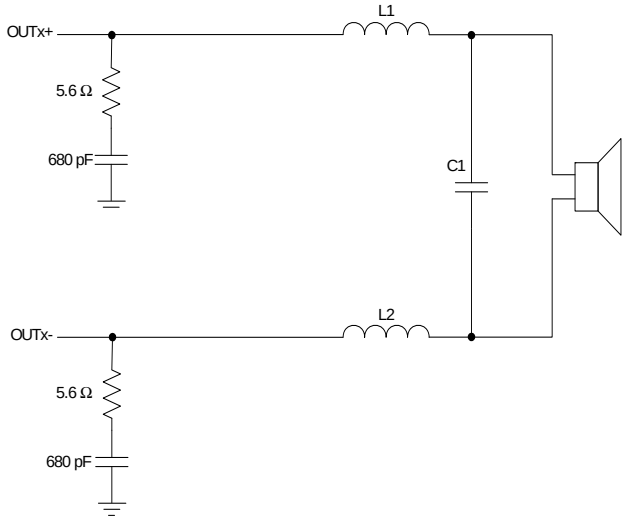


Figure 4. Output Filter

Load	L1, L2	C1
8 Ω	22 µH	0.47 µF
6 Ω	15 µH	0.47 µF

Table 2. Low-Pass Filter Components

5. POWER SUPPLY, GROUNDING, AND PCB LAYOUT

5.1 Power Supply and Grounding

The CS3511 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. It is necessary to de-couple the power supply by placing capacitors directly between the power and ground of the CS3511. Decoupling capacitors should be as close to the pins of the CS3511 as possible. The lowest value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS3511 to minimize inductance effects. The CRD3511 reference design demonstrates the optimum layout and power supply arrangements.

5.1.1 Maximum Supply Voltage

The absolute maximum allowable voltage on the VP supply pins (pins 10, 15 and 20) is shown in the Absolute Maximum Ratings table. Device damage can occur above this voltage. Please note that the absolute maximum voltage does not represent a valid operating condition. The maximum voltage on the VP pins during operation is shown in the Recommended Operating Conditions table.

During normal operation, the output pins (pins 9, 12, 13, and 16) may experience overshoot voltages due to inductive kickback. Care should be taken to properly de-couple the VP pins because overshoot on the output pins can travel through the CS3511 output devices and appear on the VP pins. Without proper power supply decoupling, this can cause ripple voltages on the VP pins that might exceed their absolute maximum voltage shown in the Absolute Maximum Ratings table. However, this will only happen in extreme cases and can be prevented by placing the high-frequency decoupling capacitors close to the VP pins.

5.2 QFN Thermal Pad

The CS3511 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to PGND. A series of thermal vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers; the copper in these ground planes will act as a heat sink for the CS3511. The CRD3511 reference design demonstrates the optimum thermal pad and via configuration.

5.3 Layout Considerations

The CS3511 is a power (high current) amplifier that operates at relatively high switching frequencies. The outputs of the amplifier switch between the supply voltage and ground, at high speeds, while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. Additionally, the CS3511's junction temperature rises when supplying power to loads and relies on the PCB for heat sinking.

To avoid subjecting the CS3511 to potentially damaging voltage stress and output-power-limiting elevated junction temperatures, it is critical to have a good printed circuit board layout. It is strongly recommended that the Cirrus CRD3511 layout be used for all applications and only be deviated from after careful analysis of the effects of any changes. Please refer to Cirrus Logic application note AN315 for further information regarding the layout of the CS3511.

6. TYPICAL AUDIO PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): All plots were taken using the CRD3511 Reference Design Board sourced with a differential input; T_A = 25°C; 10 Hz to 20 kHz Measurement Bandwidth; Performance measurements taken with a 997 Hz sine wave and AES17 measurement filter; GAIN1 = 0, GAIN0 = 1; VP = 12 VDC.

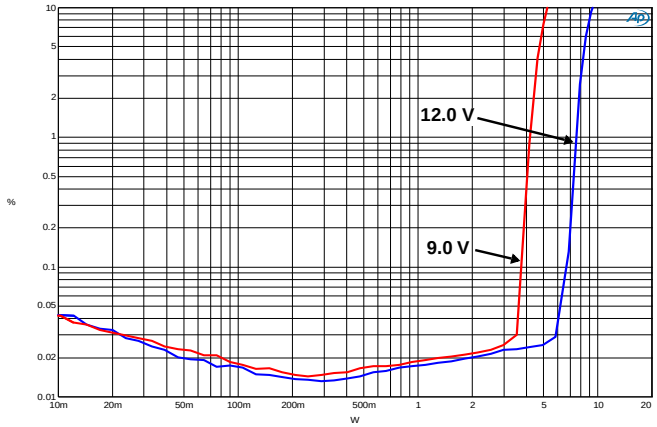


Figure 5. THD+N vs. Output Power (R_L= 8 Ω)

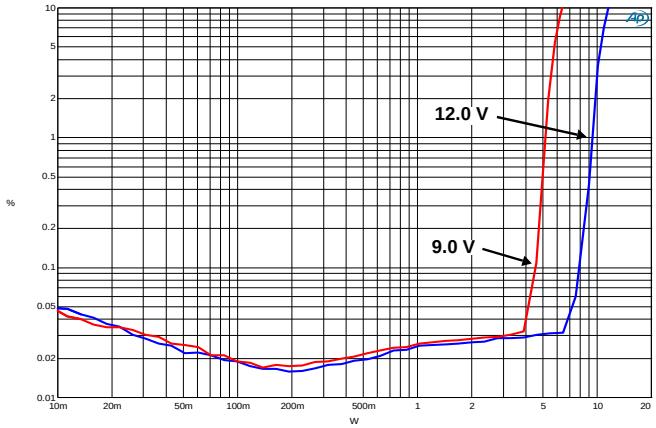


Figure 6. THD+N vs. Output Power (R_L= 6 Ω)

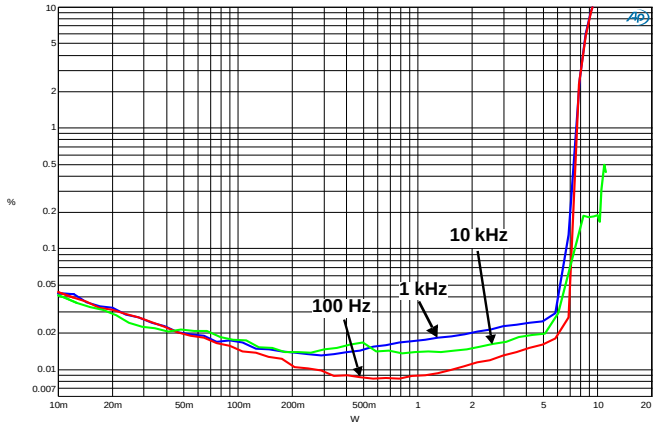


Figure 7. THD+N vs. Output Power (R_L= 8 Ω)

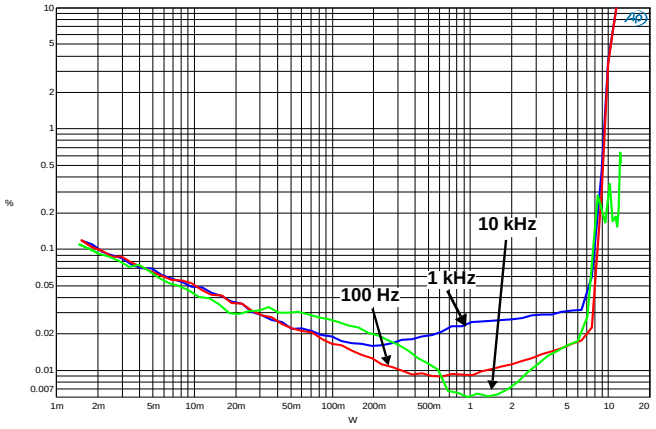


Figure 8. THD+N vs. Output Power (R_L= 6 Ω)

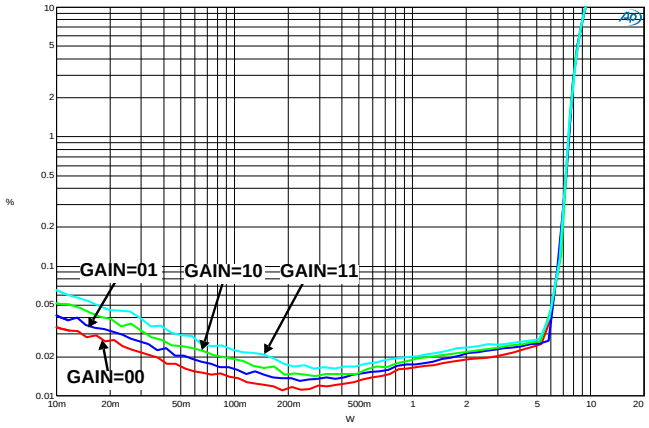


Figure 9. THD+N vs. Output Power (R_L= 8 Ω)

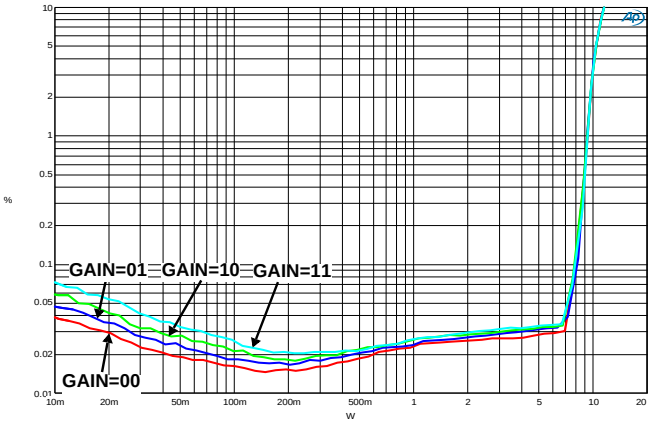


Figure 10. THD+N vs. Output Power (R_L= 6 Ω)

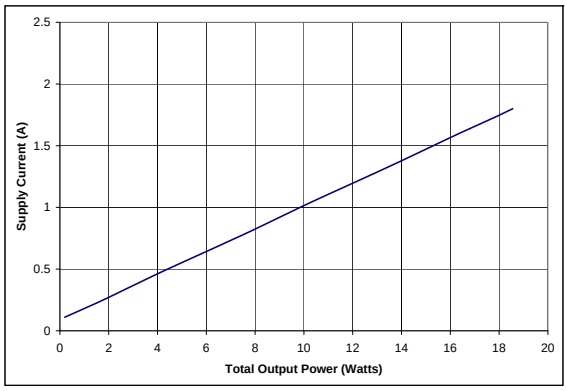


Figure 11. Supply Current vs. P_{OUT} (R_L= 8 Ω)

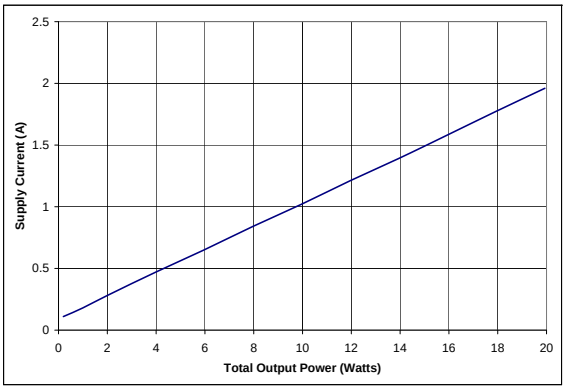


Figure 12. Supply Current vs. P_{OUT} (R_L= 6 Ω)

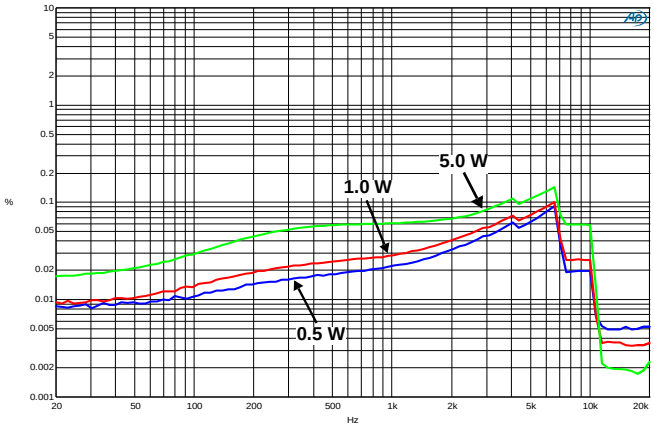


Figure 13. THD+N vs. Frequency (R_L= 8 Ω)

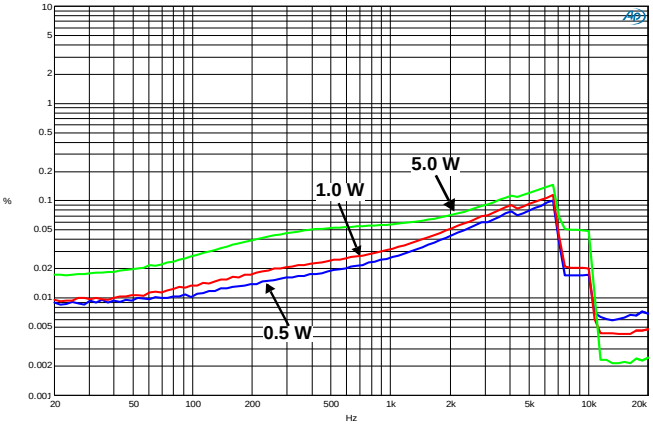


Figure 14. THD+N vs. Frequency (R_L= 6 Ω)

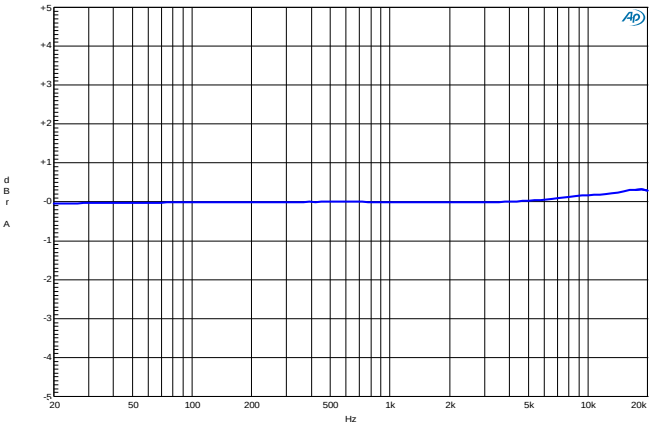


Figure 15. Frequency Response (P_{OUT} = 1 W, R_L= 8 Ω)

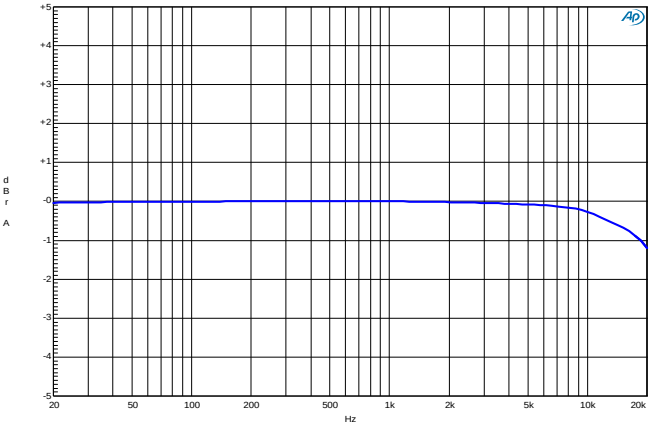


Figure 16. Frequency Response (P_{OUT} = 1 W, R_L= 6 Ω)

See Note below.

Note: The full-bridge output filter found on the CRD3511 reference design board implements 22µH inductors and is optimized for an 8 Ω load.

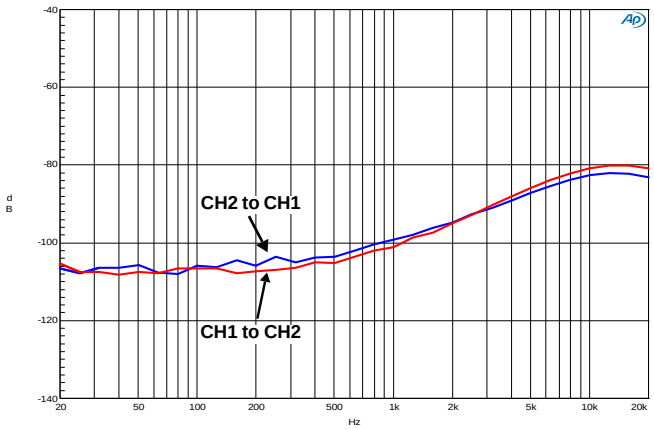


Figure 17. Crosstalk vs. Frequency (R_L= 8 Ω)

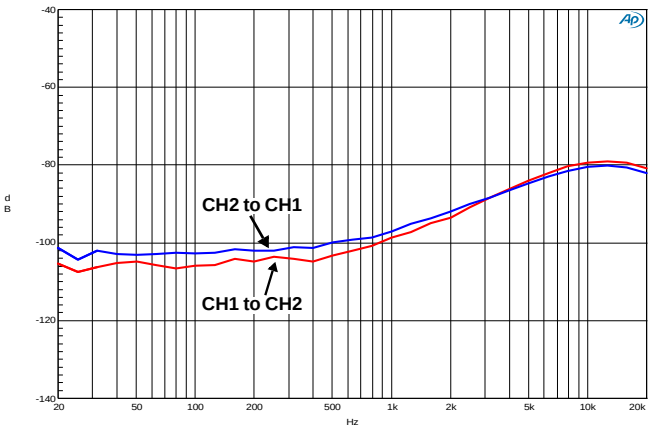


Figure 18. Crosstalk vs. Frequency (R_L= 6 Ω)

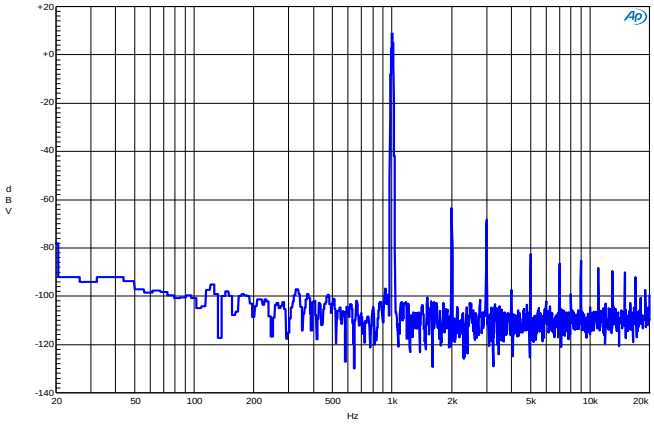


Figure 19. Output FFT (P_{OUT} = 1 W, R_L= 8 Ω)

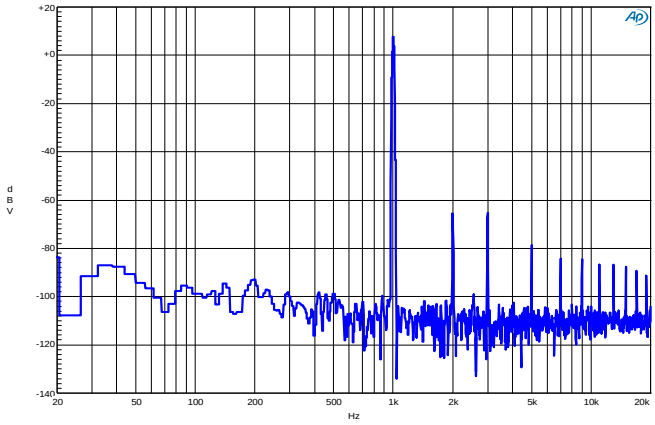


Figure 20. Output FFT (P_{OUT} = 1 W, R_L= 6 Ω)

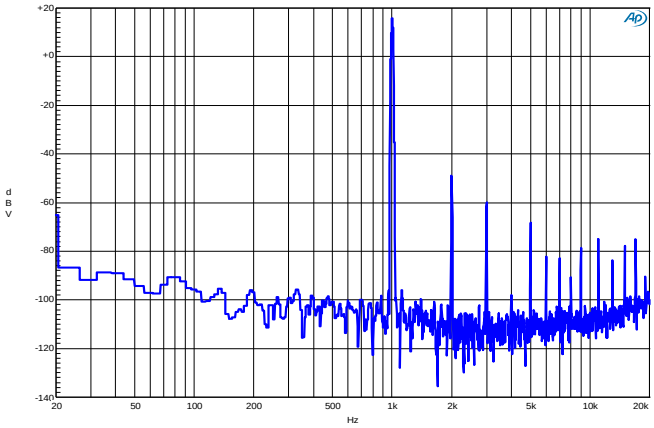


Figure 21. Output FFT (P_{OUT} = 5 W, R_L= 8 Ω)

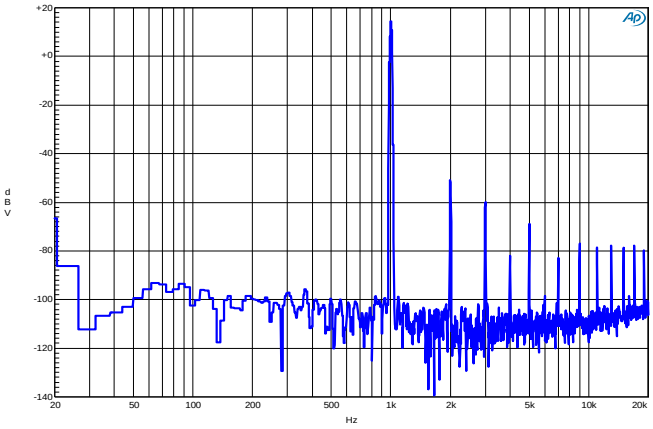


Figure 22. Output FFT (P_{OUT} = 5 W, R_L= 6 Ω)

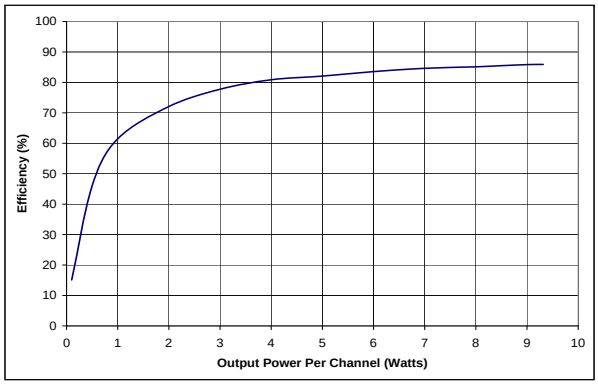


Figure 23. Efficiency (R_L= 8 Ω)

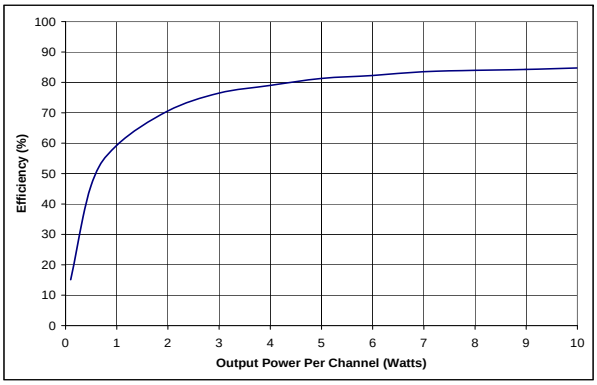


Figure 24. Efficiency (R_L= 6 Ω)

7. PARAMETER DEFINITIONS

Signal to Noise Ratio (SNR)

The ratio of the RMS value of the output signal, where Pout is equivalent to the specified output power at THD+N<1%, to the RMS value of the noise floor with no input signal applied and measured over the specified bandwidth, typically 20 Hz to 20 kHz. Expressed in decibels.

Dynamic Range (DYR)

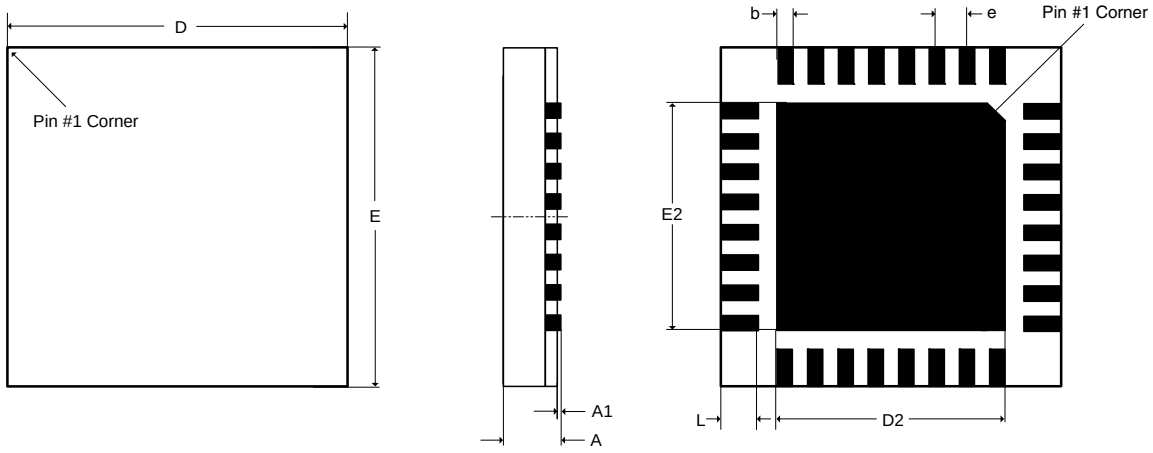
The ratio of the RMS value of the output signal produced when Pout is equivalent to the specified output power at THD+N<1% to the RMS sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement made with a -60 dBi input signal where dBi is referenced to the input signal amplitude resulting in the specified output power at THD+N<1%. This technique ensures that the distortion components are below the noise level and do not effect the measurement. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

8. PACKAGE DIMENSIONS

32L QFN (6 X 6 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.031	0.033	0.035	0.80	0.85	0.90	1
A1	0.00	--	0.05	0.00	--	0.05	1
A3	-	0.008 REF	-	-	0.203 REF	-	
b	0.008	0.010	0.012	0.20	0.25	0.30	1,2
D	-	0.2362 BSC	-	-	6.00 BSC	-	1
D2	0.177	0.181	0.185	4.50	4.60	4.70	1
E		0.2362 BSC			6.00 BSC		1
E2	0.177	0.181	0.185	4.50	4.60	4.70	1
e		0.026 BSC			0.65 BSC		1
L	0.014	0.016	0.018	0.35	0.40	0.45	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1994.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.

9. THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Junction to Case Thermal Impedance	θ_{JC}	-	1	-	°C/Watt

9.1 Thermal Flag

This device is designed to have the metal flag on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS3511. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$$\theta_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$$

where,
θ_{CA} = Thermal resistance of the metal plane in °C/Watt
$T_{J(MAX)}$ = Maximum rated operating junction temperature in °C, equal to 150 °C
T_A = Ambient temperature in °C
P_D = RMS power dissipation of the device, equal to $0.176*P_{RMS\text{-}OUT}$ (assuming 85% efficiency)
θ_{JC} = Junction-to-case thermal resistance of the device in °C/Watt, equal to 1 °C/Watt

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS3511	Stereo, 10W High-Efficiency Class-D Audio Amplifier	32-QFN	Yes	Commercial	-10° to +70°C	Rail	CS3511-CNZ
						Tape and Reel	CS3511-CNZR
CRD3511-Q1	2 x 10 W, 4 Layer / 1 oz. Copper Reference Design	-	-	-	-	-	CRD3511-Q1

11.REVISION HISTORY

Release	Changes
A1	Initial Release
A2	– Updated cover diagram. – Removed Dynamic Output Offset Voltage specification. – Updated Section 4.2 on page 12.
A3	– Updated PWM Output Over-Current specification in "AC Electrical Characteristics" table on page 7 and in the General Description on the front page. – FAULT pin (8) name updated to STATUS. – Updated Section 4.7 on page 14. – Updated "Under-Voltage Protection" table on page 14 and "DC Electrical Characteristics" table on page 8 from V5GEN to V5A for 5 V voltage sensing. – Updated Input Impedance specification in "AC Electrical Characteristics" table on page 7.
PP1	– Updated front page Features and Common Applications. – Updated DC Power Supply specification in "Absolute Maximum Ratings" table on page 6. – Updated THD+N, Dynamic Range, SNR, PSRR, Channel Separation, Amplifier Gain, Gain Matching, and Efficiency specifications in "AC Electrical Characteristics" table on page 7. – Updated Sleep Supply Current, Mute Supply Current, Quiescent Current, 5VGEN Nominal Voltage, REF Nominal Voltage, and BIASCAP Nominal Voltage in "DC Electrical Characteristics" table on page 8. – Updated Leakage Current specification in "Digital Interface Specifications" table on page 8. – Updated the typical audio performance plots in Section 6.
PP2	– Added SLEEP and MUTE pin transition time specification and information to the "DC Electrical Characteristics" table on page 8. – Added Section 4.6, Section 4.6.1, and Section 4.6.2. – Updated the typical audio performance plots in Section 6. – Updated Input Impedance specifications in "AC Electrical Characteristics" table on page 7. – Updated front page Features, "AC Electrical Characteristics" table on page 7, and Section 4.3 to reference four GAIN settings.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.