

# IP4221CZ6-S

Dual USB 2.0 integrated quad with ESD protection to IEC 61000-4-2, level 4 (Pb-free)

Rev. 01 — 29 April 2008

Product data sheet

## 1. Product profile

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### 1.1 General description

The IP4221CZ6-S is designed to protect Input/Output (I/O) ports that are sensitive to capacitive load, such as USB 2.0, Ethernet and DVI from destruction by ElectroStatic Discharge (ESD). It provides protection to downstream signal and supply components from ESD voltages as high as  $\pm 8$  kV (contact discharge).

The IP4221CZ6-S incorporates four pairs of ultra-low capacitance rail-to-rail diodes plus a Zener diode. The rail-to-rail diodes are connected to the Zener diode which allows ESD protection to be independent of supply voltage. The IP4221CZ6-S is fabricated using thin film-on-silicon technology integrating four ultra-low capacitance rail-to-rail ESD protection diodes in a miniature 6-terminal SOT886 package.

### 1.2 Features

- Pb-free and RoHS compliant
- ESD protection compliant to IEC 61000-4-2 level 4,  $\pm 8$  kV contact discharge
- Four ultra-low input capacitance (1 pF typical) rail-to-rail ESD protection diodes
- Low voltage clamping due to integrated Zener diode
- Small 6-terminal SOT886 package

### 1.3 Applications

- General-purpose downstream ESD protection high frequency analog signals and high-speed serial data transmission for ports inside:
  - ◆ Cellular and PCS mobile handsets
  - ◆ PC/notebook USB 2.0/IEEE 1394 ports
  - ◆ DVI/HDMI interfaces
  - ◆ Cordless telephones
  - ◆ Wireless data (WAN/LAN) systems
  - ◆ PDAs

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	ESD protection I/O 1	<p>bottom view</p>	
2	ground (GND)		
3	ESD protection I/O 2		
4	ESD protection I/O 3		
5	supply voltage (V <sub>CC</sub> )		
6	ESD protection I/O 4		

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## 3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4221CZ6-S	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

## 4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>I</sub>	input voltage		-0.5	+5.5	V
V <sub>esd</sub>	electrostatic discharge voltage	all pins; IEC 61000-4-2; level 4			
		contact discharge	-8	+8	kV
		air discharge	-15	+15	kV
T <sub>stg</sub>	storage temperature		-55	+125	°C

## 5. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>amb</sub>	ambient temperature		-40	+85	°C

## 6. Characteristics

**Table 5. Electrical Characteristics**  
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

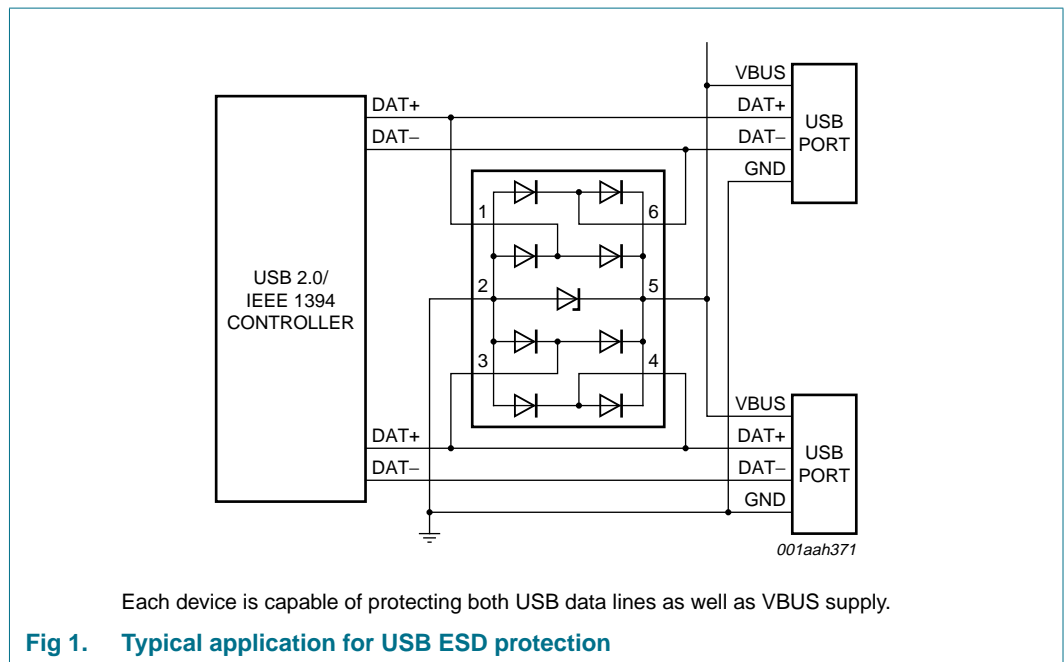
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C <sub>(I/O-GND)</sub>	input/output to ground capacitance	V <sub>I</sub> = 0 V; f = 1 MHz; V <sub>CC</sub> = 3 V	[1]	-	1.0	pF
I <sub>LR</sub>	reverse leakage current	V <sub>I</sub> = 3 V	[1]	-	100	nA
C <sub>sup</sub>	supply pin to ground capacitance	V <sub>I</sub> = 0 V; f = 1 MHz; V <sub>CC</sub> = 3 V	[2]	20	-	pF
V <sub>BR</sub>	breakdown voltage	Zener diode; I <sub>I</sub> = 1 mA	[2]	6	9	V
V <sub>F</sub>	forward voltage		-	0.7	-	V

- [1] Measured from pins 1, 3, 4 and 6 to ground.
- [2] Measured from pin 5 to pin 2.

## 7. Application information

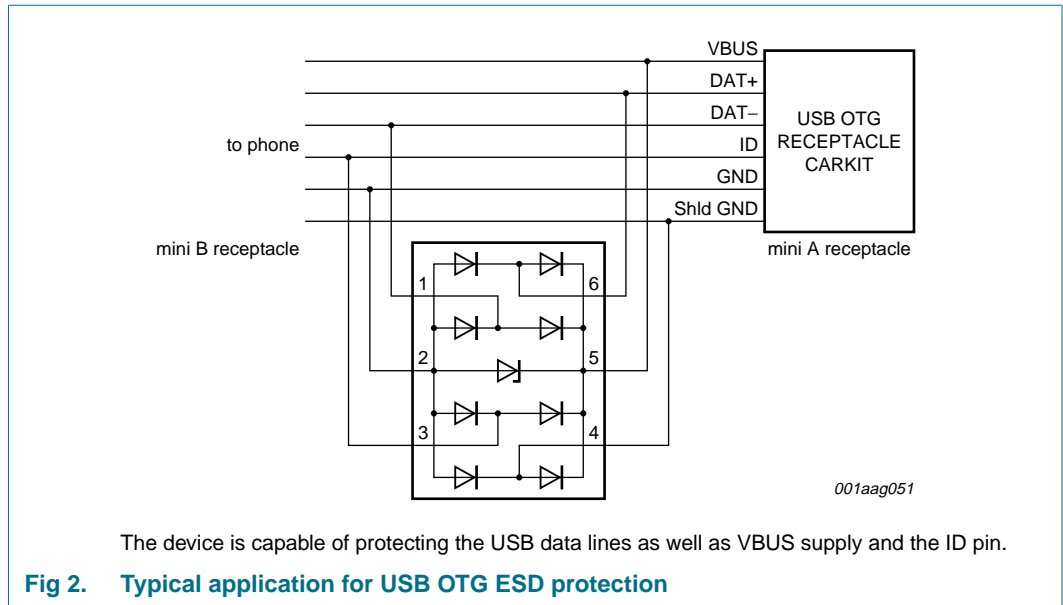
### 7.1 Universal serial bus 1.1 and 2.0 protection

The IP4221CZ6-S is optimized to protect two USB 2.0 ports against ESD.



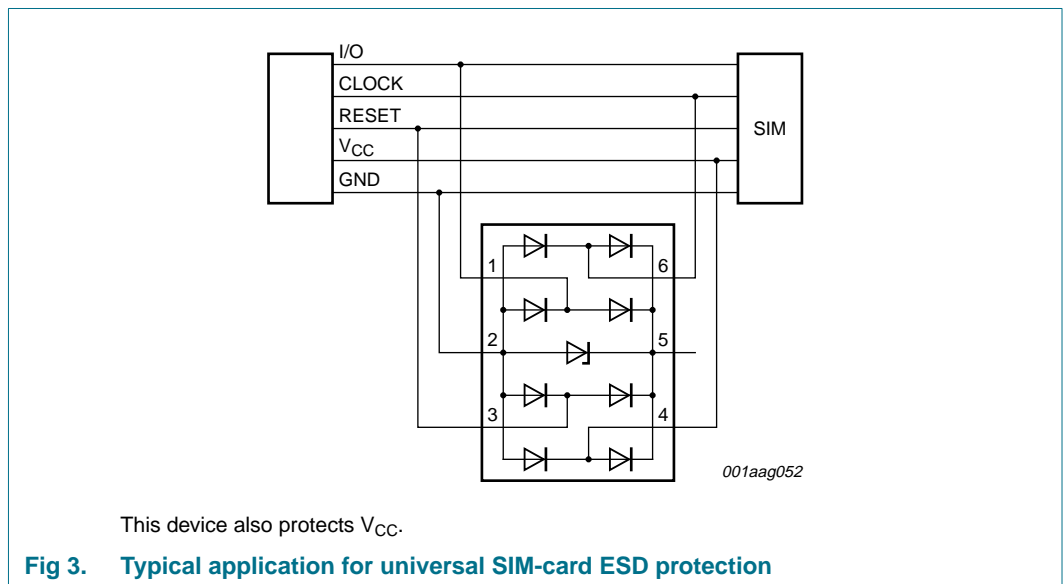
### 7.2 Universal serial bus OTG protection

The IP4221CZ6-S is optimized to protect USB 2.0 ports with or without OTG functionality against ESD.



### 7.3 Universal SIM-card protection

The IP4221CZ6-S protects the SIM-card interfaces against ESD.



7.4 IEEE 1394a/b protection

The IP4221CZ6-S is optimized to protect both the IEEE 1394 physical layer and the IEEE 1394 connector ports against ESD.

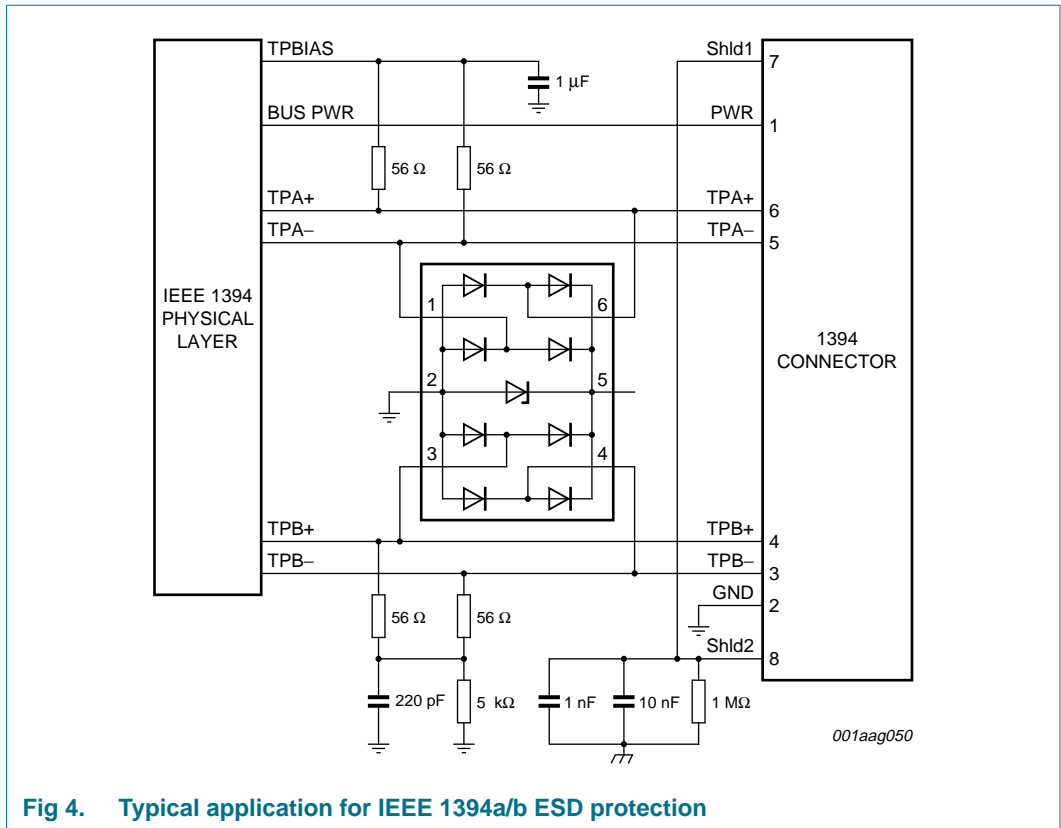


Fig 4. Typical application for IEEE 1394a/b ESD protection

7.5 Gigabit Ethernet transceiver protection

The IP4221CZ6-S protects the gigabit Ethernet transceiver against ESD.

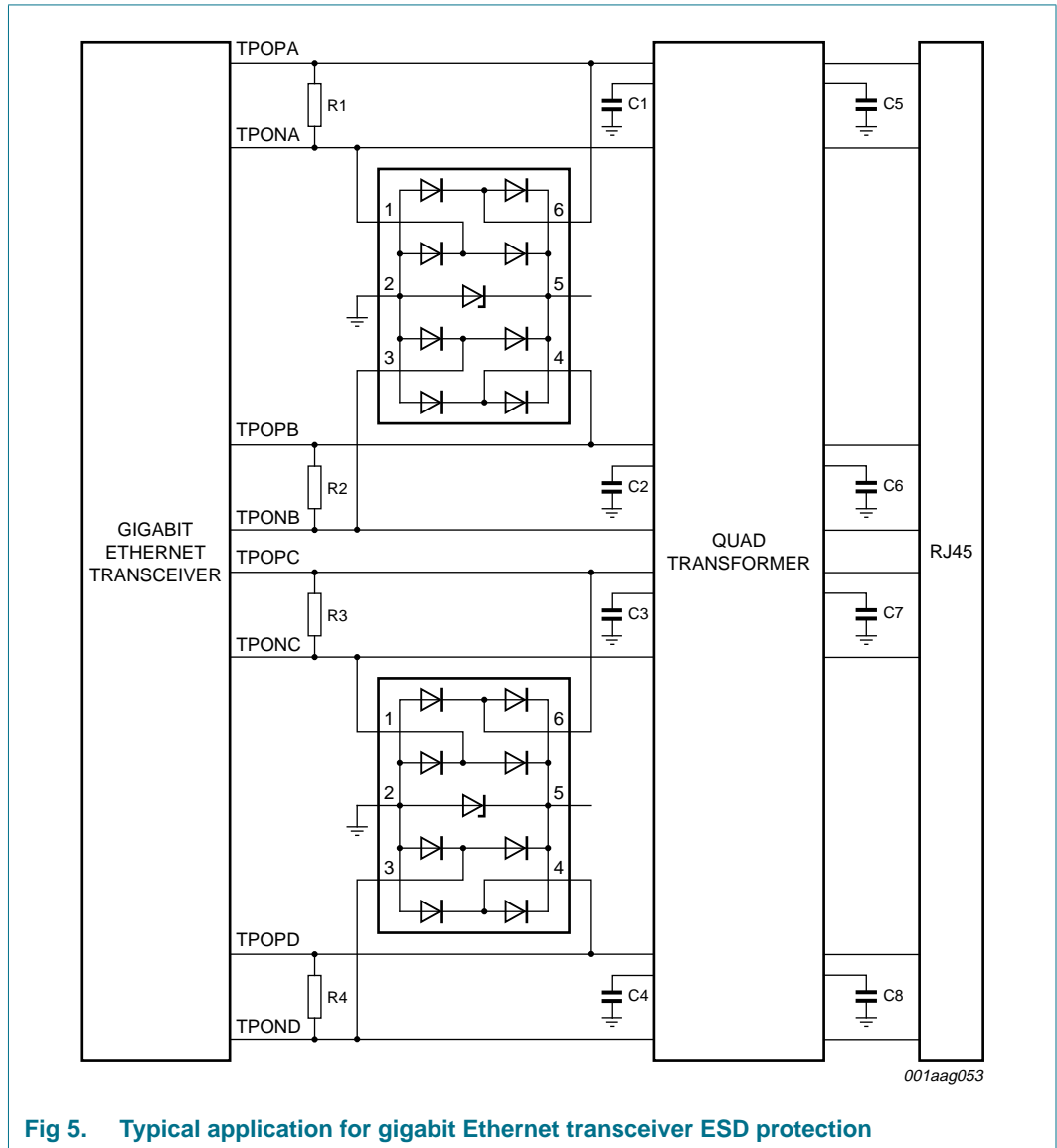


Fig 5. Typical application for gigabit Ethernet transceiver ESD protection

7.6 Universal microSD/TransFlash and SD-memory card protection

The IP4221CZ6-S protects each data line of the microSD/TransFlash device against ESD.

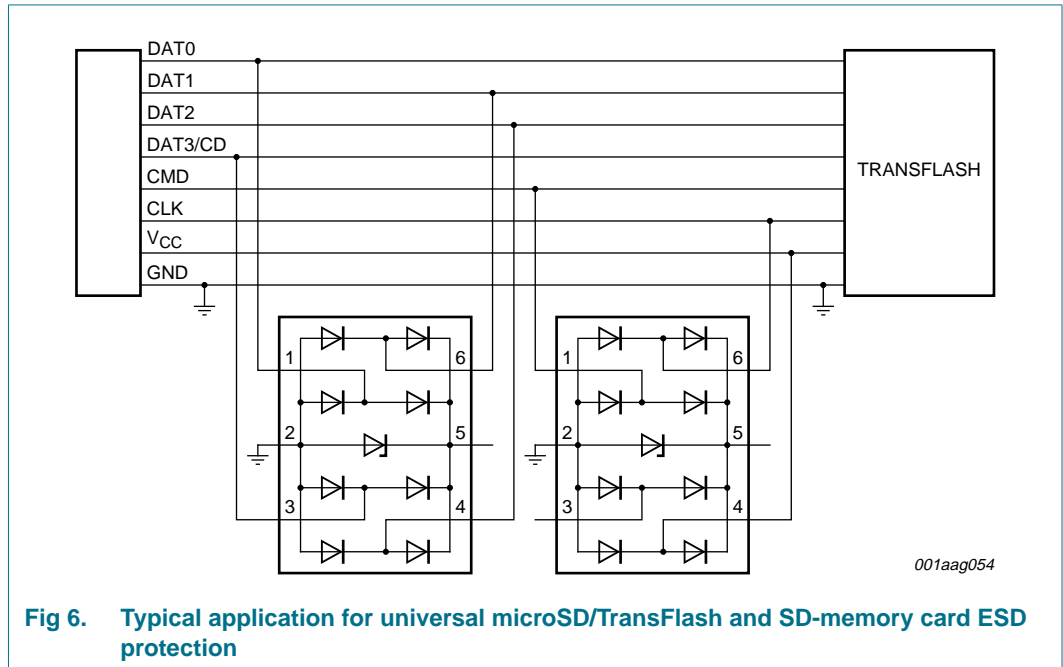
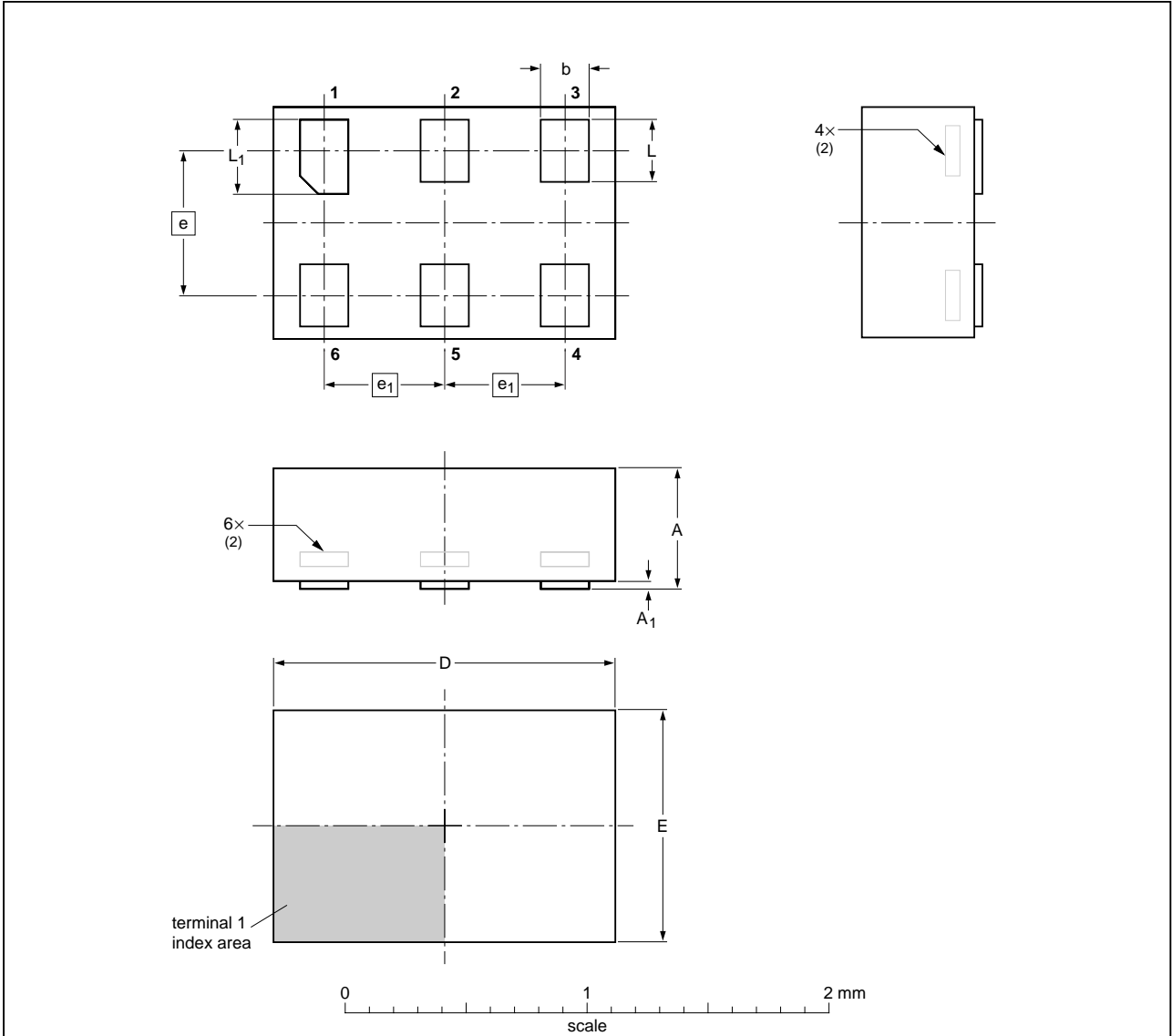


Fig 6. Typical application for universal microSD/TransFlash and SD-memory card ESD protection

8. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

- 1. Including plating thickness.
- 2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT886		MO-252			04-07-15 04-07-22

Fig 7. Package outline SOT886 (XSON6)



## 9. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 9.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 9.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 9.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

9.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 6](#) and [7](#)

Table 6. SnPb eutectic process (from J-STD-020C)

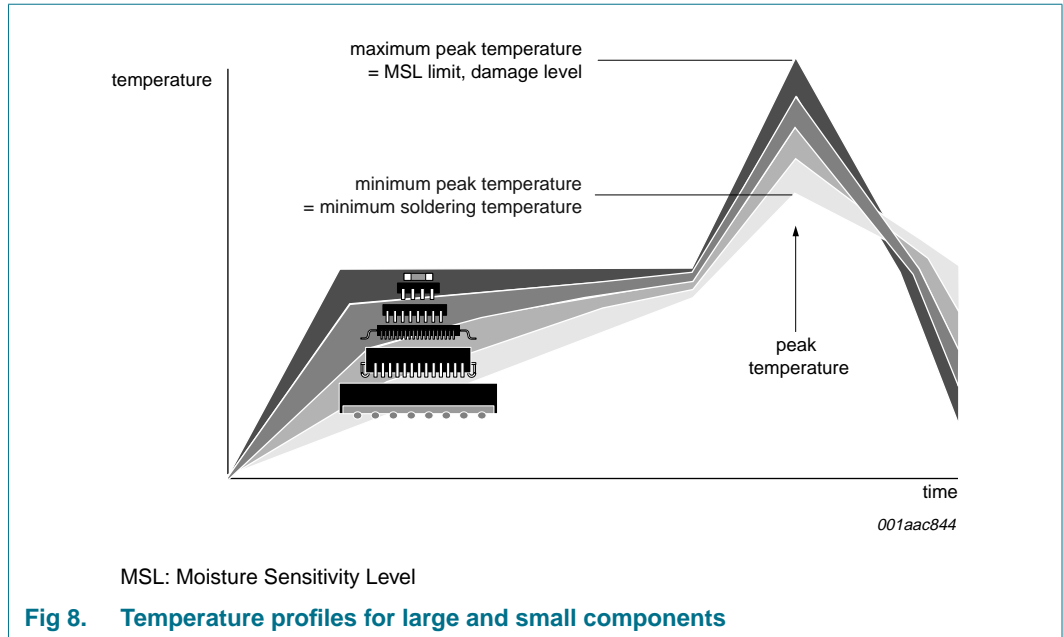
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 10. Abbreviations

**Table 8. Abbreviations**

Acronym	Description
DVI	Digital Video Interface
ESD	ElectroStatic Discharge
HDMI	High Definition Multimedia interface
LAN	Local Area Network
OTG	On-The-Go
PCS	Personal Computing System
PDA	Personal Digital Assistant
RoHS	Restriction of the use of certain Hazardous substances
SIM	Subscriber Identity Module
USB	Universal Serial Bus
WAN	Wide Area Network

## 11. Revision history

**Table 9. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4221CZ6-S_1	20080429	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 29 April 2008

Document identifier: IP4221CZ6-S\_1