

3A DDR Termination Regulator

FEATURES

Source and sink current capability of 3A
Low output voltage offset, ±20mV
High accuracy output voltage at full-load
Vout adjustable by external resistors
Low external component count
Current limit protection
Thermal protection
SO-8, TO-252-5 and TO-263-5 packages

APPLICATIONS

Mother Boards
Graphic Cards
DDR Termination Voltage Supply - supports
DDR1 (1.25VTT), DDR2 (0.9VTT), and meets
JEDEC SSTL-2 and SSTL-3 term. specifications

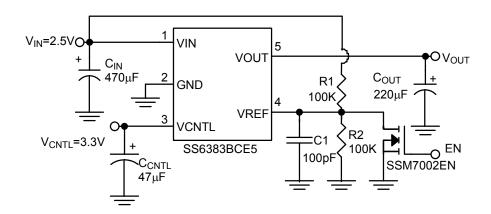
DESCRIPTION

The SS6383B linear regulator is designed to provide 3A source and sink current while regulating an output voltage to within 45mV.

The SS6383B converts voltage supplies ranging from 1.6V to 6V into an output voltage that is set by two external voltage-divider resistors. It provides an excellent voltage source for active termination schemes for high-speed transmission lines such as those seen in high-speed memory buses.

The built-in current-limiting in source and sink mode, together with thermal shutdown, provides maximum protection to the SS6383B against fault conditions.

TYPICAL APPLICATION CIRCUIT



This device is available with Pb-free lead finish (second-level interconnect) as SS6383BGxx

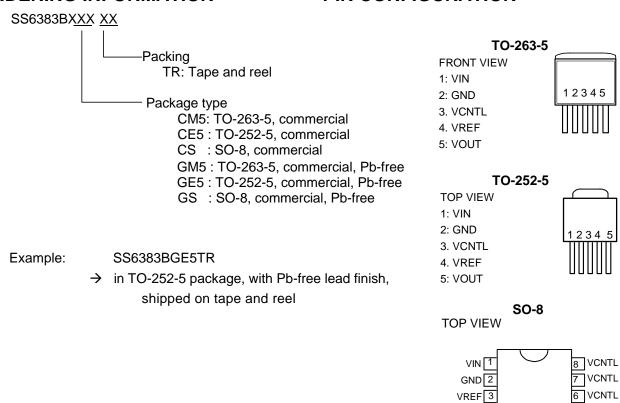
5 VCNTL

VOUT 4



ORDERING INFORMATION

PIN CONFIGURATION



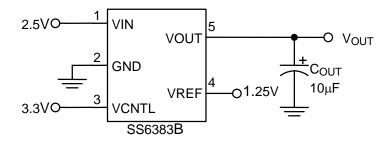
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		-0.4V to 7V
Operating Temperature Range		-40°C~85°C
Storage Temperature Range		-65°C ~150°C
Lead Temperature (Solder, 10sec)		260°C
Thermal Resistance θ_{JC}	TO-263	3°C /W
	TO-252	12.5°C /W
	SO-8	40°C /W
Thermal Resistance θ_{JA}	TO-263	60°C /W
(Assume no ambient airflow, no heatsink)	TO-252	100°C /W
	SO-8	160°C /W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.



TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

(V_{CNTL}=3.3V, V_{IN}=2.5V, V_{REF}=0.5V_{IN}, C_{OUT}=10μF, T_A=25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Input Voltage (DDR1/2)		V _{IN}	1.6	2.5	6	V	
		V _{CNTL}	3.0	3.3	6		
Output Voltage	I _{OUT} = 0mA	V _{OUT}		V_{REF}		V	
Output Voltage Offset	Iout = 0mA	Vos	-20		20	mV	
Local Description (DDD4/0)	I _{OUT} =0.1mA ~ +3A	ΔV _{LOR}	35 45	>/			
Load Regulation (DDR1/2)	I _{OUT} =0.1mA ~ -3A			35	45	mV	
Quiescent Current	V _{REF} <0.2V, V _{OUT} = OFF	IQ		8	30	μА	
Operating Current of V _{CNTL}	No load	I _{CNTL}		3	10	mA	
V _{REF} Bias Current	V _{REF} =1.25V		0		1	μА	
Current Limit		I _{IL}	3.2	4	6.5	Α	
THERMAL PROTECTION							
Thermal Shutdown Temperature	3.3V≤V _{CNTL} ≤5V	T _{SD}	125	150		°C	
Thermal Shutdown Hysteresis	Guaranteed by design			30		°C	
SHUTDOWN SPECIFICATIONS							
	Output ON (V _{REF} =0V→1.25V)		0.8				
Shutdown Threshold	Output OFF (V _{REF} =1.25V→0V)				0.2	V	

Note 2: V_{OS} is the voltage measurement, which is defined as the difference between V_{OUT} and $V_{REF.}$

Note 3: Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.

Note 4: Current limit is measured by pulsing a short time.

Note 5: To operate the system safely; V_{CNTL} must be always greater than V_{IN} .

Note 6: Specifications are guaranteed by Statistical Quality Controls (SQC), and not production tested, within the operating temperature range of -40°C to 85°C.

Note 7: DDR2 is not supported in the TO-263 package.



TYPICAL PERFORMANCE CHARACTERISTICS

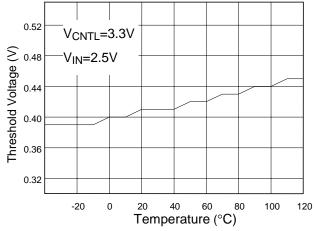


Fig. 1 Turn-On Threshold vs. Temp.

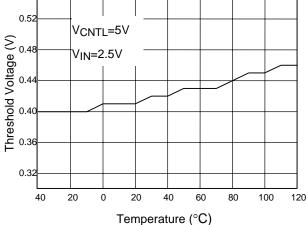


Fig. 2 Turn On Threshold vs. Temp.

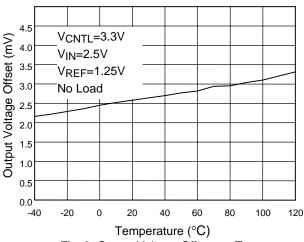


Fig. 3 Output Voltage Offset vs. Temp.

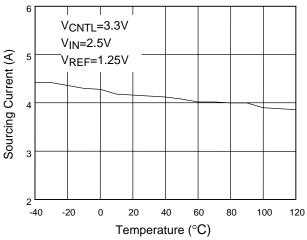


Fig. 4 Current-Limit (Sourcing) vs. Temp.

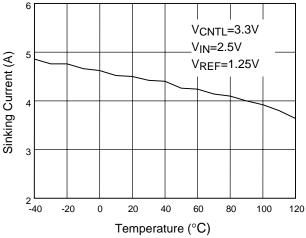


Fig. 5 Current-Limit (Sinking) vs. Temp.

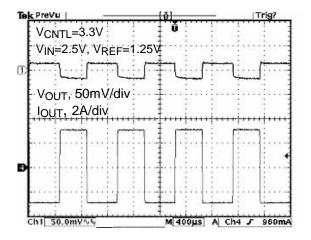
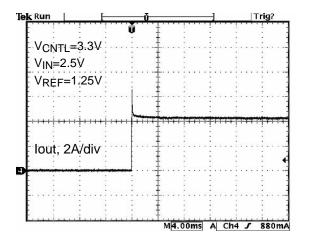


Fig. 6 Transient Response at 1.25V_{TT}/3A



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



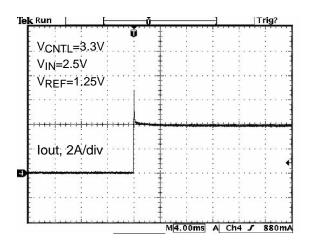
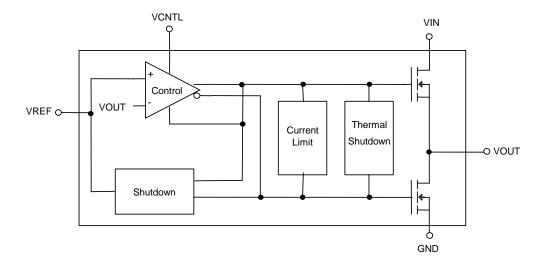


Fig. 7 Output Short-Circuit Protection (Sinking)

Fig. 8 Output Short-Circuit Protection (Sourcing)

BLOCK DIAGRAM



this pin low to shutdown device.



PIN DESCRIPTIONS (Pin numbers refer to TO-252/263)

PIN 1: VIN - Input supply pin. It provides

main power to create the external reference voltage by divider resistors for regulating

VREF and VOUT-

PIN 2: GND - Ground pin.

PIN 3: VCNTL - Input supply pin. It is used to

supply all the internal control

circuitry.

PIN 4: VREF - Reference voltage input. Pull

PIN 5: VOUT - Output pin.

APPLICATION INFORMATION

Layout Consideration

As the SS6383B is in either SO-8, TO-252-5 or TO-263-5 packages, it is unable to dissipate heat easily when it operates at high current. To avoid exceeding the maximum junction temperature, a suitable copper area must be used.

The large copper area shown at V_{CNTL} pins is able to relieve the thermal dissipation. Using the via to direct heat into the large copper area shown on the bottom layer also helps significantly.

All capacitors should be placed as close as possible to the relevant pins.

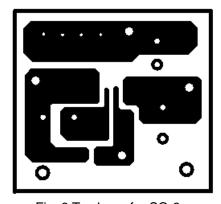


Fig. 9 Top layer for SO-8

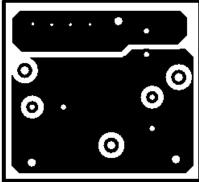


Fig. 10 Bottom layer for SO-8

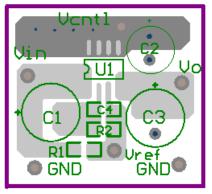
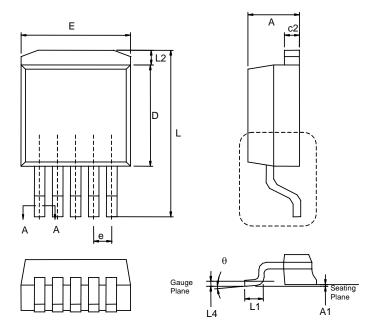


Fig. 11 Placement for SO-8



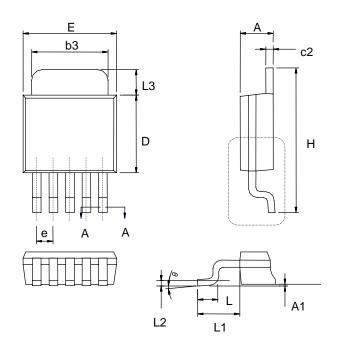
PHYSICAL DIMENSIONS

TO-263-5



SYMBOL	MIN	MAX
А	4.06	4.83
A1	0	0.15
C2	1.14	1.40
D	8.38	9.65
Е	9.65	10.29
е	1.70 BSC	
L	14.61	15.88
L1	2.29	2.79
L2		1.40
L4	0.25 BSC	
θ	0°	8°

TO-252-5

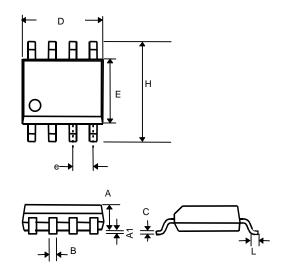


SYMBOL	MIN	MAX
А	2.19	2.38
A1	0	0.13
b3	5.21	5.46
c2	0.46	0.58
D	5.33	5.59
Е	6.35	6.73
е	1.27 BSC	
Н	9.40	10.41
L	1.4	1.78
L1	2.67 REF	
L2	0.51 BSC	
L3	1.52	2.03
θ	0°	8°



PHYSICAL DIMENSIONS (cont.)

SO-8



SYMBOL	MIN	MAX
Α	1.35	1.75
A1	0.10	0.25
В	0.33	0.51
С	0.19	0.25
D	4.80	5.00
Е	3.80	4.00
е	1.27(TYP)	
Н	5.80	6.20
L	0.40	1.27

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