ELPIDA

PRELIMINARY DATA SHEET

256MB Unbuffered DDR SDRAM DIMM

EBD26UB8ALFA (32M words × 64 bits, 2 Banks)

Description

The EBD26UB8ALFA is 32M words × 64 bits, 2 banks Double Data Rate (DDR) SDRAM unbuffered module, mounted 16 pieces of 128M bits DDR SDRAM (EDD1208ALTA) sealed in TSOP package. Read and write operations are performed at the cross points of the CLK and the /CLK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 184-pin socket type dual in line memory module (DIMM)
  - Outline: 133.35mm (Length) × 31.75mm (Height) × 4.00mm (Thickness)
  - Lead pitch: 1.27mm
- 2.5V power supply (VDD/VDDQ)
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 133MHz/100MHz (max.)
- Data inputs and outputs are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2, 4, 8
  - Burst read stop capability
- Programmable burst sequence
  - Sequential
  - Interleave
- Start addressing capability
  - Even and Odd
- Programmable /CAS latency (CL): 2, 2.5
- 4096 refresh cycles: 15.6μs (4096/64ms)
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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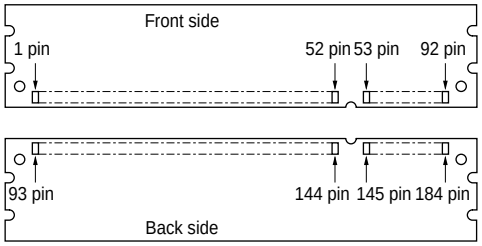
Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad	Mounted devices
EBD26UB8ALFA-7A	133	2.0			
EBD26UB8ALFA-75	133	2.5	184-pin DIMM	Gold	EDD1208ALTA
EBD26UB8ALFA-1A	100	2.0			

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	47	NC	93	VSS	139	VSS
2	DQ0	48	A0	94	DQ4	140	NC
3	VSS	49	NC	95	DQ5	141	A10
4	DQ1	50	VSS	96	VDDQ	142	NC
5	DQS0	51	NC	97	DM0/DQS9	143	VDDQ
6	DQ2	52	BA1	98	DQ6	144	NC
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	CLK1	62	VDDQ	108	VDD	154	/RAS
17	/CLK1	63	/WE	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	/CAS	111	CKE1	157	/CS0
20	DQ11	66	VSS	112	VDDQ	158	/CS1
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	NC	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	CLK2	121	DQ22	167	NC

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
30	VDDQ	76	/CLK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	NC	180	VDDQ
43	A1	89	VSS	135	NC	181	SA0
44	NC	90	NC	136	VDDQ	182	SA1
45	NC	91	SDA	137	CLK0	183	SA2
46	VDD	92	SCL	138	/CLK0	184	VDDSPD

Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A11 Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0, /CS1	Chip select
CKE0, CKE1	Clock enable
CLK0 to CLK2	Clock input
/CLK0 to /CLK2	Differential clock input
DQS0 to DQS7	Input and output data strobe
DM0 to DM7/DQS9 to DQS16	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VDD	Power for internal circuit
VDDQ	Power for DQ circuit
VDDSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VDDID	VDD indentication flag
NC	No connection

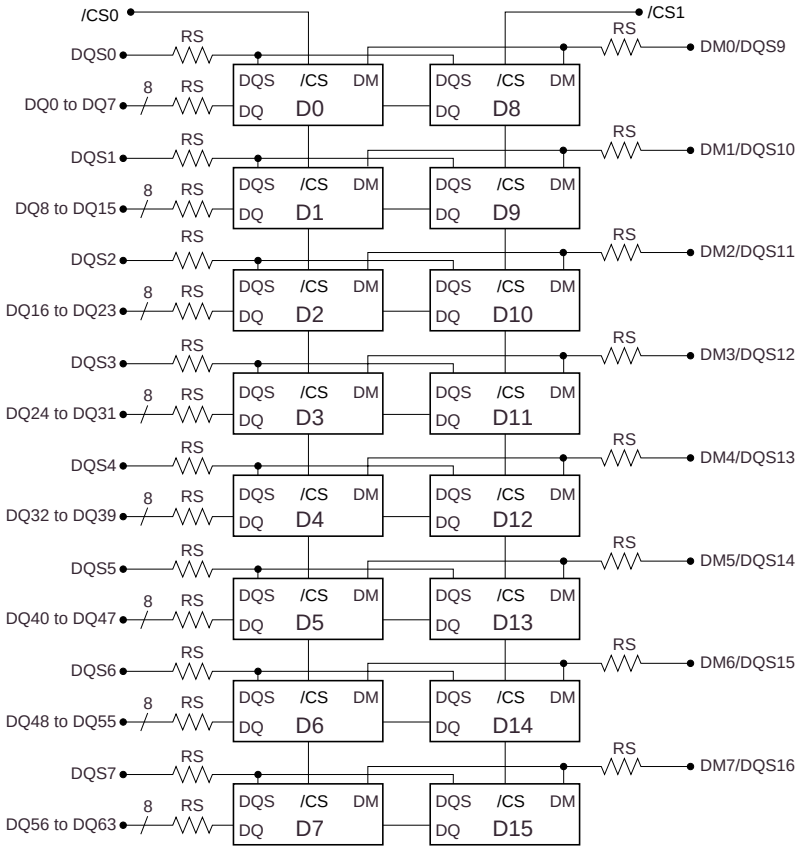
Serial PD Matrix

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	1	1	07H	DDR SDRAM
3	Number of row address	0	0	0	0	1	1	0	0	0CH	12
4	Number of column address	0	0	0	0	1	0	1	0	0AH	10
5	Number of DIMM banks	0	0	0	0	0	0	1	0	02H	2
6	Module data width	0	1	0	0	0	0	0	0	40H	64
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04H	SSTL2
9	DDR SDRAM cycle time, CL = 2.5 -7A	0	1	1	1	0	1	0	1	75H	7.5ns
	-75	0	1	1	1	0	1	0	1	75H	7.5ns
	-1A	1	0	1	0	0	0	0	0	A0H	10ns
10	SDRAM access from clock (tAC) -7A	0	1	1	1	0	1	0	1	75H	0.75ns
	-75	0	1	1	1	0	1	0	1	75H	0.75ns
	-1A	1	0	0	0	0	0	0	0	80H	0.8ns
11	DIMM configuration type	0	0	0	0	0	0	0	0	00H	None.
12	Refresh rate/type	1	0	0	0	0	0	0	0	80H	Norm
13	Primary SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00H	None.
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0EH	2,4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0CH	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02H	1
21	SDRAM module attributes	0	0	1	0	0	0	0	0	20H	Differential Clock
22	SDRAM device attributes: General	0	0	0	0	0	0	0	0	00H	VDD ± 0.2V
23	Minimum clock cycle time at CL = 2 -7A	0	1	1	1	0	1	0	1	75H	7.5ns
	-75	1	0	1	0	0	0	0	0	A0H	10ns
	-1A	1	0	1	0	0	0	0	0	A0H	10ns
24	Maximum data access time (tAC) from clock at CL = 2 -7A	0	1	1	1	0	1	0	1	75H	0.75ns
	-75	0	1	1	1	0	1	0	1	75H	0.75ns
	-1A	1	0	0	0	0	0	0	0	80H	0.8ns
25 to 26		0	0	0	0	0	0	0	0	00H	

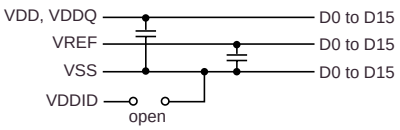
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
27	Minimum row precharge time (tRP) -7A	0	1	0	1	0	0	0	0	50H	20ns
	-75	0	1	0	1	0	0	0	0	50H	20ns
	-1A	0	1	0	1	0	0	0	0	50H	20ns
28	Minimum row active to row active delay (tRRD) -7A	0	0	1	1	1	1	0	0	3CH	15ns
	-75	0	0	1	1	1	1	0	0	3CH	15ns
	-1A	0	0	1	1	1	1	0	0	3CH	15ns
29	Minimum /RAS to /CAS delay (tRCD) -7A	0	1	0	1	0	0	0	0	50H	20ns
	-75	0	1	0	1	0	0	0	0	50H	20ns
	-1A	0	1	0	1	0	0	0	0	50H	20ns
30	Minimum active to precharge time (tRAS) -7A	0	0	1	0	1	1	0	1	2DH	45ns
	-75	0	0	1	0	1	1	0	1	2DH	45ns
	-1A	0	0	1	1	0	0	1	0	32H	50ns
31	Module bank density	0	0	1	0	0	0	0	0	20H	128M bytes
32	Address and command setup time before clock (tIS) -7A	1	0	0	1	0	0	0	0	90H	0.9ns
	-75	1	0	0	1	0	0	0	0	90H	0.9ns
	-1A	1	0	1	1	0	0	0	0	B0H	1.1ns
33	Address and command hold time after clock (tIH) -7A	1	0	0	1	0	0	0	0	90H	0.9ns
	-75	1	0	0	1	0	0	0	0	90H	0.9ns
	-1A	1	0	1	1	0	0	0	0	B0H	1.1ns
34	Data input setup time before clock (tDS) -7A	0	1	0	1	0	0	0	0	50H	0.5ns
	-75	0	1	0	1	0	0	0	0	50H	0.5ns
	-1A	0	1	1	0	0	0	0	0	60H	0.6ns
35	Data input hold time after clock (tDH) -7A	0	1	0	1	0	0	0	0	50H	0.5ns
	-75	0	1	0	1	0	0	0	0	50H	0.5ns
	-1A	0	1	1	0	0	0	0	0	60H	0.6ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00H	
62	SPD Revision	0	0	0	0	0	0	0	0	00H	
63	Checksum for bytes 0 to 62 -7A	0	1	1	1	0	0	1	0	72H	
	-75	1	0	0	1	1	1	0	1	9DH	
	-1A	0	1	0	0	0	0	1	1	43H	
64	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location										
73 to 90	Manufacturer's part number										
91 to 92	Revision code										
93 to 94	Manufacturing date										

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

Block Diagram



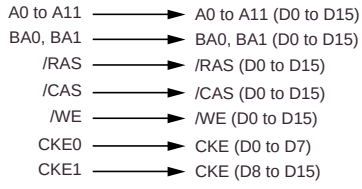
* D0 to D15: EDD1208ALTA
U0: 2k bits EEPROM
RS: 22Ω

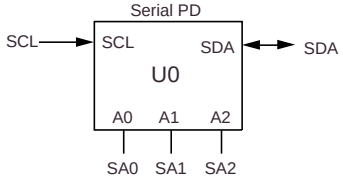


Clock wiring

Clock input	DDR SDRAMS
CLK0, /CLK0	4DRAM loads
CLK1, /CLK1	6DRAM loads
CLK2, /CLK2	6DRAM loads

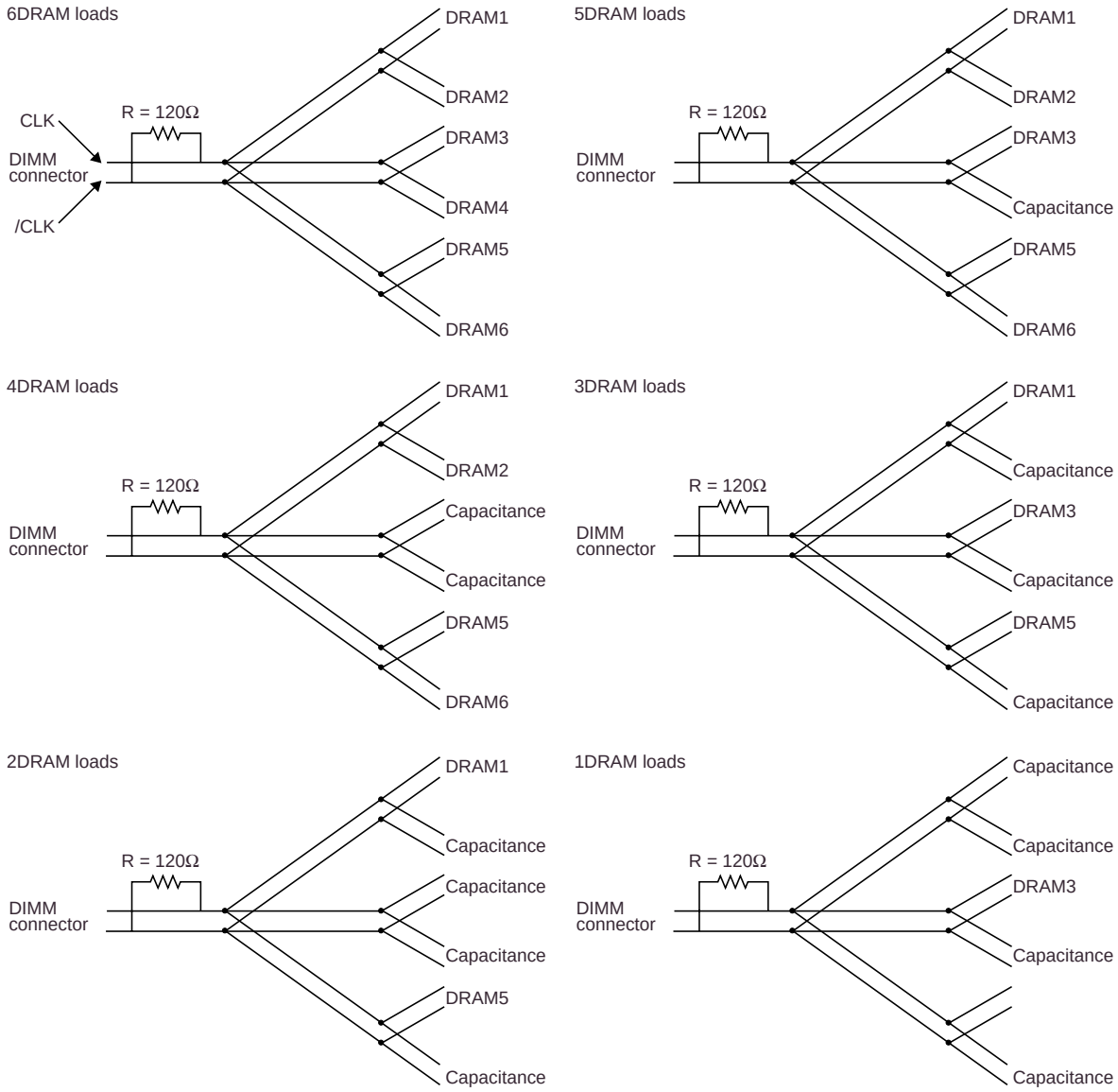
Note: Wire per Clock loading table/Wiring diagrams.





Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Logical Clock Net Structure



Pin Functions (1)

CLK, /CLK (input pin): The CLK and the /CLK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CLK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CLK and the /CLK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CLK and the /CLK.

/CS (input pin): When /CS is Low, commands and data can be input. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by the A0 to the A11 level at the cross point of the CLK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9) is loaded via the A0 to the A9 at the cross point of the CLK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0, BA1 (input pin): BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CLK cycle (= LCKEPW) at least, that is, if CKE changes at the cross point of the CLK rising edge and the VREF level with proper setup time tIS, at the next CLK rising edge CKE level must be kept with proper hold time tIH.

Pin Functions (2)

DQ (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

DM (input pins): DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and VREF

VDD and VDDQ (power supply pins): 2.5V is applied. (VDD is for the internal circuit and VDDQ is for the output buffer.)

VDDSPD (power supply pin): 2.5V is applied (For serial EEPROM).

VSS (power supply pin): Ground is connected.

Detailed Operation Part, AC Characteristics and Timing Waveforms

Refer to the EDD1204ALTA, EDD1208ALTA, EDD1216ALTA Series datasheet (E0136E).

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +3.6	V	1
Supply voltage relative to VSS	VDD, VDDQ	–0.5 to +3.6	V	1
Short circuit output current	IO	50	mA	
Power dissipation	PD	16	W	
Operating temperature	TA	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. Respect to VSS.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TA = 0 to +55°C)

Parameter	Symbol	min.	Typ	max.	Unit	Notes
Supply voltage	VDD, VDDQ	2.3	2.5	2.7	V	1, 2
	VSS	0	0	0	V	
Input reference voltage	VREF	0.49 × VDDQ	—	0.51 × VDDQ	V	1
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	1
DC Input high voltage	VIH	VREF + 0.18	—	VDDQ + 0.3	V	1, 3
DC Input low voltage	VIL	–0.3	—	VREF – 0.18	V	1, 4
DC Input signal voltage	VIN (dc)	–0.3	—	VDDQ + 0.3	V	5
DC differential input voltage	VSWING (dc)	0.36	—	VDDQ + 0.6	V	6

Notes: 1. All parameters are referred to VSS, when measured.
2. VDDQ must be lower than or equal to VDD.
3. VIH is allowed to exceed VDD up to 4.6V for the period shorter than or equal to 5ns.
4. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
5. VIN (dc) specifies the allowable dc execution of each differential input.
6. VSWING (dc) specifies the input differential voltage required for switching.

DC Characteristics (TA = 0 to 55°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	ICC0	-7A -75 -1A	TBD	mA	CKE ≥ VIH, tRC = tRC (min.)	1, 2, 5
Operating current (ACTV-READ-PRE)	ICC1	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5, tRC = tRC (min.)	1, 2, 5
Idle power down standby current	ICC2P	-7A -75 -1A	TBD	mA	CKE ≤ VIL	4
Idle standby current	ICC2N	-7A -75 -1A	TBD	mA	CKE ≥ VIH, /CS ≥ VIH	4
Active power down standby current	ICC3P	-7A -75 -1A	TBD	mA	CKE ≤ VIL	3
Active standby current	ICC3N	-7A -75 -1A	TBD	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = tRAS (max.)	3
Operating current (Burst read operation)	ICC4R	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Operating current (Burst write operation)	ICC4W	-7A -75 -1A	TBD	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Auto refresh current	ICC5	-7A -75 -1A	TBD	mA	tRFC = tRFC (min.) Input ≤ VIL or ≥ VIH	
Self refresh current	ICC6	-7A -75 -1A	TBD	mA	Input ≥ VDD – 0.2V Input ≤ 0.2V.	

Notes. 1. These ICC data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The ICC data on this table are measured with regard to tCK = tCK (min.) in general.

DC Characteristics2 (TA = 0 to 70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–32	32	µA	VDD ≥ VIN ≥ VSS	
Output leakage current	ILO	–10	10	µA	VDD ≥ VOUT ≥ VSS	
Output high current	IOH	–15.2	—	mA	VOUT = 1.95V	
Output low current	IOL	15.2	—	mA	VOUT = 0.35V	

Pin Capacitance (TA = 25°C, VDD, VDDQ = 2.5V ± 0.2V)

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /CS, CKE	TBD	pF	
Input capacitance	CI2	CLK, /CLK	TBD	pF	
Data and DQS input/output capacitance	CO	DQ, DQS	TBD	pF	

AC Characteristics

Synchronous Characteristics

		-7A		-75		-1A			
Parameter	Symbol	min.	max.	min.	max.	min.	max.	Unit	Note
Clock cycle time CL = 2.5	tCK	7.5	12	7.5	12	10	12	ns	
CL = 2		7.5	12	10	12	10	12	ns	
CLK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CLK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQ output access time from CLK, /CLK	tAC	–0.75	0.75	–0.75	0.75	–0.8	0.8	ns	
DQS output access time from CLK, /CLK	tDQSCK	–0.75	0.75	–0.75	0.75	–0.8	0.8	ns	
DQS-DQ skew (for DQS and associated DQ signals)	tDQSQ	—	0.5	—	0.5	—	0.6	ns	
DQS-DQ skew (for DQS and all DQ signals)	tDQSQA	—	0.5	—	0.5	—	0.6	ns	
Data out low-impedance time from CLK, /CLK	tLZ	–0.75	0.75	–0.75	0.75	–0.8	0.8	ns	
Data out high-impedance time from CLK, /CLK	tHZ	–0.75	0.75	–0.75	0.75	–0.8	0.8	ns	
Half clock period	tHP	tCH, tCL	—	tCH, tCL	—	tCH, tCL	—	ns	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQ/DQS output hold time from DQS	tQH	tHP – 0.75	—	tHP – 0.75	—	tHP – 1	—	ns	
DQ and DM input setup time	tDS	0.5	—	0.5	—	0.6	—	ns	
DQ and DM input hold time	tDH	0.5	—	0.5	—	0.6	—	ns	
DQ and DM input pulse width (for each input)	tDIPW	1.75	—	1.75	—	2	—	ns	
Write preamble setup time	tWPRES	0	—	0	—	0	—	ns	
Write preamble	tWPRE	0.25	—	0.25	—	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	0.35	—	tCK	
DQS falling edge to CLK setup time	tDSS	0.2	—	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CLK	tDSH	0.2	—	0.2	—	0.2	—	tCK	
Address and control input setup time	tIS	0.9	—	0.9	—	1.1	—	ns	
Address and control input hold time	tIH	0.9	—	0.9	—	1.1	—	ns	
Address and control input pulse width	tIPW	2.2	—	2.2	—	2.5	—	ns	
Internal write to read command delay	tWTR	1	—	1	—	1	—	tCK	

Synchronous Characteristics Example

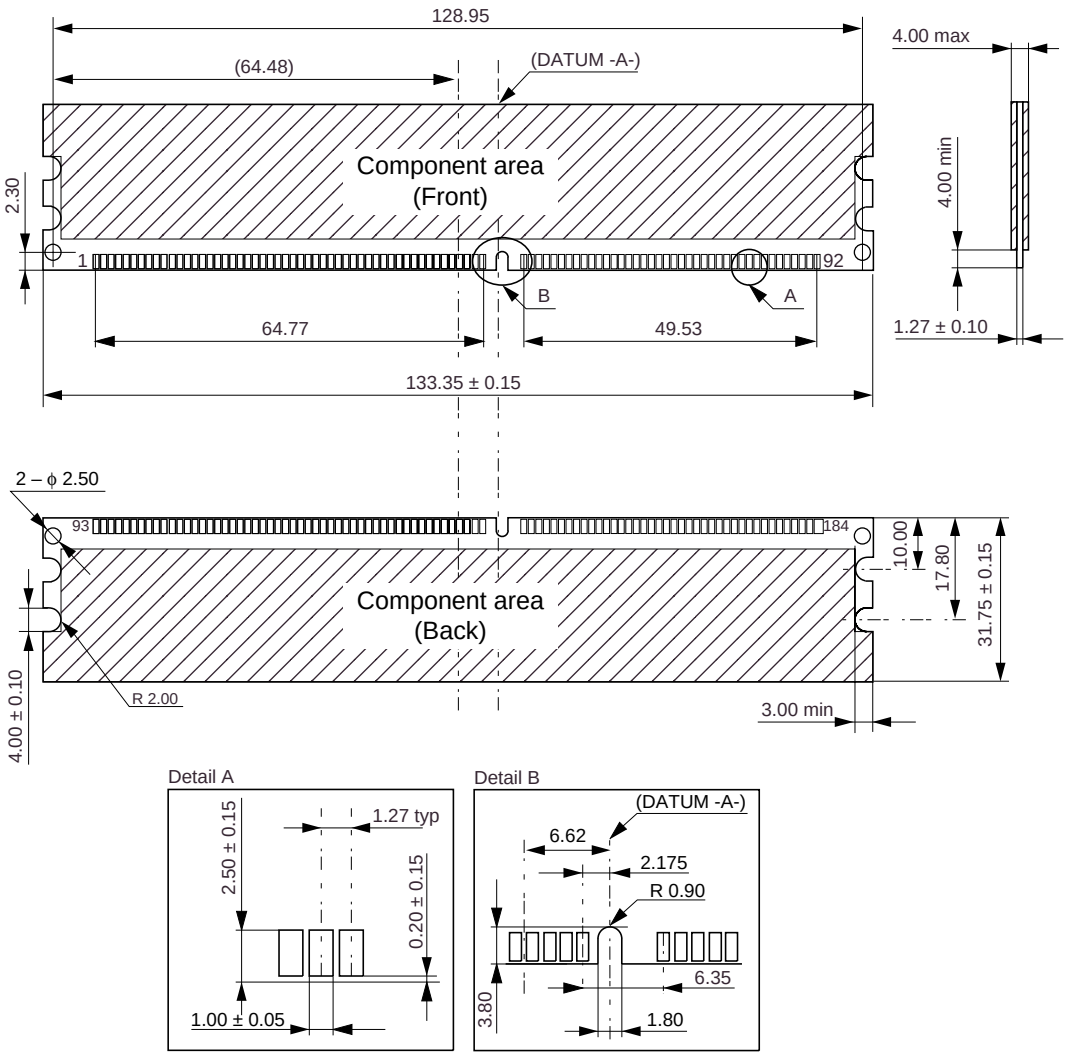
tCK	7.5 ns		10 ns		
Symbol	min.	max.	min.	max.	Unit
tCH	3.4	4.1	4.5	5.5	ns
tCL	3.4	4.1	4.5	5.5	ns
tRPRE	6.75	8.25	9	11	ns
tRPST	3	4.5	4	6	ns
tWPRE	0.25	—	2.5	—	ns
tWPST	3	4.5	4	6	ns
tDQSS	5.6	9.4	7.5	12.5	ns
tDQSH	2.63	—	3.5	—	ns
tDQSL	2.63	—	3.5	—	ns
tDSS	1.5	—	2	—	ns
tDSH	1.5	—	2	—	ns
tWTR	7.5	—	10	—	ns

Asynchronous Characteristics

		-7A		-75		-1A		
Parameter	Symbol	min.	max.	min.	max.	min.	max.	Unit
ACT to REF/ACT command period (operation)	tRC	65	—	65	—	70	—	ns
REF to REF/ACT command period (refresh)	tRFC	75	—	75	—	80	—	ns
ACT to PRE command period	tRAS	45	120,000	45	120,000	50	120,000	ns
PRE to ACT command period	tRP	20	—	20	—	20	—	ns
ACT to READ/WRITE delay	tRCD	20	—	20	—	20	—	ns
ACT(one) to ACT(another) command period	tRRD	15	—	15	—	15	—	ns
Write recovery time	tWR	2	—	2	—	2	—	CLK
Auto precharge write recovery time + precharge time	tDAL	TBD	—	TBD	—	TBD	—	ns
Mode register set command cycle time	tMRD	15	—	15	—	15	—	ns
Exit self refresh to command	tXSNR	75	—	75	—	80	—	ns
Average periodic Refresh interval	tREF1	—	15.6	—	15.6	—	15.6	μs

Physical Outline

Unit: mm



Note: Tolerance on all dimensions ± 0.13 unless otherwise specified.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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