

FEATURES

- Selectable LVDS/CMOS outputs
- Up to 6 LVDS (1.2 GHz) or 12 CMOS (250 MHz) outputs
- <16 mW per channel (100 MHz operation)
- 54 fs integrated jitter (12 kHz to 20 MHz)
- 100 fs additive broadband jitter
- 2.0 ns propagation delay (LVDS)
- 135 ps output rise/fall (LVDS)
- 65 ps output-to-output skew (LVDS)
- Sleep mode
- Pin-programmable control
- 1.8 V power supply

APPLICATIONS

- Low jitter clock distribution
- Clock and data signal restoration
- Level translation
- Wireless communications
- Wired communications
- Medical and industrial imaging
- ATE and high performance instrumentation

GENERAL DESCRIPTION

The ADCLK846 is a 1.2 GHz/250 MHz, LVDS/CMOS, fanout buffer optimized for low jitter and low power operation. Possible configurations range from 6 LVDS to 12 CMOS outputs, including combinations of LVDS and CMOS outputs. Two control lines are used to determine whether fixed blocks of outputs are LVDS or CMOS outputs.

FUNCTIONAL BLOCK DIAGRAM

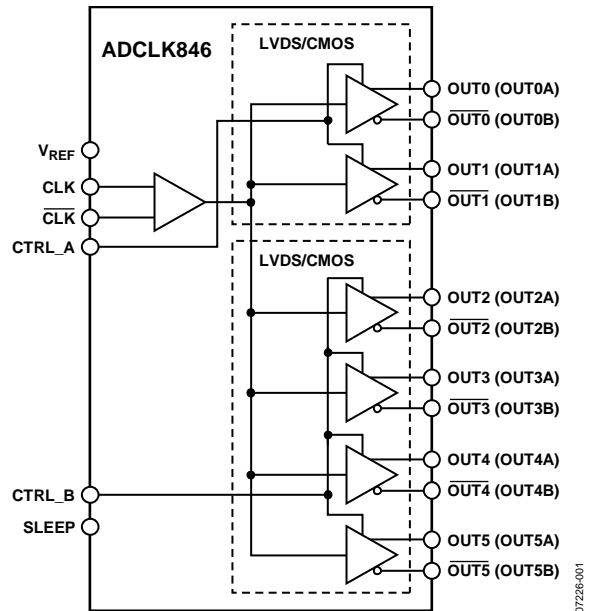


Figure 1.

The clock input accepts various types of single-ended and differential logic levels including LVPECL, LVDS, HSTL, CML, and CMOS.

Table 8 provides interface options for each type of connection. The SLEEP pin enables a sleep mode to power down the device.

This device is available in a 24-pin LFCSP package. It is specified for operation over the standard industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

Rev. A

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TABLE OF CONTENTS

| | | | |
|---|---|---|----|
| Features | 1 | Typical Performance Characteristics | 8 |
| Applications | 1 | Functional Description | 11 |
| Functional Block Diagram | 1 | Clock Inputs | 11 |
| General Description | 1 | AC-Coupled Applications | 11 |
| Revision History | 2 | Clock Outputs | 12 |
| Specifications | 3 | Control and Function Pins | 12 |
| Electrical Characteristics | 3 | Power Supply | 12 |
| Timing Characteristics | 4 | Applications Information | 13 |
| Clock Characteristics | 5 | Using the ADCLK846 Outputs for ADC Clock | |
| Logic and Power Characteristics | 5 | Applications | 13 |
| Absolute Maximum Ratings | 6 | LVDS Clock Distribution | 13 |
| Determining Junction Temperature | 6 | CMOS Clock Distribution | 13 |
| ESD Caution | 6 | Input Termination Options | 14 |
| Thermal Performance | 6 | Outline Dimensions | 15 |
| Pin Configuration and Function Descriptions | 7 | Ordering Guide | 15 |

REVISION HISTORY

6/09—Rev. 0 to Rev. A

No Content Updates..... Throughout

4/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Typical values are given for $V_S = 1.8\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted. Minimum and maximum values are given over the full $V_S = 1.8\text{ V} \pm 5\%$ and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ variations, unless otherwise noted. Input slew rate $> 1\text{ V/ns}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---------------------------------|------------------|---------------|---------|----------------|---------------|--|
| CLOCK INPUTS | | | | | | |
| Input Frequency | | 0 | | 1200 | MHz | Differential input |
| Input Sensitivity, Differential | | | 150 | | mV p-p | Jitter performance is improved with higher slew rates (greater voltage swing) |
| Input Level | | | | 1.8 | V p-p | Larger voltage swings can turn on the protection diodes and can degrade jitter performance |
| Input Common-Mode Voltage | V_{CM} | $V_S/2 - 0.1$ | | $V_S/2 + 0.05$ | V | Inputs are self-biased; enables ac coupling |
| Input Common-Mode Range | V_{CMR} | 0.4 | | $V_S - 0.4$ | V | Inputs are dc-coupled with 200 mV p-p signal applied |
| Input Voltage Offset | | | 30 | | mV | |
| Input Sensitivity, Single-Ended | | | 150 | | mV p-p | CLK ac-coupled; \overline{CLK} ac-bypassed to ground |
| Input Resistance (Differential) | | | 7 | | k Ω | |
| Input Capacitance | C_{IN} | | 2 | | pF | |
| Input Bias Current (Each Pin) | | -350 | | +350 | μA | Full input swing |
| LVDS CLOCK OUTPUTS | | | | | | |
| Output Frequency | | | | 1200 | MHz | Termination = 100 Ω ; differential (\overline{OUTx} , \overline{OUTx}) |
| Differential Output Voltage | V_{OD} | 247 | 344 | 454 | mV | See Figure 9 for a swing vs. frequency plot |
| | ΔV_{OD} | | | 50 | mV | |
| Offset Voltage | V_{OS} | 1.125 | 1.25 | 1.375 | V | |
| | ΔV_{OS} | | | 50 | mV | |
| Short-Circuit Current | I_{SA}, I_{SB} | | 3 | 6 | mA | Each pin (output shorted to GND) |
| CMOS CLOCK OUTPUTS | | | | | | |
| Output Frequency | | | | 250 | MHz | Single-ended; termination = open \overline{OUTx} and \overline{OUTx} in phase |
| Output Voltage High | V_{OH} | $V_S - 0.1$ | | | V | At 1 mA load |
| | | $V_S - 0.35$ | | | V | At 10 mA load |
| Output Voltage Low | V_{OL} | | | 0.1 | V | At 1 mA load |
| | | | | 0.35 | V | At 10 mA load |
| Reference Voltage | V_{REF} | | | | V | |
| Output Voltage | | $V_S/2 - 0.1$ | $V_S/2$ | $V_S/2 + 0.1$ | V | $\pm 500\ \mu\text{A}$ |
| Output Resistance | | | 60 | | Ω | |
| Output Current | | | | 500 | μA | |

ADCLK846

TIMING CHARACTERISTICS

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|------------|-----|-----|-----|-----------------|---|
| LVDS OUTPUTS | | | | | | |
| Output Rise/Fall Time | t_R, t_F | | 135 | 235 | ps | Termination = 100 Ω differential; 3.5 mA 20% to 80% measured differentially |
| Propagation Delay, CLK-to-LVDS Output | t_{PD} | 1.5 | 2.0 | 2.7 | ns | $V_{ICM} = V_{REF}, V_{ID} = 0.5 V$ |
| Temperature Coefficient | | | 2.0 | | ps/ $^{\circ}C$ | |
| Output Skew ¹ | | | | | | |
| All LVDS Outputs on the Same Part | | | | 65 | ps | |
| All LVDS Outputs Across Multiple Parts | | | | 390 | ps | |
| Additive Time Jitter | | | | | | |
| Integrated Random Jitter | | | 54 | | fs rms | BW = 12 kHz to 20 MHz, CLK = 1000 MHz |
| | | | 74 | | fs rms | BW = 50 kHz to 80 MHz, CLK = 1000 MHz |
| | | | 86 | | fs rms | BW = 12 kHz to 20 MHz, CLK = 1000 MHz |
| Broadband Random Jitter ² | | | 150 | | fs rms | Input slew rate = 1 V/ns |
| Crosstalk-Induced Jitter | | | 260 | | fs rms | Calculated from spur energy with an interferer 10 MHz offset from carrier |
| CMOS OUTPUTS | | | | | | |
| Output Rise/Fall Time | t_R, t_F | | 525 | 950 | ps | Termination = open 20% to 80%; CMOS load = 10 pF |
| Propagation Delay, CLK-to-CMOS Output | t_{PD} | 2.5 | 3.2 | 4.2 | ns | 10 pF load |
| Temperature Coefficient | | | 2.2 | | ps/ $^{\circ}C$ | |
| Output Skew ² | | | | | | |
| All CMOS Outputs on the Same Part | | | | 175 | ps | |
| All CMOS Outputs Across Multiple Parts | | | | 640 | ps | |
| Additive Time Jitter | | | | | | |
| Integrated Random Jitter | | | 56 | | fs rms | BW = 12 kHz to 20 MHz, CLK = 200 MHz |
| Broadband Random Jitter ³ | | | 100 | | fs rms | Input slew = 2 V/ns; see Figure 11 |
| Crosstalk-Induced Jitter | | | 260 | | fs rms | Calculated from spur energy with an interferer 10 MHz offset from carrier |
| LVDS-TO-CMOS OUTPUT SKEW² | | | | | | |
| LVDS Output(s) and CMOS Output(s) on the Same Part | | 0.8 | | 1.6 | ns | CMOS load = 10 pF and LVDS load = 100 Ω |

¹ This is the difference between any two similar delay paths while operating at the same voltage and temperature.

² Measured at rising edge of clock signal.

³ Calculated from SNR of ADC method.

CLOCK CHARACTERISTICS

Table 3. Clock Output Phase Noise

| Parameter | Min | Typ | Max | Unit | Conditions |
|--|-----|------|-----|--------|---|
| CLK-TO-LVDS ABSOLUTE PHASE NOISE 1000 MHz | | -90 | | dBc/Hz | Input slew rate > 1 V/ns At 10 Hz offset |
| | | -108 | | dBc/Hz | At 100 Hz offset |
| | | -117 | | dBc/Hz | At 1 kHz offset |
| | | -126 | | dBc/Hz | At 10 kHz offset |
| | | -134 | | dBc/Hz | At 100 kHz offset |
| | | -141 | | dBc/Hz | At 1 MHz offset |
| | | -146 | | dBc/Hz | At 10 MHz offset |
| CLK-TO-CMOS ABSOLUTE PHASE NOISE 200 MHz | | -100 | | dBc/Hz | Input slew rate > 1 V/ns At 10 Hz offset |
| | | -117 | | dBc/Hz | At 100 Hz offset |
| | | -128 | | dBc/Hz | At 1 kHz offset |
| | | -138 | | dBc/Hz | At 10 kHz offset |
| | | -147 | | dBc/Hz | At 100 kHz offset |
| | | -153 | | dBc/Hz | At 1 MHz offset |
| | | -156 | | dBc/Hz | At 10 MHz offset |

LOGIC AND POWER CHARACTERISTICS

Table 4. Control Pin Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|--|--------------------|----------------------|-----|------|-------|---|
| CONTROL PINS (CTRL_A, CTRL_B, SLEEP) ¹ | | | | | | |
| Logic 1 Voltage | V _{IH} | V _S - 0.4 | | | V | |
| Logic 0 Voltage | V _{IL} | | | 0.4 | V | |
| Logic 1 Current | I _{IH} | 5 | 8 | 20 | μA | |
| Logic 0 Current | I _{IL} | -5 | | +5 | μA | |
| Capacitance | | | 2 | | pF | |
| POWER | | | | | | |
| Supply Voltage Requirement | V _S | 1.71 | 1.8 | 1.89 | V | V _S = 1.8 V ± 5% |
| LVDS Outputs, Full Operation | | | | | | |
| LVDS at 100 MHz | | | 55 | 70 | mA | All outputs enabled as LVDS and loaded, R _L = 100 Ω |
| LVDS at 1200 MHz | | | 110 | 130 | mA | All outputs enabled as LVDS and loaded, R _L = 100 Ω |
| CMOS Outputs, Full Operation | | | | | | |
| CMOS at 100 MHz | | | 75 | 95 | mA | All outputs enabled as CMOS and loaded, CMOS load = 10 pF |
| CMOS at 250 MHz | | | 155 | 190 | mA | All outputs enabled as CMOS and loaded, CMOS load = 10 pF |
| Sleep | | | | 3 | mA | SLEEP pin pulled high; does not include power dissipated in external resistors |
| Power Supply Rejection ² | | | | | | |
| LVDS | PSR _{TPD} | | 0.9 | | ps/mV | |
| CMOS | PSR _{TPD} | | 1.2 | | ps/mV | |

¹ These pins each have a 200 kΩ internal pull-down resistor.

² Change in T_{PD} per change in V_S.

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|---|-----------------|
| Supply Voltage V _S to GND | 2 V |
| Inputs CLK and $\overline{\text{CLK}}$ | -0.3 V to +2 V |
| CMOS Inputs | -0.3 V to +2 V |
| Outputs Maximum Voltage | -0.3 V to +2 V |
| Voltage Reference Voltage (V _{REF}) | -0.3 V to +2 V |
| Operating Temperature Range Ambient | -40°C to +85°C |
| Junction | 150°C |
| Storage Temperature Range | -65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DETERMINING JUNCTION TEMPERATURE

To determine the junction temperature on the application PCB, use the following formula:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:

T_J is the junction temperature (°C).

T_{CASE} is the case temperature (°C) measured by the customer at top center of the package.

Ψ_{JT} is indicated in Table 6.

PD is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JB} are provided for package comparison and PCB design considerations.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL PERFORMANCE

Table 6.

| Parameter | Symbol | Description | Value ¹ | Unit |
|---|----------------|--------------------------------|--------------------|------|
| Junction-to-Ambient Thermal Resistance Still Air 0.0 m/sec Airflow | θ_{JA} | Per JEDEC JESD51-2 | 57.0 | °C/W |
| Moving Air 1.0 m/sec Airflow | θ_{JMA} | Per JEDEC JESD51-6 | 49.8 | °C/W |
| 2.5 m/sec Airflow | | | 44.7 | °C/W |
| Junction-to-Board Thermal Resistance Moving Air 1.0 m/sec Airflow | θ_{JB} | Per JEDEC JESD51-8 | 35.2 | °C/W |
| Junction-to-Case Thermal Resistance Moving Air Die-to-Heat Sink | θ_{JC} | Per MIL-STD 883, Method 1012.1 | 2.0 | °C/W |
| Junction-to-Top-of-Package Characterization Parameter Still Air 0 m/sec Airflow | Ψ_{JT} | Per JEDEC JESD51-2 | 1.0 | °C/W |

¹ Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

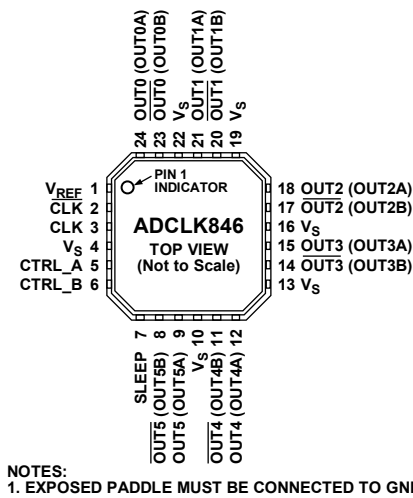


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|-----------------------|---------------------------|--|
| 1 | V_{REF} | Reference Voltage. |
| 2 | \overline{CLK} | Clock Input (Negative). |
| 3 | CLK | Clock Input (Positive). |
| 4, 10, 13, 16, 19, 22 | V_S | Supply Voltage. |
| 5 | CTRL_A | CMOS Input Control for Output 1 to Output 0. (0: LVDS, 1: CMOS.) |
| 6 | CTRL_B | CMOS Input Control for Output 5 to Output 2. (0: LVDS, 1: CMOS.) |
| 7 | SLEEP | CMOS Input for Sleep Mode. (0: normal operation, 1: sleep.) |
| 8 | $\overline{OUT5}$ (OUT5B) | Complementary Side of Differential LVDS Output 5, or CMOS Output 5 on Channel B. |
| 9 | OUT5 (OUT5A) | True Side of Differential LVDS Output 5, or CMOS Output 5 on Channel A. |
| 11 | $\overline{OUT4}$ (OUT4B) | Complementary Side of Differential LVDS Output 4, or CMOS Output 4 on Channel B. |
| 12 | OUT4 (OUT4A) | True Side of Differential LVDS Output 4, or CMOS Output 4 on Channel A. |
| 14 | $\overline{OUT3}$ (OUT3B) | Complementary Side of Differential LVDS Output 3, or CMOS Output 3 on Channel B. |
| 15 | OUT3 (OUT3A) | True Side of Differential LVDS Output 3, or CMOS Output 3 on Channel A. |
| 17 | $\overline{OUT2}$ (OUT2B) | Complementary Side of Differential LVDS Output 2, or CMOS Output 2 on Channel B. |
| 18 | OUT2 (OUT2A) | True Side of Differential LVDS Output 2, or CMOS Output 2 on Channel A. |
| 20 | $\overline{OUT1}$ (OUT1B) | Complementary Side of Differential LVDS Output 1, or CMOS Output 1 on Channel B. |
| 21 | OUT1 (OUT1A) | True Side of Differential LVDS Output 1, or CMOS Output 1 on Channel A. |
| 23 | $\overline{OUT0}$ (OUT0B) | Complementary Side of Differential LVDS Output 0, or CMOS Output 0 on Channel B. |
| 24 | OUT0 (OUT0A) | True Side of Differential LVDS Output 0, or CMOS Output 0 on Channel A. |
| (25) | EPAD | Exposed Paddle. The exposed paddle must be connected to ground. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 1.8\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

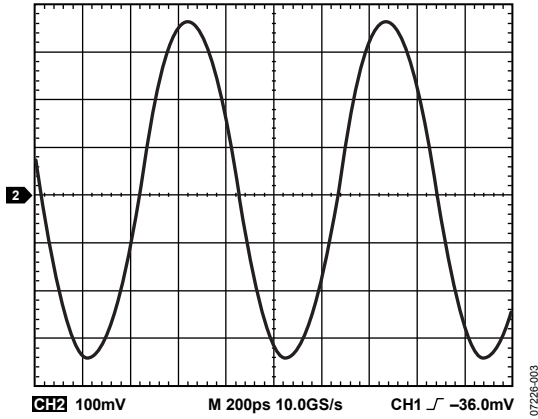


Figure 3. LVDS Output Waveform at 1200 MHz

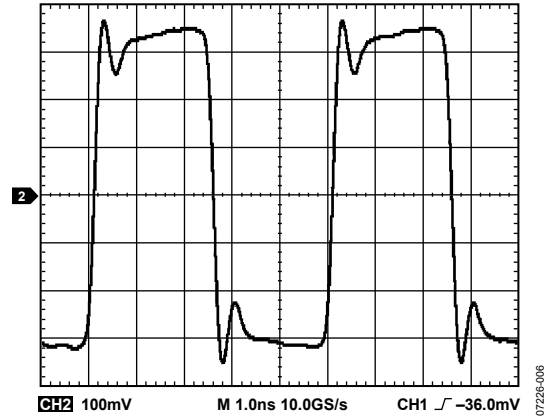


Figure 6. LVDS Output Waveform at 200 MHz

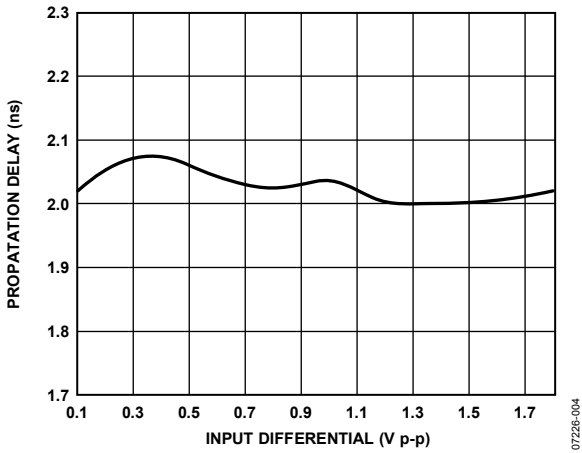


Figure 4. LVDS Propagation Delay vs. V_{ID}

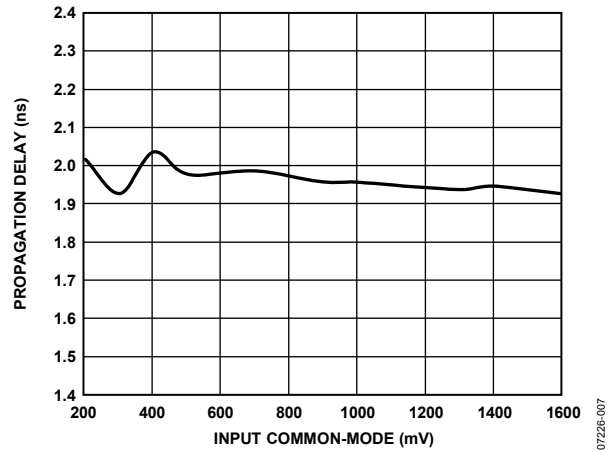


Figure 7. LVDS Propagation Delay vs. V_{CM}

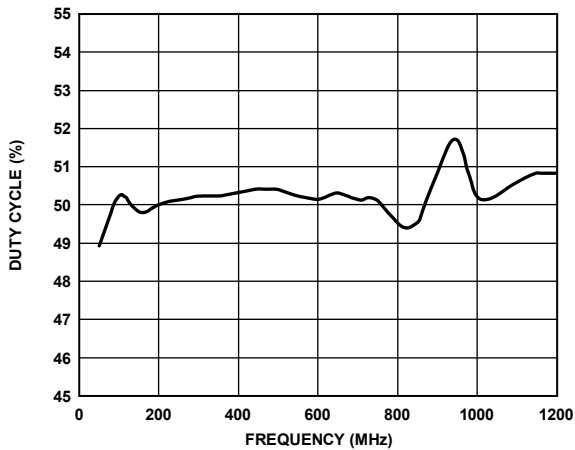


Figure 5. LVDS Output Duty Cycle vs. Frequency

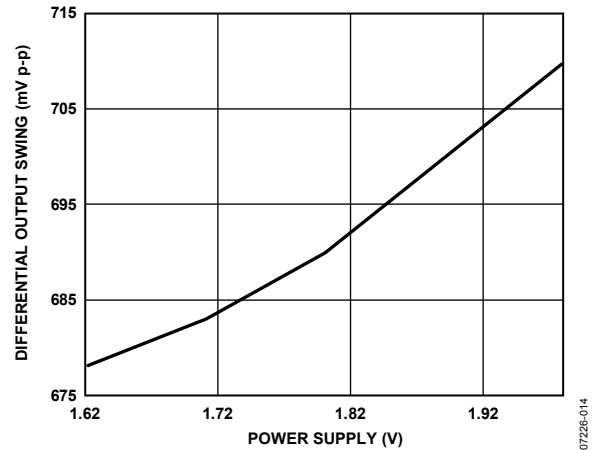


Figure 8. LVDS Output Swing vs. Power Supply Voltage

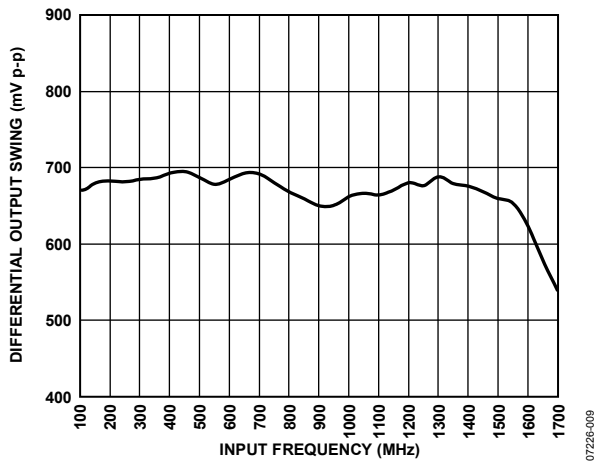


Figure 9. LVDS Differential Output Swing vs. Input Frequency

07226-009

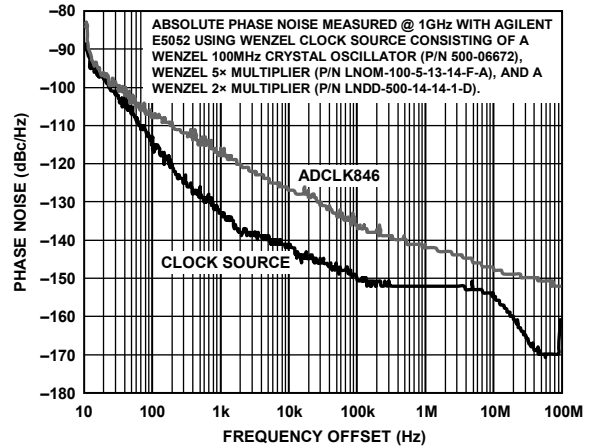


Figure 12. Absolute Phase Noise LVDS at 1000 MHz

07226-112

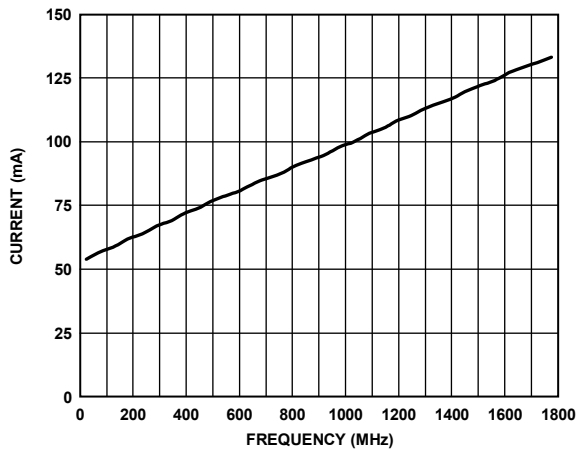


Figure 10. LVDS Current vs. Frequency, All Banks Set to LVDS

07226-110

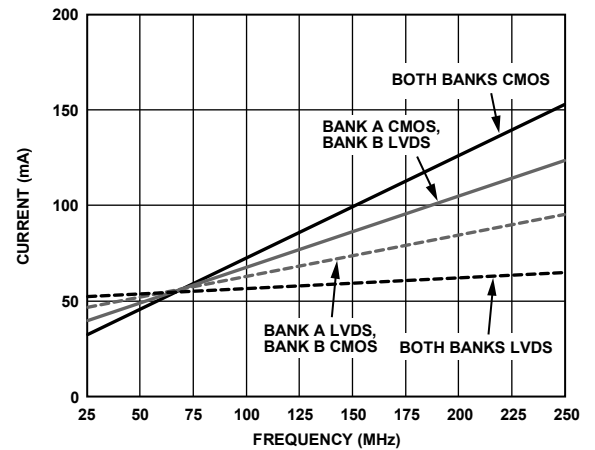


Figure 13. LVDS/CMOS Current vs. Frequency with Various Logic Combinations

07226-113

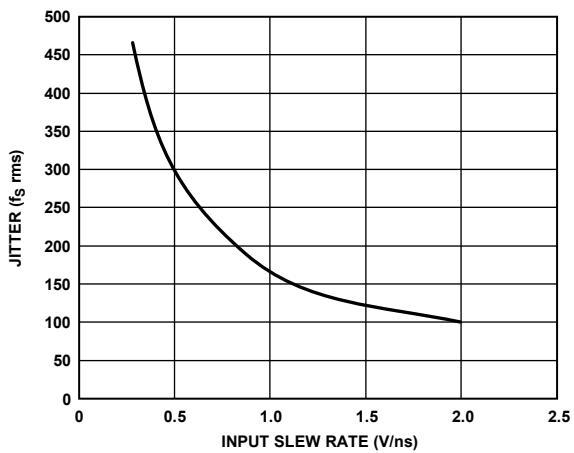


Figure 11. Additive Broadband Jitter vs. Input Slew Rate

07226-011

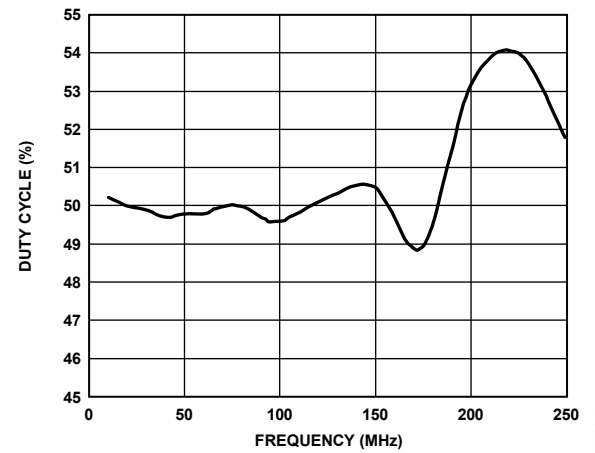


Figure 14. CMOS Output Duty Cycle vs. Frequency, 10 pF Load

07226-114

ADCLK846

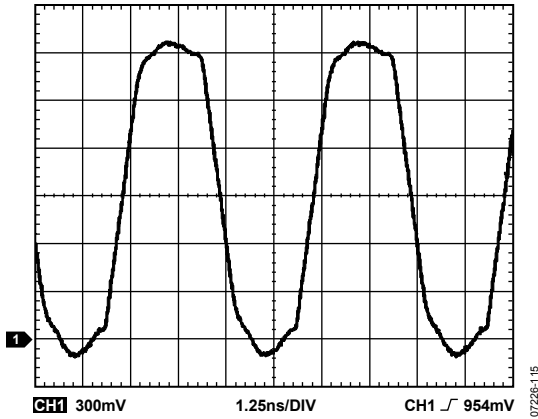


Figure 15. CMOS Output Waveform at 200 MHz, 10 pF Load

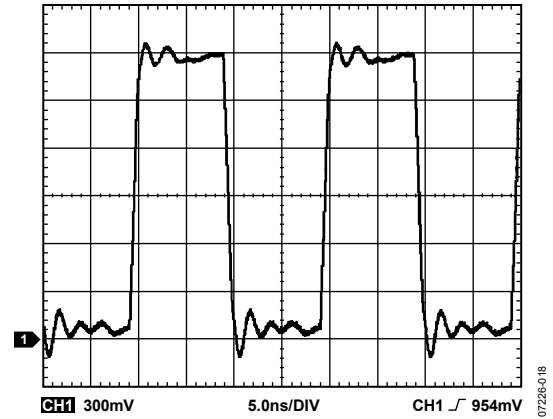


Figure 18. CMOS Output Waveform at 50 MHz, 10 pF Load

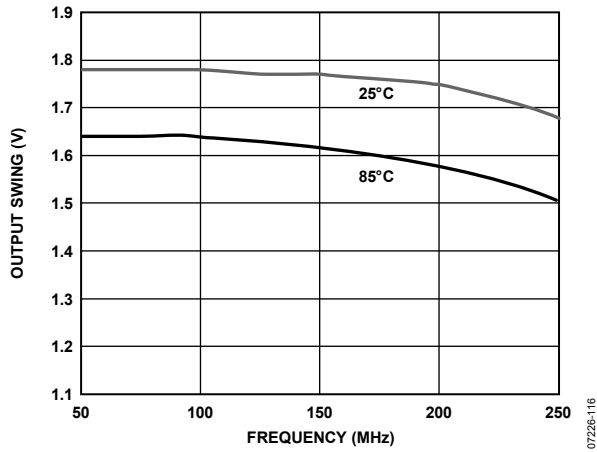


Figure 16. CMOS Output Swing vs. Frequency and Temperature, 10 pF Load

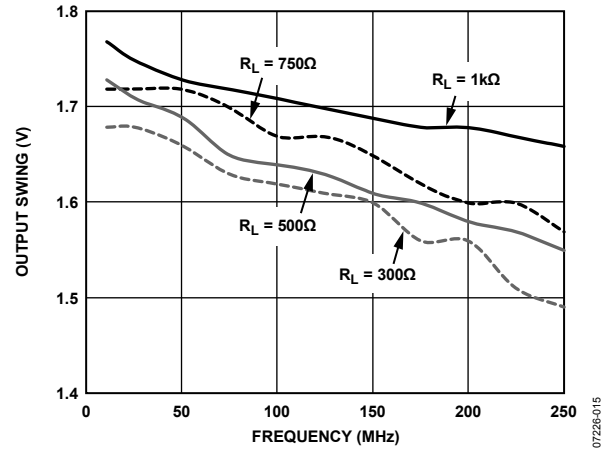


Figure 19. CMOS Output Swing vs. Frequency and Resistive Load

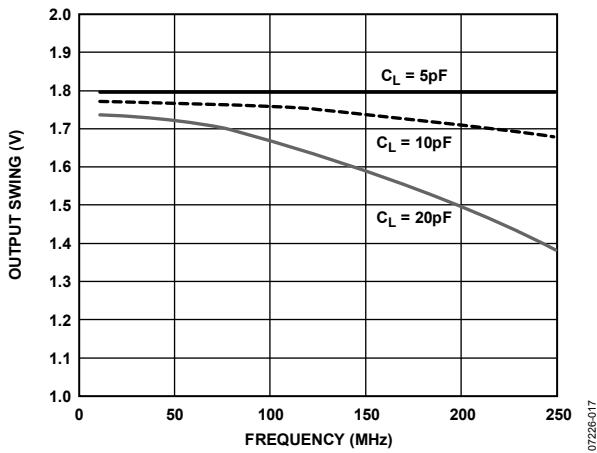


Figure 17. CMOS Output Swing vs. Frequency and Capacitive Load

FUNCTIONAL DESCRIPTION

The ADCLK846 clock input is distributed to all output channels. Each channel bank is pin programmable for either LVDS or CMOS levels. This allows the selection of multiple logic configurations ranging from 6 LVDS to 12 CMOS outputs, along with other combinations using both types of logic.

CLOCK INPUTS

The differential inputs of the ADCLK846 are internally self-biased. The clock inputs have a resistor divider, which sets the common-mode level for the inputs. The complementary inputs are biased about 30 mV lower than the true input to avoid oscillations if the input signal ceases. See Figure 20 for the equivalent input circuit.

The inputs can be ac-coupled or dc-coupled. Table 8 displays a guide for input logic compatibility. If a single-ended input is desired, this can be accommodated by ac or dc coupling to one side of the differential input. Bypass the other input to ground by a capacitor.

Note that jitter performance degrades with low input slew rate, as shown in Figure 11. See Figure 28 through Figure 32 for different termination schemes.

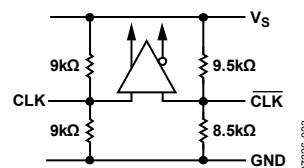


Figure 20. ADCLK846 Input Stage

AC-COUPLED APPLICATIONS

When ac coupling is desired, the ADCLK846 offers two options. The first option requires no external components (excluding the dc blocking capacitor); it allows the user to couple the reference signal onto the clock input pins (see Figure 31).

The second option allows the use of the V_{REF} pin to set the dc bias level for the ADCLK846. The V_{REF} pin can be connected to CLK and \overline{CLK} through resistors. This method allows lower impedance termination of signals at the ADCLK846 (see Figure 32).

The internal bias resistors are still in parallel with the external biasing. However, the relatively high impedance of the internal resistors allows the external termination to V_{REF} to dominate. This is also useful if it is not desirable to offset the inputs slightly as previously mentioned using only the internal biasing.

Table 8. Input Logic Compatibility

| Supply (V) | Logic | Common Mode (V) | Output Swing (V) | AC-Coupled | DC-Coupled |
|------------|--------|-----------------|------------------|-------------|-------------|
| 3.3 | CML | 2.9 | 0.8 | Yes | Not allowed |
| 2.5 | CML | 2.1 | 0.8 | Yes | Not allowed |
| 1.8 | CML | 1.4 | 0.8 | Yes | Yes |
| 3.3 | CMOS | 1.65 | 3.3 | Not allowed | Not allowed |
| 2.5 | CMOS | 1.25 | 2.5 | Not allowed | Not allowed |
| 1.8 | CMOS | 0.9 | 1.8 | Yes | Yes |
| 1.5 | HSTL | 0.75 | 0.75 | Yes | Yes |
| | LVDS | 1.25 | 0.4 | Yes | Yes |
| 3.3 | LVPECL | 2.0 | 0.8 | Yes | Not allowed |
| 2.5 | LVPECL | 1.2 | 0.8 | Yes | Yes |
| 1.8 | LVPECL | 0.5 | 0.8 | Yes | Yes |

ADCLK846

CLOCK OUTPUTS

Each driver consists of a differential LVDS output or two single-ended CMOS outputs (always in phase). When the LVDS driver is enabled, the corresponding CMOS driver is in tristate. When the CMOS driver is enabled, the corresponding LVDS driver is powered down and tristated. Figure 21 and Figure 22 display the equivalent output stage.

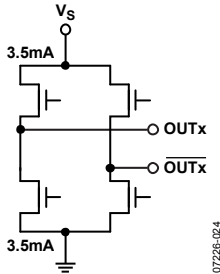


Figure 21. LVDS Output Simplified Equivalent Circuit

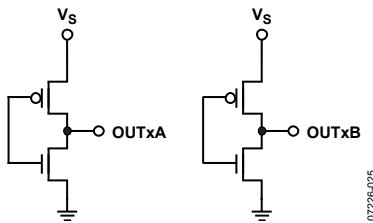


Figure 22. CMOS Equivalent Output Circuit

CONTROL AND FUNCTION PINS

Logic Select for CTRL_A

CTRL_A selects either CMOS (high) or LVDS (low) logic for Output 1 and Output 0. This pin has an internal 200 k Ω pull-down resistor.

Logic Select for CTRL_B

CTRL_B selects either CMOS (high) or LVDS (low) logic for Output 5, Output 4, Output 3, and Output 2. This pin has an internal 200 k Ω pull-down resistor.

Sleep Mode

SLEEP powers down the chip except for the band gap. The input is active high, which puts the outputs into a high-Z state. This pin has a 200 k Ω pull-down resistor. The control pins are operational during sleep mode.

POWER SUPPLY

The ADCLK846 requires a 1.8 V \pm 5% power supply for V_s. Best practice recommends bypassing the power supply on the PCB with adequate capacitance (>10 μ F) and bypassing all power pins with adequate capacitance (0.1 μ F) as close to the part as possible. The layout of the ADCLK846 evaluation board (ADCLK846/PCBZ) provides a good layout example.

Exposed Metal Paddle

The exposed metal paddle on the ADCLK846 package is an electrical connection, as well as a thermal enhancement. For the device to function properly, the paddle must be properly attached to ground (GND). The ADCLK846 dissipates heat through its exposed paddle. The PCB acts as a heat sink for the ADCLK846. The PCB attachment must provide a good thermal path to a larger heat dissipation area, such as the ground plane on the PCB. This requires a grid of vias from the top layer down to the ground plane. See Figure 23 for an example.

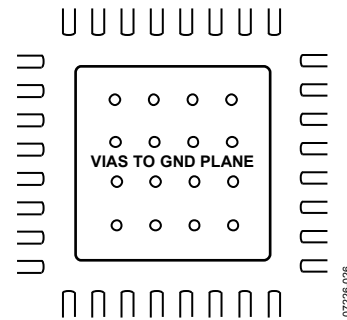


Figure 23. PCB Land Example for Attaching Exposed Paddle

APPLICATIONS INFORMATION

USING THE ADCLK846 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed analog-to-digital converter (ADC) is extremely sensitive to the quality of the sampling clock provided by the user. An ADC can be thought of as a sampling mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the ADC output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥ 14 -bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution where the step size and quantization error can be ignored, the available SNR can be expressed approximately by

$$SNR = 20 \log \left[\frac{1}{2\pi f_A T_j} \right]$$

where:

f_A is the highest analog frequency being digitized.

T_j is the rms jitter on the sampling clock.

Figure 24 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB). See AN-756 Application Note and AN-501 Application Note for more information.

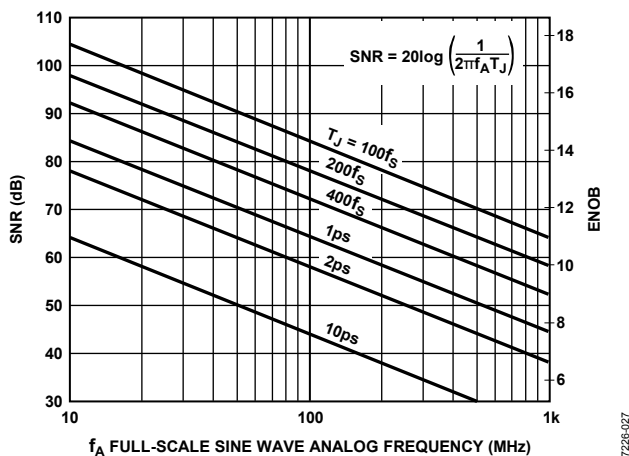


Figure 24. SNR and ENOB vs. Analog Input Frequency

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sample clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment. The ADCLK846 features LVDS outputs that provide differential clock outputs, which enable clock solutions that maximize converter SNR performance. Consider the input requirements of the ADC (differential or single-ended, logic level, termination) when selecting the best clocking/converter solution.

LVDS CLOCK DISTRIBUTION

The ADCLK846 provides clock outputs that are selectable as either CMOS or LVDS level outputs. LVDS is a differential output option that uses a current-mode output stage. The nominal current is 3.5 mA, which yields 350 mV output swing across a 100 Ω resistor. The LVDS output meets or exceeds all ANSI/TIA/EIA-644 specifications. A recommended termination circuit for the LVDS outputs is shown in Figure 25.

If ac coupling is necessary, place decoupling capacitors either before or after the 100 Ω termination resistor.

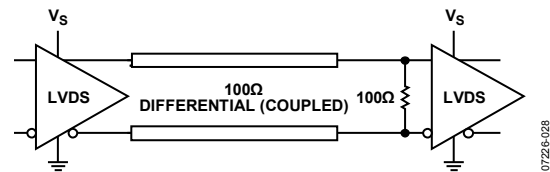


Figure 25. LVDS Output Termination

See the AN-586 Application Note at www.analog.com for more information on LVDS.

CMOS CLOCK DISTRIBUTION

The output drivers of the ADCLK846 can also be configured as CMOS drivers. When selected as a CMOS driver, each output becomes a pair of CMOS outputs. These outputs are 1.8 V CMOS compatible.

When single-ended CMOS clocking is used, some of the following guidelines outlined in this section apply.

Design point-to-point connections such that each driver has only one receiver, if possible. Connecting outputs in this manner allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the output trace. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver.

The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and signal integrity.

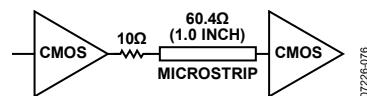


Figure 26. Series Termination of CMOS Output

ADCLK846

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the ADCLK846 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 27. Match the far-end termination network to the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

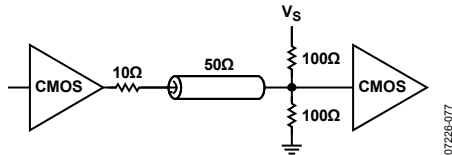


Figure 27. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The ADCLK846 offers LVDS outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

INPUT TERMINATION OPTIONS

For single-ended operation, always bypass unused input to GND as shown in Figure 31.

Figure 32 illustrates the use of the V_{REF} to provide low impedance termination into $V_s/2$. In addition, Figure 32 shows a way to negate the 30 mV input offset with external resistor values. For example, use 1.8 V CMOS with long traces to provide far-end termination.

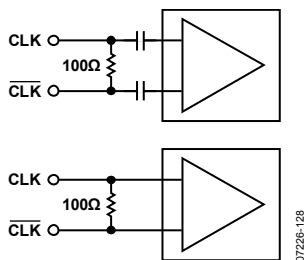


Figure 28. Typical AC-Coupled or DC-Coupled LVDS or HSTL Configurations (see Table 8)

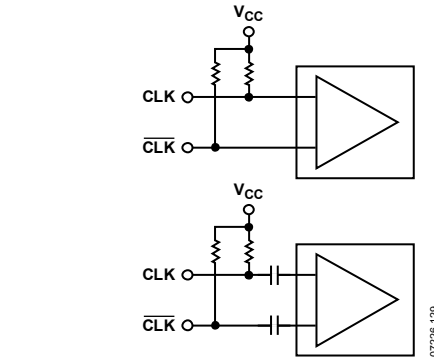


Figure 29. Typical AC-Coupled or DC-Coupled CML Configurations (see Table 8 for CML Coupling Limitations)

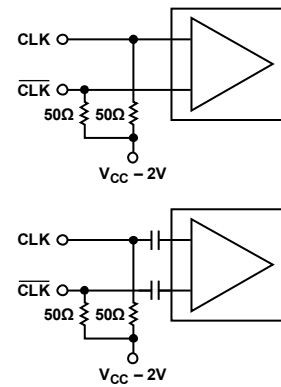


Figure 30. Typical AC-Coupled or DC-Coupled LVPECL Configurations (see Table 8 for LVPECL DC Coupling Limitations)

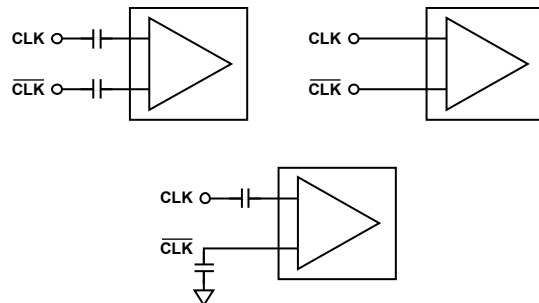


Figure 31. Typical 1.8 V CMOS Configurations for Short Trace Lengths (see Table 8 for CMOS compatibility)

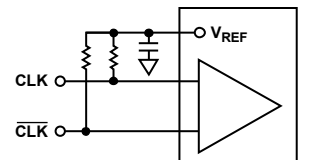
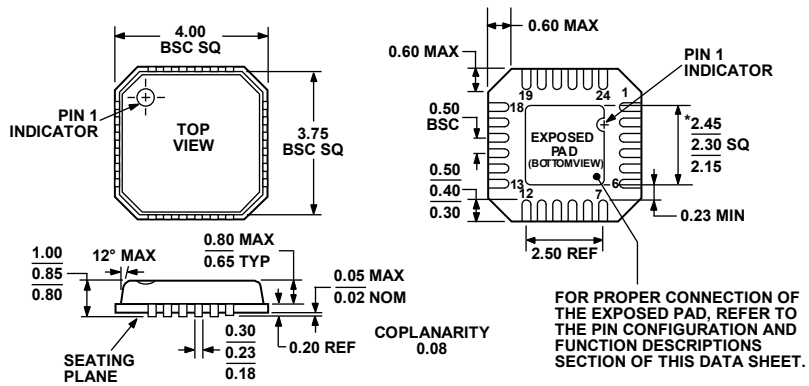


Figure 32. Use of the V_{REF} to Provide Low Impedance Termination into $V_s/2$

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2 EXCEPT FOR EXPOSED PAD DIMENSION

Figure 33. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 4 mm × 4 mm Body, Very Thin Quad
 CP-24-2
 Dimensions shown in millimeters

060808-A

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------------------------|-------------------|---------------------|----------------|
| ADCLK846BCPZ ¹ | -40°C to +85°C | 24-Lead LFCSP_VQ | CP-24-2 |
| ADCLK846BCPZ-REEL7 ¹ | -40°C to +85°C | 24-Lead LFCSP_VQ | CP-24-2 |
| ADCLK846/PCBZ ¹ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

ADCLK846

NOTES