ELPIDA

512M bits DDR2 SDRAM
for HYPER DIMM

EDE5108ABSE-BE, -AE (64M words × 8 bits)

Description

The EDE5108AB is a 512M bits DDR2 SDRAM organized as 16,777,216 words × 8 bits × 4 banks.
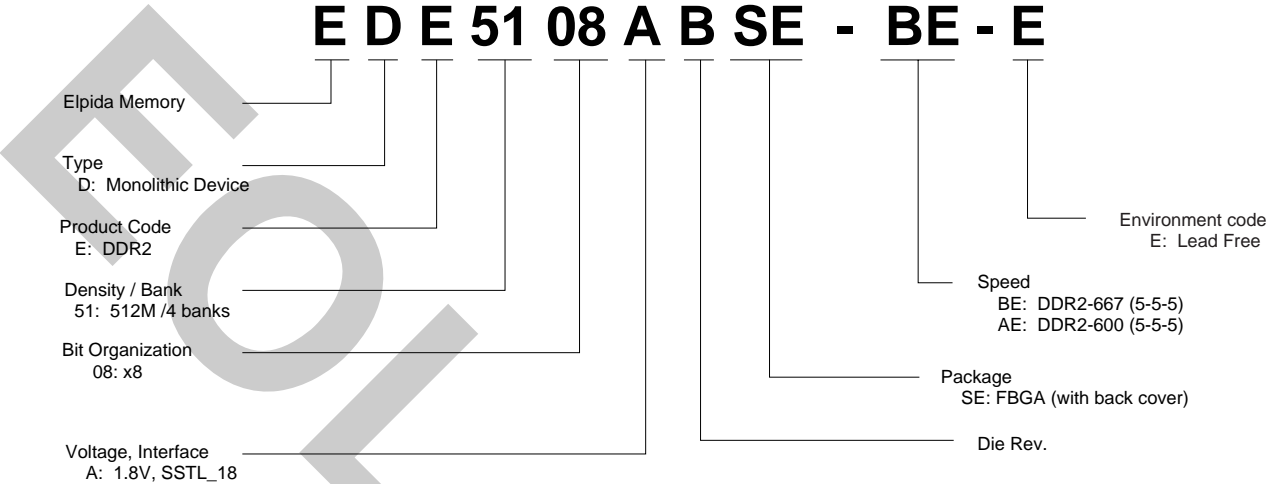It is packaged in 64-ball FBGA package.

Features

- 1.8V power supply
- Double-data-rate architecture: two data transfers per clock cycle
- Bi-directional, differential data strobe (DQS and /DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge aligned with data for READs: center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge: data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 4, 8
- /CAS Latency (CL): 3, 4, 5
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- 7.8μs average periodic refresh interval
- 1.8V (SSTL_18 compatible) I/O
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- Programmable RDQS, /RDQS output for making × 8 organization compatible to × 4 organization
- /DQS, (/RDQS) can be disabled for single-ended Data Strobe operation.
- FBGA package with lead free solder (Sn-Ag-Cu)

Ordering Information

Part number	Mask version	Organization (words × bits)	Internal Banks	Speed bin (CL-tRCD-tRP)	Package
EDE5108ABSE-BE-E	B	64M × 8	4	DDR2-667 (5-5-5)	64-ball FBGA
EDE5108ABSE-AE-E				DDR2-600 (5-5-5)	

Part Number

E D E 51 08 A B SE - BE - E

Elpida Memory

Type
D: Monolithic Device

Product Code
E: DDR2

Density / Bank
51: 512M /4 banks

Bit Organization
08: x8

Voltage, Interface
A: 1.8V, SSTL_18

Environment code
E: Lead Free

Speed
BE: DDR2-667 (5-5-5)
AE: DDR2-600 (5-5-5)

Package
SE: FBGA (with back cover)

Die Rev.

ELPIDA

Pin Configurations

/xxx indicates active low signal.

64-ball FBGA

	1	2	3		7	8	9
A	NC	NC				NC	NC
B							
C							
D							
E	VDD	NU/ /RDQS	VSS		VSSQ	/DQS	VDDQ
F	DQ6	VSSQ	DM/RDQS		DQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ		VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3		DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS		VSSDL	CK	VDD
K		CKE	/WE		/RAS	/CK	ODT
L	NC	BA0	BA1		/CAS	/CS	
M		A10	A1		A2	A0	VDD
N	VSS	A3	A5		A6	A4	
P		A7	A9		A11	A8	VSS
R	VDD	A12	NC		NC	A13	
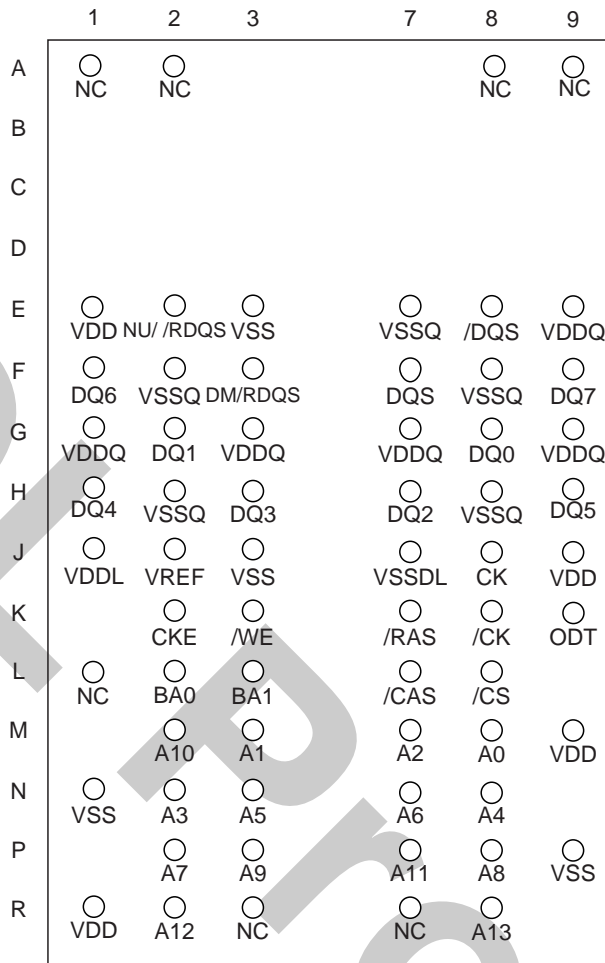
(Top view)

Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0, BA1	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ15	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
RDQS, /RDQS	Differential data strobe for read	VSSQ	Ground for DQ circuit
/CS	Chip select	VREF	Input reference voltage
/RAS, /CAS, /WE	Command input	VDDL	Supply voltage for DLL circuit
CKE	Clock enable	VSSDL	Ground for DLL circuit
CK, /CK	Differential clock input	NC*[1]	No connection
DM	Write data mask	NU*[2]	Not usable

Notes: 1. Not internally connected with die.

2. Don't use other than reserved functions.

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Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	VDD	−1.0 to +2.3	V	1
Power supply voltage for output	VDDQ	−0.5 to +2.3	V	1
Input voltage	VIN	−0.5 to +2.3	V	1
Output voltage	VOUT	−0.5 to +2.3	V	1
Storage temperature	Tstg	−55 to +100	°C	1, 2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating case temperature	TC	0 to +85	°C	1, 2

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. The operation temperature range is the temperature where all DRAM specification will be supported. Out side of this temperature range, even it is still within the limit of stress condition, some deviation on portion of operation specification may be required.

   During operation, the DRAM case temperature must be maintained between 0 to +85°C under all other specification parameters.

Recommended DC Operating Conditions (SSTL_18)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD	1.8	1.85	1.9	V	4
Supply voltage for output	VDDQ	1.8	1.85	1.9	V	4
Input reference voltage	VREF	$0.49 \times$ VDDQ	$0.50 \times$ VDDQ	$0.51 \times$ VDDQ	V	1, 2
Termination voltage	VTT	VREF − 0.04	VREF	VREF + 0.04	V	3
DC input logic high	VIH (DC)	VREF + 0.125	—	VDDQ + 0.3V	V	
DC input low	VIL (DC)	−0.3	—	VREF − 0.125	V	
AC input logic high	VIH (AC)	VREF + 0.250	—	—	V	
AC input low	VIL (AC)	—	—	VREF − 0.250	V	

Notes: 1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about $0.5 \times$ VDDQ of the transmitting device and VREF are expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed ±2% VREF (DC).
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

DC Characteristics 1 (TC = 0 to +85ºC, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	Symbol	Grade	max.	Unit	Test condition	
Operating current (ACT-PRE)	IDD0	-BE -AE	125 120	mA	one bank; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	

Operating current (ACT-READ-PRE)	IDD1	-BE
		-AE
			140
			135
				mA	one bank; IOUT = 0mA;
					BL = 4, CL = CL(IDD), AL = 0;
					tCK = tCK (IDD), tRC = tRC (IDD),
					tRAS = tRAS min.(IDD); tRCD = tRCD (IDD);
					CKE is H, /CS is H between valid commands;
					Address bus inputs are SWITCHING;
					Data pattern is same as IDD4W	

Precharge power-down standby current	IDD2P	-BE -AE	12 11	mA	all banks idle; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	
Precharge quiet standby current	IDD2Q	-BE -AE	30 25	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	
Idle standby current	IDD2N	-BE -AE	40 35	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	
Active power-down standby current	IDD3P-F	-BE -AE	45 40	mA	all banks open; tCK = tCK (IDD); CKE is L;	Fast PDN Exit MRS(12) = 0
	IDD3P-S	-BE -AE	30 25	mA	Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Slow PDN Exit MRS(12) = 1
Active standby current	IDD3N	-BE -AE	80 75	mA	all banks open; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	

Operating current (Burst read operating)	IDD4R	-BE
		-AE
			220
			210
				mA	all banks open, continuous burst reads, IOUT = 0mA;
					BL = 4, CL = CL(IDD), AL = 0;
					tCK = tCK (IDD), tRAS = tRAS max.(IDD),
					tRP = tRP (IDD);
					CKE is H, /CS is H between valid commands;
					Address bus inputs are SWITCHING;
					Data pattern is same as IDD4W	

Operating current (Burst write operating)	IDD4W	-BE -AE	220 210	mA	all banks open, continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	

Parameter	Symbol	Grade	max.	Unit	Test condition
Auto-refresh current	IDD5	-BE -AE	270 260	mA	tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Self-refresh current	IDD6		6	mA	Self Refresh Mode; CK and /CK at 0V; CKE $\leq$ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
Operating current (Bank interleaving)	IDD7	-BE -AE	340 330	mA	all bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD (IDD) −1 × tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD(IDD), tRCD = 1 × tCK (IDD); CKE is H, CS is H between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4W;

Notes: 1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Input Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, /DQS, RDQS, /RDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
   L is defined as VIN $\leq$ VIL (AC) (max.)
   H is defined as VIN $\geq$ VIH (AC) (min.)
   STABLE is defined as inputs stable at an H or L level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as:
   inputs changing between H and L every other clock cycle (once per two clocks) for address and control signals, and inputs changing between H and L every other data transfer (once per clock) for DQ signals not including masks or strobes.
6. Refer to AC Timing for IDD Test Conditions.

AC Timing for IDD Test Conditions
For purposes of IDD testing, the following parameters are to be utilized.

Parameter	DDR2-667 5-5-5	DDR2-600 5-5-5	Unit
CL(IDD)	5	5	tCK
tRCD(IDD)	15	15	ns
tRC(IDD)	60	65	ns
tRRD(IDD)	7.5	7.5	ns
tCK(IDD)	3	3.3	ns
tRAS(min.)(IDD)	45	47.5	ns
tRAS(max.)(IDD)	70000	70000	ns
tRP(IDD)	15	15	ns
tRFC(IDD)	105	105	ns

DC Characteristics 2 (TC = 0 to +85°C, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	Symbol	Value	Unit	Notes
Input leakage current	$\lvert ILI \rvert$	2	μA	VDD ≥ VIN ≥ VSS
Output leakage current	$\lvert ILO \rvert$	5	μA	VDDQ ≥ VOUT ≥ VSS
Minimum required output pull-up under AC test load	VOH	VTT + 0.603	V	5
Maximum required output pull-down under AC test load	VOL	VTT − 0.603	V	5
Output timing measurement reference level	VOTR	$0.5 \times VDDQ$	V	1
Output minimum sink DC current	IOL	+13.4	mA	3, 4, 5
Output minimum source DC current	IOH	−13.4	mA	2, 4, 5

Notes: 1. The VDDQ of the device under test is referenced.

2. VDDQ = 1.7V; VOUT = 1.42V.

3. VDDQ = 1.7V; VOUT = 0.28V.

4. The DC value of VREF applied to the receiving device is expected to be set to VTT.

5. After OCD calibration to 18Ω at TC = 25°C, VDD = VDDQ = 1.8V.

DC Characteristics 3 (TC = 0 to +85°C, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	Symbol	min.	max.	Unit	Note
AC differential input voltage	VID (AC)	0.5	VDDQ + 0.6	V	1, 2
AC differential cross point voltage	VIX (AC)	$0.5 \times VDDQ - 0.175$	$0.5 \times VDDQ + 0.175$	V	2
AC differential cross point voltage	VOX (AC)	$0.5 \times VDDQ - 0.125$	$0.5 \times VDDQ + 0.125$	V	3

Notes: 1. VID(AC) specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as CK, DQS) and VCP is the complementary input signal (such as /CK, /DQS). The minimum value is equal to VIH(AC) – VIL(AC).

2. The typical value of VIX(AC) is expected to be about $0.5 \times VDDQ$ of the transmitting device and VIX(AC) is expected to track variations in VDDQ . VIX(AC) indicates the voltage at which differential input signals must cross.

3. The typical value of VOX(AC) is expected to be about $0.5 \times VDDQ$ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at which differential output signals must cross.

Differential Signal Levels*[1, 2]
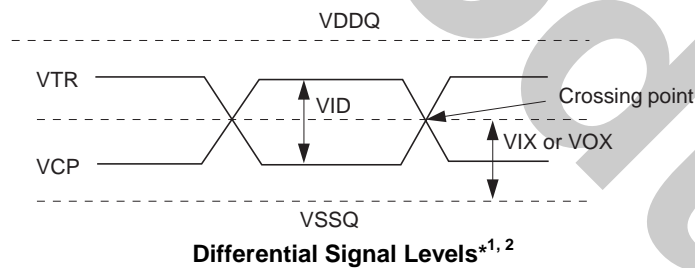
ODT DC Electrical Characteristics (TC = 0 to +85°C, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	Symbol	min	typ	max	Unit	Notes
Rtt effective impedance value for EMRS (A6, A2) = 0, 1; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1, 0; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Deviation of VM with respect to VDDQ/2	ΔVM	−3.75	—	+3.75	%	1

Note: 1. Test condition for Rtt measurements.

Measurement Definition for Rtt(eff)

Apply VIH (AC) and VIL (AC) to test pin separately, then measure current I(VIH(AC)) and I(VIL(AC)) respectively. VIH(AC), and VDDQ values defined in SSTL_18.

$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for ΔVM

Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100\%$$

OCD Default Characteristics (TC = 0 to +85°C, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	min	typ	max	Unit	Notes
Output impedance	12.6	18	23.4	Ω	1
Pull-up and pull-down mismatch	0	—	4	Ω	1, 2
Output slew rate	1.5	—	4.5	V/ns	3, 4

Notes: 1. Impedance measurement condition for output source DC current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT−VDDQ)/IOH must be less than 23.4Ω for values of VOUT between VDDQ and VDDQ−280mV. Impedance measurement condition for output sink DC current: VDDQ = 1.7V; VOUT = 280mV; VOUT/IOL must be less than 23.4Ω for values of VOUT between 0V and 280mV.

2. Mismatch is absolute value between pull up and pull down, both are measured at same temperature and voltage.

3. Slew rate measured from VIL(AC) to VIH(AC).

4. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

Pin Capacitance (TA = 25°C, VDD, VDDQ = 1.85V ± 0.05V)

Parameter	Symbol	Pins	min.	max.	Unit	Notes
CLK input pin capacitance	CCK	CK, /CK	1.0	2.0	pF	1
Input pin capacitance	CIN	/RAS, /CAS, /WE, /CS, CKE, ODT, Address	1.0	2.0	pF	1
Input/output pin capacitance	CI/O	DQ, DQS, /DQS, RDQS, /RDQS, DM	3.0	4.0	pF	2

Notes: 1. Matching within 0.25pF.
　　　 2. Matching within 0.50pF.

AC Characteristics (TC = 0 to +85°C, VDD, VDDQ = 1.85V ± 0.05V, VSS, VSSQ = 0V)

Parameter	Symbol	-BE 667 min.	-BE 667 max.	-AE 600 min.	-AE 600 max.	Unit	Notes
/CAS latency	CL	5	5	5	5	tCK	
Active to read or write command delay	tRCD	15	—	15	—	ns	
Precharge command period	tRP	15	—	15	—	ns	
Active to active/auto refresh command time	tRC	55	—	55	—	ns	
DQ output access time from CK, /CK	tAC	−450	+450	−500	+500	ps	
DQS output access time from CK, /CK	tDQSCK	−400	+400	−450	+450	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min. (tCL, tCH)	—	min. (tCL, tCH)	—	ps	
Clock cycle time	tCK	3000	8000	3300	8000	ps	
DQ and DM input hold time	tDH	225	—	225	—	ps	5
DQ and DM input setup time	tDS	100	—	100	—	ps	4
Control and Address input pulse width for each input	tIPW	0.6	—	0.6	—	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	—	0.35	—	tCK	
Data-out high-impedance time from CK,/CK	tHZ	—	tAC max.	—	tAC max.	ps	
Data-out low-impedance time from CK,/CK	tLZ	tAC min.	tAC max.	tAC min.	tAC max.	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	—	300	—	300	ps	
DQ hold skew factor	tQHS	—	400	—	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	tHP – tQHS	—	ps	
Write command to first DQS latching transition	tDQSS	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	tCK	
Mode register set command cycle time	tMRD	2	—	2	—	tCK	
Write preamble setup time	tWPRES	0	—	0	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	—	0.35	—	tCK	
Address and control input hold time	tIH	250	—	375	—	ps	5
Address and control input setup time	tIS	125	—	250	—	ps	4
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to precharge command	tRAS	40	70000	40	70000	ns	
Active to auto-precharge delay	tRAP	tRCD min.	—	tRCD min.	—	ns	

Frequency (Mbps)		-BE		-AE			
		667		600			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Active bank A to active bank B command period	tRRD	7.5	—	7.5	—	ns	
Write recovery time	tWR	15	—	15	—	ns	
Auto precharge write recovery + precharge time	tDAL	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	tCK	1
Internal write to read command delay	tWTR	7.5	—	7.5	—	ns	
Internal read to precharge command delay	tRTP	7.5	—	7.5	—	ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10	—	tRFC + 10	—	ns	
Exit self refresh to a read command	tXSRD	200	—	200	—	tCK	
Exit precharge power down to any non-read command	tXP	2	—	2	—	tCK	
Exit active power down to read command	tXARD	2	—	2	—	tCK	3
Exit active power down to read command (slow exit/low power mode)	tXARDS	6 − AL	—	6 − AL	—	tCK	2, 3
CKE minimum pulse width (high and low pulse width)	tCKE	3	—	3	—	tCK	
Output impedance test driver delay	tOIT	0	12	0	12	ns	
Auto refresh to active/auto refresh command time	tRFC	105	—	105	—	ns	
Average periodic refresh interval	tREFI	—	7.8	—	7.8	µs	
Minimum time clocks remains ON after CKE asynchronously drops low	tDELAY	tIS + tCK + tIH	—	tIS + tCK + tIH	—	ns	

Notes: 1. For each of the terms above, if not already an integer, round to the next higher integer.

2. AL: Additive Latency.

3. MRS A12 bit defines which active power down exit timing to be applied.

4. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIH(AC) level for a rising signal and VIL(AC) for a falling signal applied to the device under test.

5. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIH(DC) level for a rising signal and VIL(DC) for a falling signal applied to the device under test.
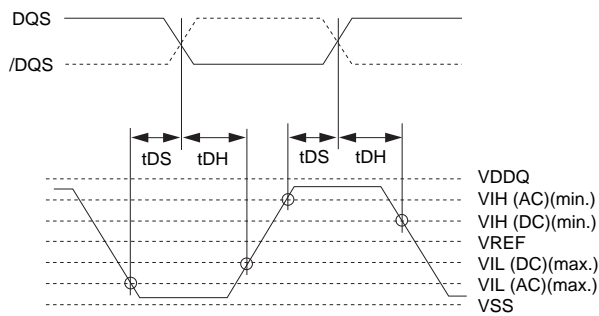
Input Waveform Timing 1 (tDS, tDH)
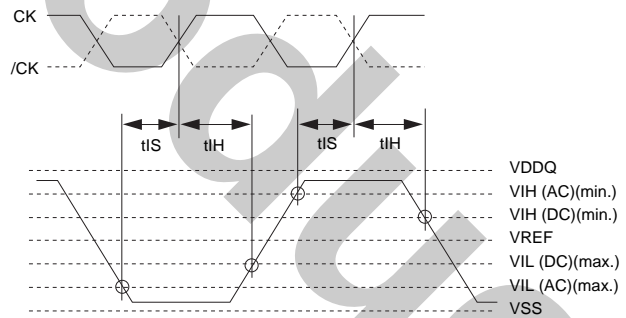
Input Waveform Timing 2 (tIS, tIH)

ODT AC Electrical Characteristics

Parameter	Symbol	min	max	Unit	Notes
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) + 1000	ps	1
ODT turn-on (power down mode)	tAONPD	tAC(min) + 2000	2tCK + tAC(max) + 1000	ps	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max) + 600	ps	2
ODT turn-off (power down mode)	tAOFPD	tAC(min) + 2000	2.5tCK + tAC(max) + 1000	ns	
ODT to power down entry latency	tANPD	3	3	tCK	
ODT power down exit latency	tAXPD	8	8	tCK	

Notes: 1. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.
2. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

AC Input Test Conditions

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	$0.5 \times$ VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(max.)	1.0	V	1
Input signal maximum slew rate	SLEW	1.0	V/ns	2, 3

Notes: 1. Input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VIL(DC) (max.) to VIH(AC) (min.) for rising edges and the range from VIH(DC) (min.) to VIL(AC) (max.) for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.

Start of falling edge input timing   Start of rising edge input timing

VDDQ
VIH (AC)(min.)
VIH (DC)(min.)
VREF
VIL (DC)(max.)
VIL (AC)(max.)
VSS

VSWING(max.)

ΔTF ΔTR

$$\text{Falling slew} = \frac{\text{VIH (DC)(min.)} - \text{VIL (AC)(max.)}}{\Delta\text{TF}}$$

$$\text{Rising slew} = \frac{\text{VIH (AC) min.} - \text{VIL (DC)(max.)}}{\Delta\text{TR}}$$
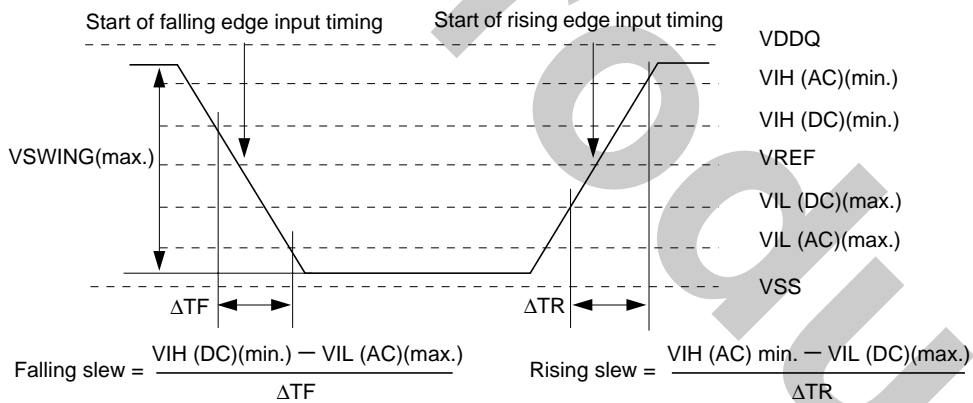
AC Input Test Signal Wave forms

Measurement point

DQ ○———W———● VTT

RT = 25 Ω

Output Load

Block Diagram

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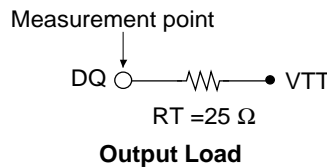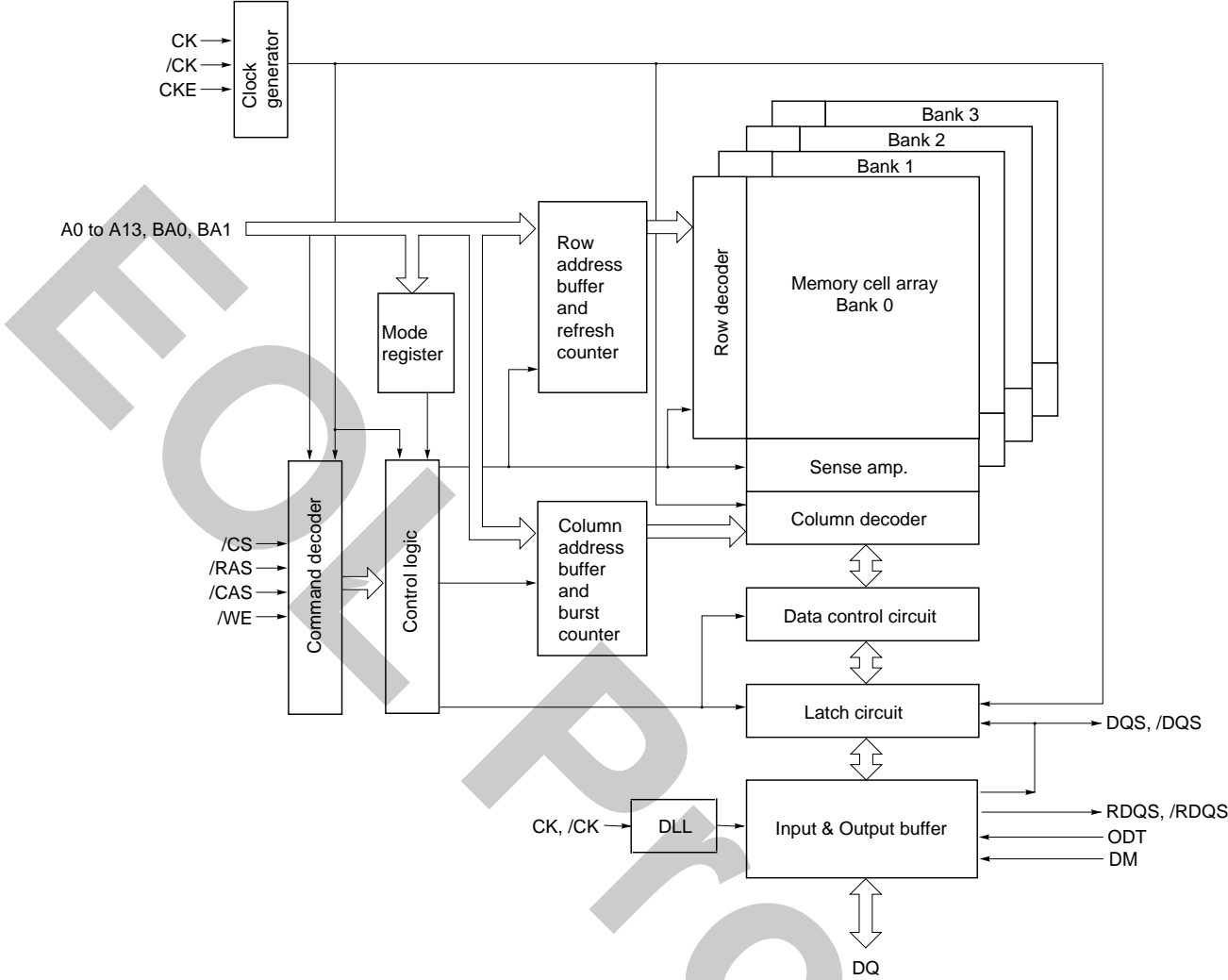
Pin Function

CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pin)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

/RAS, /CAS, /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A13 (input pins)

Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during mode register set commands.

[Address Pins Table]

Part number	Address (A0 to A13)		Note
	Row address	Column address	
EDE5108AB	AX0 to AX13	AY0 to AY9	

A10 (AP) (input pin)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by BA0, BA1.

BA0, BA1 (input pins)

BA0 and BA1 define to which bank an active, read, write or precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and Self Refresh operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

DM (input pins)

DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For ×8 configuration, DM function will be disabled when RDQS function is enabled by EMRS.

DQ (input/output pins)

Bi-directional data bus.

DQS, /DQS (input/output pins)

Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, centered in write data. Used to capture write data. /DQS can be disabled by EMRS.

RDQS, /RDQS (output pins)

Differential Data Strobe for READ operation only. DM and RDQS functions are switch able by EMRS. These pins exist only in ×8 configuration. /RDQS output will be disabled when /DQS is disabled by EMRS**.**

ODT (input pins)

ODT (On Die Termination control) is a registered high signal that enables termination resistance internal to the DDR II SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for × 8 configurations. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

VDD, VSS, VDDQ, VSSQ (power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

VDDL and VSSDL (power supply)

VDDL and VSSDL are power supply pins for DLL circuits.

VREF (Power supply)

SSTL_18 reference voltage: $(0.50 \pm 0.01) \times$ VDDQ

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Command Operation

Command Truth Table

The DDR2 SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Function	Symbol	CKE Previous cycle	CKE Current cycle	/CS	/RAS	/CAS	/WE	BA1, BA0	A13 to A11	A10	A0 to A9	Notes
Mode register set	MRS	H	H	L	L	L	L	BA0 = 0 and MRS OP Code				1
Extended mode register set	EMRS	H	H	L	L	L	L	BA0 = 1 and EMRS OP Code				1
Auto refresh	REF	H	H	L	L	L	H	×	×	×	×	1
Self refresh entry	SELF	H	L	L	L	L	H	×	×	×	×	1
Self refresh exit	SELFX	L	H	H	×	×	×	×	×	×	×	1, 6
		L	H	L	H	H	H	×	×	×	×	
Single bank precharge	PRE	H	H	L	L	H	L	BA	×	L	×	1, 2
Precharge all banks	PALL	H	H	L	L	H	L	×	×	H	×	1
Bank activate	ACT	H	H	L	L	H	H	BA	Row Address			1, 2
Write	WRIT	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with auto precharge	WRITA	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	READ	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with auto precharge	READA	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No operation	NOP	H	×	L	H	H	H	×	×	×	×	1
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×	1
Power down mode entry	PDEN	H	L	H	×	×	×	×	×	×	×	1, 4
		H	L	L	H	H	H	×	×	×	×	
Power down mode exit	PDEX	L	H	H	×	×	×	×	×	×	×	1, 4
		L	H	L	H	H	H	×	×	×	×	

Remark: H = VIH. L = VIL. × = VIH or VIL

Notes: 1. All DDR2 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock.

2. Bank select (BA0, BA1), determine which bank is to be operated upon.

3. Burst reads or writes should not be terminated other than specified as ″Reads interrupted by a Read″ in burst read command [READ] or ″Writes interrupted by a Write″ in burst write command [WRIT].

4. The power down mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements of the device. One clock delay is required for mode entry and exit.

5. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.

6. Self refresh exit is asynchronous.

CKE Truth Table

Current state*2	CKE Previous cycle (n-1)*1	CKE Current cycle (n)*1	Command(n)*3 /CS, /RAS, /CAS, /WE	Operation (n)*3	Notes
Power down	L	L	×	Maintain power down	11, 13, 15
	L	H	DESL or NOP	Power down exit	4, 8, 11, 13
Self refresh	L	L	×	Maintain self refresh	11, 15
	L	H	DESL or NOP	Self refresh exit	4, 5, 9
Bank Active	H	L	DESL or NOP	Active power down entry	4, 8, 10, 11, 13
All banks idle	H	L	DESL or NOP	Precharge power down entry	4, 8, 10, 11, 13
	H	L	SELF	Self refresh entry	6, 9, 11, 13
Any state other than listed above	H	H	Refer to the Command Truth Table		7

Remark: H = VIH. L = VIL. × = Don't care

Notes: 1. CKE (n) is the logic state of CKE at clock edge n; CKE (n−1) was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.

3. Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).

4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

5. On self refresh exit, [DESL] or [NOP] commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.

6. Self refresh mode can only be entered from the all banks idle state.

7. Must be a legal command as defined in the command truth table.

8. Valid commands for power down entry and exit are [NOP] and [DESL] only.

9. Valid commands for self refresh exit are [NOP] and [DESL] only.

10. Power down and self-refresh can not be entered while read or write operations, (extended) mode register set operations or precharge operations are in progress. See section Power Down and Self Refresh Command for a detailed list of restrictions.

11. Minimum CKE high time is 3 clocks; minimum CKE low time is 3 clocks.

12. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh. See section ODT (On Die Termination).

13. The power down does not perform any refresh operations. The duration of power down mode is therefore limited by the refresh requirements outlined in section automatic refresh command.

14. CKE must be maintained high while the SDRAM is in OCD calibration mode.

15. "×" means "don't care" (including floating around VREF) in self refresh and power down. However ODT must be driven high or low in power down if the ODT function is enabled (bit A2 or A6 set to "1" in EMRS(1)).

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Idle	H	×	×	×	×	DESL	Nop or Power down	
	L	H	H	H	×	NOP	Nop or Power down	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10 (AP)	PRE	Precharge	
	L	L	H	L	A10 (AP)	PALL	Precharge all banks	
	L	L	L	H	×	REF	Auto refresh	2
	L	L	L	H	×	SELF	Self refresh	2
	L	L	L	L	BA, MRS-OPCODE	MRS	Mode register accessing	2
	L	L	L	L	BA, EMRS-OPCODE	EMRS	Extended mode register accessing	2
Bank(s) active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	L	H	BA, CA, A10 (AP)	READ	Begin Read	
	L	H	L	H	BA, CA, A10 (AP)	READA	Begin Read	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	Begin Write	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	Begin Write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	Precharge	
	L	L	H	L	A10 (AP)	PALL	Precharge all banks	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end -> Row active	
	L	H	H	H	×	NOP	Continue burst to end -> Row active	
	L	H	L	H	BA, CA, A10 (AP)	READ	Burst interrupt	1, 4
	L	H	L	H	BA, CA, A10 (AP)	READA	Burst interrupt	1, 4
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

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Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Write	H	×	×	×	×	DESL	Continue burst to end -> Write recovering	
	L	H	H	H	×	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	Burst interrupt	1, 4
	L	H	L	L	BA, CA, A10 (AP)	WRITA	Burst interrupt	1, 4
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end -> Precharging	
	L	H	H	H	×	NOP	Continue burst to end -> Precharging	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Write with auto Precharge	H	×	×	×	×	DESL	Continue burst to end ->Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end ->Write recovering with auto precharge	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Precharging	H	×	×	×	×	DESL	Nop -> Enter idle after tRP	
	L	H	H	H	×	NOP	Nop -> Enter idle after tRP	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	Nop -> Enter idle after tRP	
	L	L	H	L	A10 (AP)	PALL	Nop -> Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop -> Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop -> Enter bank active after tRCD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop -> Enter bank active after tWR	
	L	H	H	H	×	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	New write	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Write recovering with	H	×	×	×	×	DESL	Nop -> Enter bank active after tWR	
auto precharge	L	H	H	H	×	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop -> Enter idle after tRFC	
	L	H	H	H	×	NOP	Nop -> Enter idle after tRFC	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop -> Enter idle after tMRD	
	L	H	H	H	×	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Extended Mode	H	×	×	×	×	DESL	Nop -> Enter idle after tMRD	
register accessing	L	H	H	H	×	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Remark: H = VIH. L = VIL. × = VIH or VIL

Notes: 1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in "IDLE".
3. All AC timing specs must be met.
4. Only allowed at the boundary of 4 bits burst. Burst interruption at other timings are illegal.

Simplified State Diagram

Simplified State Diagram

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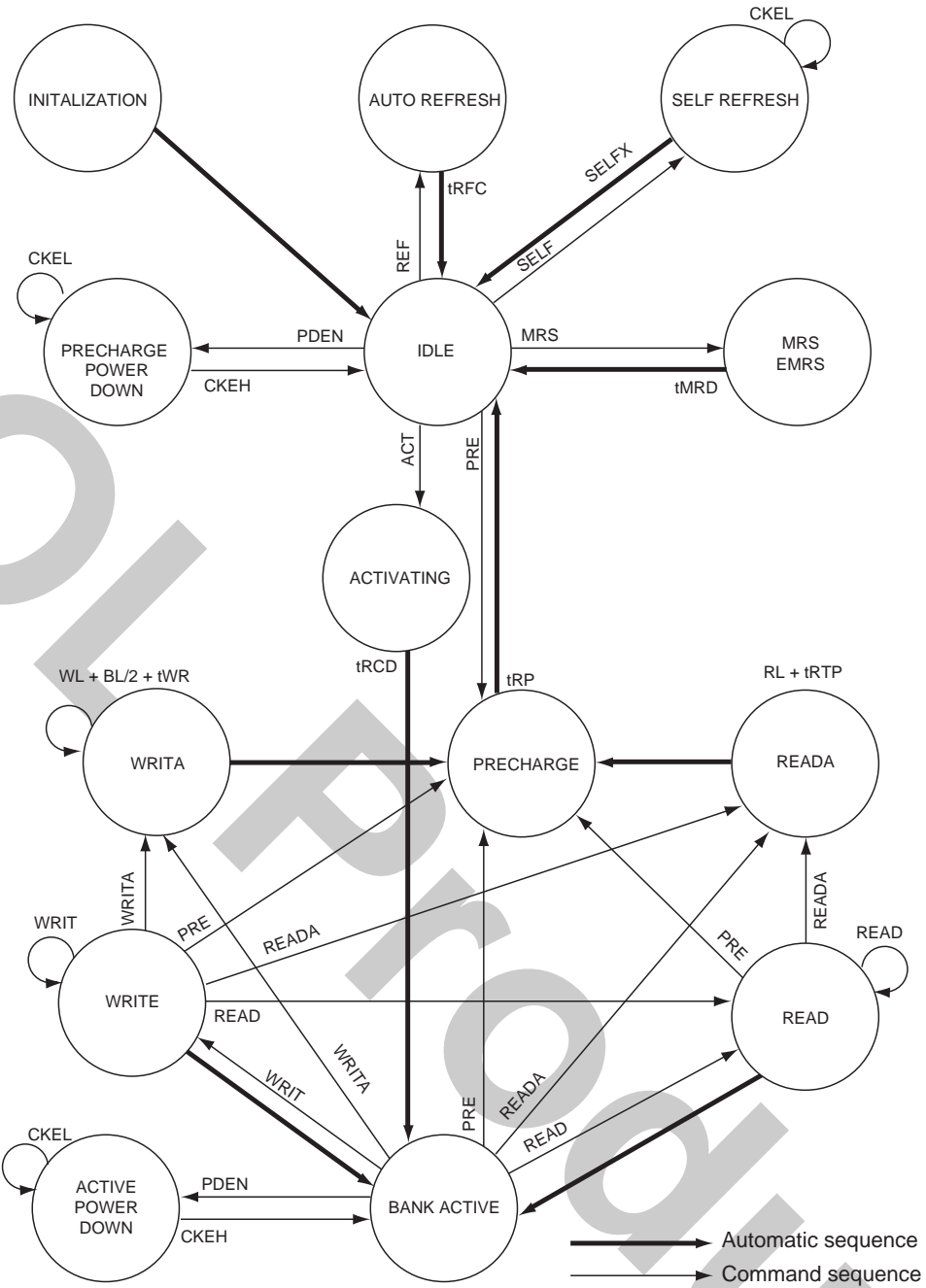
Operation of DDR2 SDRAM

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four or eight in a programmed sequence. Accesses begin with the registration of an active command, which is then followed by a read or write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0, BA1 select the bank; A0 to A13 select the row). The address bits registered coincident with the read or write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

Power On and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-Up and Initialization Sequence

The following sequence is required for power up and initialization.

1. Apply power and attempt to maintain CKE below $0.2 \times$ VDDQ and ODT [1] at a low state (all other inputs may be undefined.)
— VDD, VDDL and VDDQ are driven from a single power converter output, AND
— VTT is limited to 0.95V max, AND
— VREF tracks VDDQ/2.
   or
— Apply VDD before or at the same time as VDDL.
— Apply VDDL before or at the same time as VDDQ.
— Apply VDDQ before or at the same time as VTT and VREF.
   at least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition.
3. For the minimum of 200μs after stable power and clock(CK, /CK), then apply [NOP] or [DESL] and take CKE high.
4. Wait minimum of 400ns then issue precharge all command. [NOP] or [DESL] applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide low to BA0, high to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, high to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue DLL enable command, provide low to A0, high to BA0 and low to BA1 and A13.)
8. Issue a mode register set command for DLL reset.
   (To issue DLL reset command, provide high to A8 and low to BA0, BA1, and A13 to A15.)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD default command (A9 = A8 = A7 = 1) followed by EMRS OCD calibration mode exit command (A9 = A8 = A7 = 0) must be issued with other operating parameters of EMRS.
13. The DDR2 SDRAM is now ready for normal operation.

Note: 1. To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

Power up and Initialization Sequence

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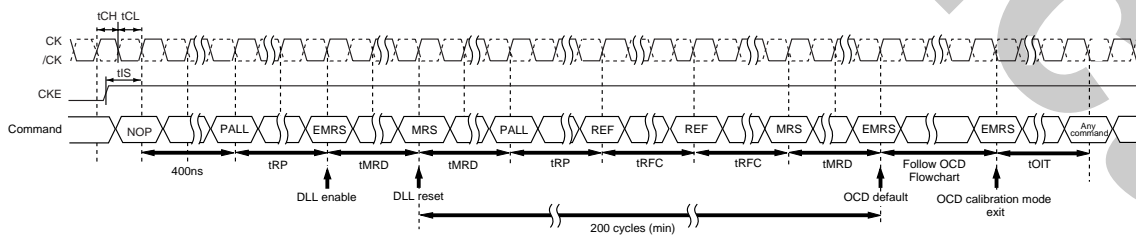
Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, /CAS latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a mode register set command [MRS]. Additionally, DLL disable function, driver impedance, additive /CAS latency, ODT(On Die Termination), single-ended strobe, and OCD (Off-Chip Driver Impedance Adjustment) are also user defined variables and must be programmed with an extended mode register set command [EMRS]. Contents of the Mode Register (MR) or Extended Mode Registers (EMR(#)) can be altered by reexecuting the MRS and EMRS commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

DDR2 SDRAM Mode Register Set [MRS]
The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls /CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0 and BA1, while controlling the state of address pins A0 to A13.

The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 to A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, /CAS latency is defined by A4 to A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 to A11. Refer to the table for specific codes.

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address field
0*1	0	0*1	PD	WR			DLL	TM	/CAS latency			BT	Burst length			Mode register

Burst length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A8	DLL reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst type
0	Sequential
1	Interleave

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A12	Active power down exit timing
0	Fast exit (use tXARD timing)
1	Slow exit (use tXARDS timing)

Write recovery for autoprecharge

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

DDR400 / DDR533

/CAS latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

Notes: 1. BA1 and A13 are reserved for future use and must be programmed to 0 when setting the mode register.
2. WR (min.) (Write Recovery for autoprecharge) is determined by tCK (max.) and WR (max.) is determined by tCK (min.).
WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer   (WR [cycles] = tWR (ns) / tCK (ns)).
The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Mode Register Set (MRS)

DDR2 SDRAM Extended Mode Registers Set [EMRS]

EMRS(1) Programming

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, /DQS disable, OCD program, RDQS enable. The default value of the extended mode register(1) is not defined, therefore the extended mode register(1) must be written after power-up for proper operation. The extended mode register(1) is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0 and low on BA1, while controlling the states of address pins A0 to A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3 to A5 determines the additive latency, A7 to A9 are used for OCD control, A10 is used for /DQS disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

Address field: BA1 | BA0 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0

Extended mode register: 0 | 1 | 0*1 | Qoff | RDQS | /DQS | OCD program | Rtt | Additive latency | Rtt | D.I.C | DLL

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	Rtt (nominal)
0	0	ODT Disabled
0	1	75Ω
1	0	150Ω
1	1	Reserved

A0	DLL enable
0	Enable
1	Disable

Driver impedance adjustment

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode*2
1	1	1	OCD Calibration default*3

A12	Qoff
0	Output buffers enabled
1	Output buffers disabled

A10	/DQS enable
0	Enable
1	Disable

A11	RDQS enable
0	Disable
1	Enable

Additive latency

A5	A4	A3	Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Driver strength control

A1	Output driver impedance control	Driver size
0	Normal	100%
1	Weak	60%

A11 (RDQS enable)	A10 (/DQS enable)	Strobe function matrix			
		RDQS/DM	/RDQS	DQS	/DQS
0	0 (Enable)	DM	High-Z	DQS	/DQS
0	1 (Disable)	DM	High-Z	DQS	High-Z
1	0 (Enable)	RDQS	/RDQS	DQS	/DQS
1	1 (Disable)	RDQS	High-Z	DQS	High-Z

Notes: 1. A13 are reserved for future use, and must be programmed to 0 when setting the extended mode register.
2. When adjust mode is issued, AL from previously set value must be applied.
3. After setting to default, OCD mode needs to be exited by setting A9 to A7 to 000.
Refer to the chapter Off-Chip Driver (OCD)Impedance Adjustment for detailed information.

EMRS(1)

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self-refresh operation and is automatically re-enabled upon exit of self-refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

EMRS(2) Programming: Reserved[1]

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address field

1	0	0[1]	Extended mode register (2)
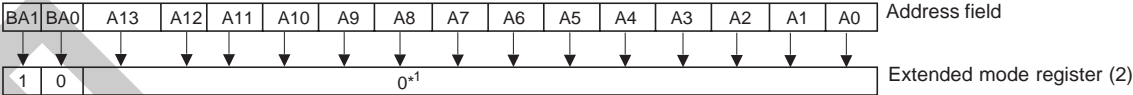
Note : 1. EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMRS(2)

EMRS(3) Programming: Reserved[1]

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field

1	1	0[1]	Extended Mode Register(3)
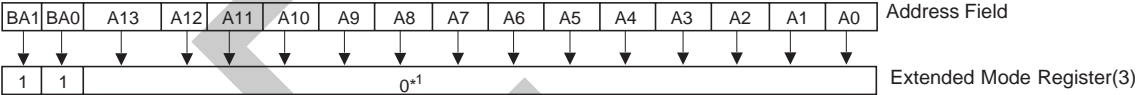
Note : 1. EMRS (3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMRS(3)

Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the OCD Flow Chart is an example of sequence.   Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued.   MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.
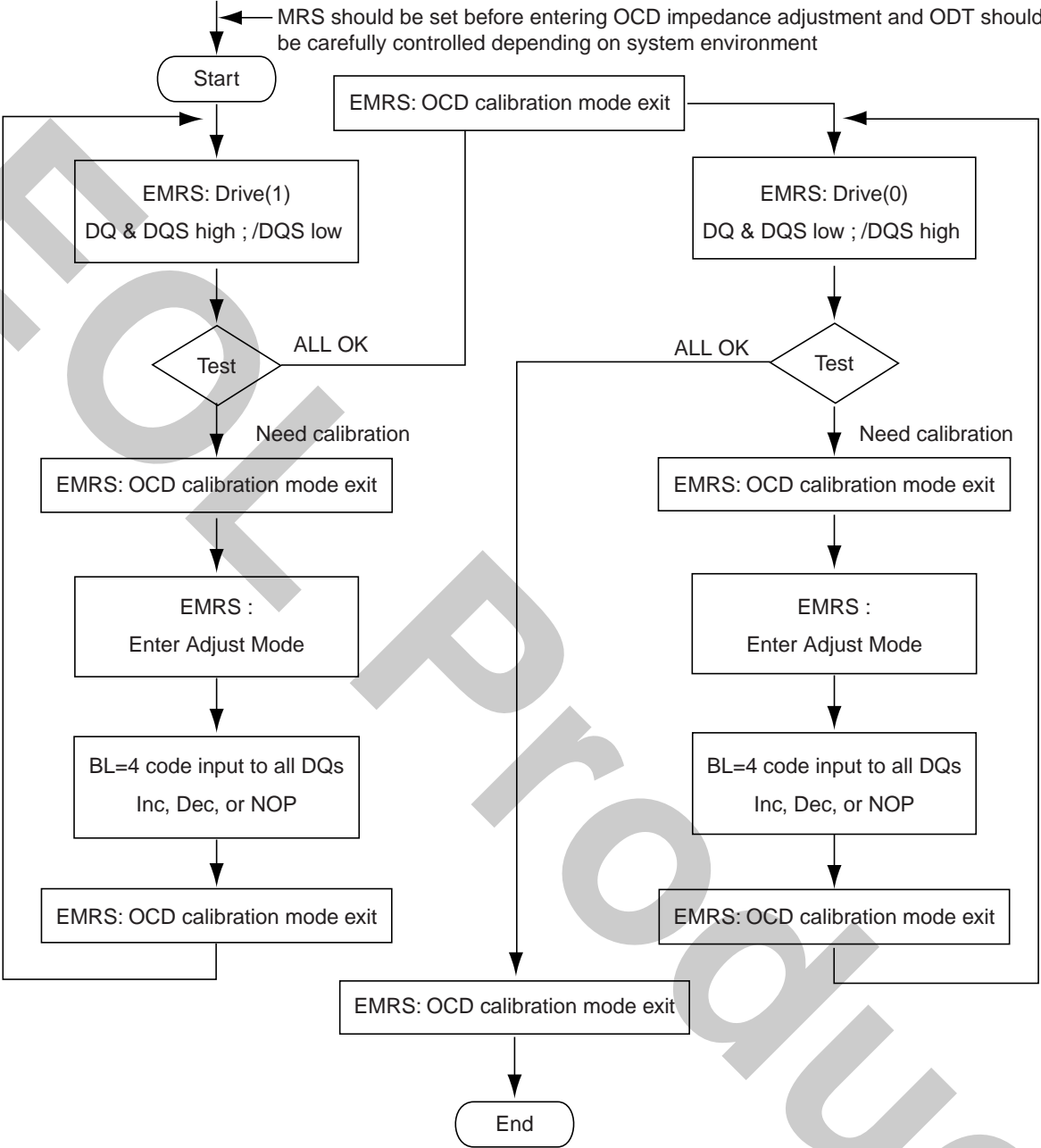
OCD Flow Chart

Extended Mode Register Set for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all /DQS signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all /DQS signals are driven high.

In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics follow approximate nominal V/I curve for 18Ω output drivers, but are not guaranteed. If tighter control is required, which is controlled within 18Ω $\pm$ 3Ω driver impedance range, OCD must be used.

[OCD Mode Set Program]

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS, (RDQS) high and /DQS low
0	1	0	Drive (0) DQ, DQS, (RDQS) low and /DQS high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD Impedance Adjustment

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR2 SDRAM as in OCD Adjustment Program table. For this operation, burst length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in OCD Adjustment Program table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16-step range.

[OCD Adjustment Program]

4bits burst data inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP	NOP
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other combinations				Reserved	

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For proper operation of adjust mode, WL = RL − 1 = AL + CL − 1 clocks and tDS/tDH should be met as the Output Impedance Control Register Set Cycle. For input data pattern for adjustment, DT0 to DT3 is a fixed order and not affected by MRS addressing mode (i.e. sequential or interleave).
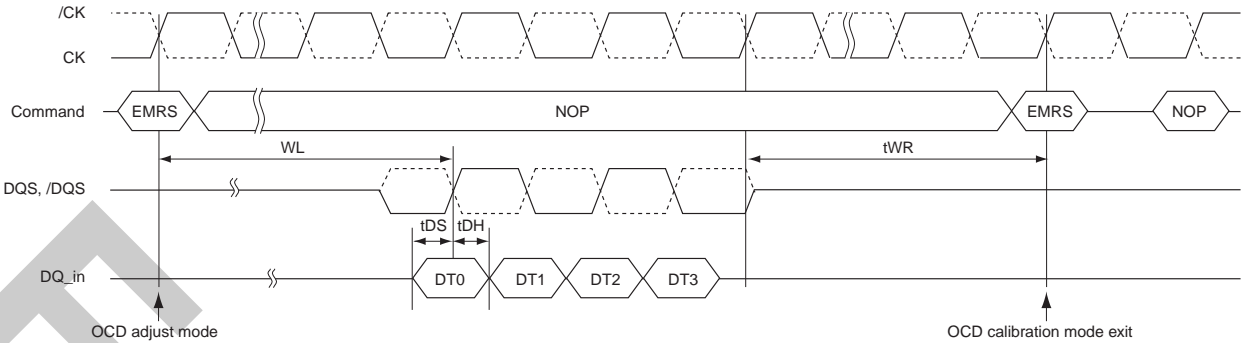
Output Impedance Control Register Set Cycle

Drive Mode

Drive mode, both drive (1) and drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after "Enter drive mode" command and all output drivers are turned-off tOIT after "OCD calibration mode exit" command as the "Output Impedance Measurement/Verify Cycle".
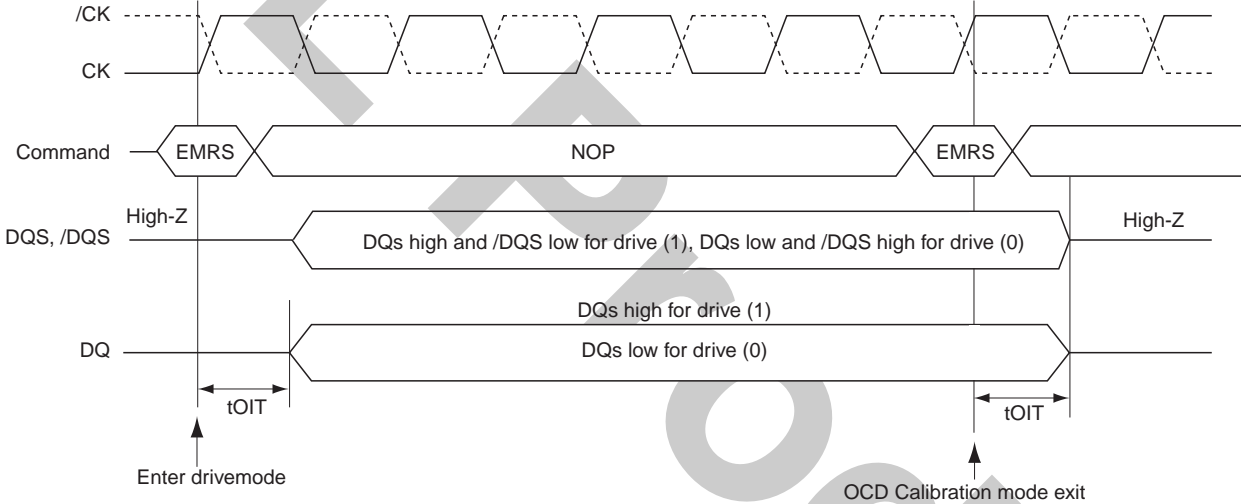
Output Impedance Measurement/Verify Cycle

ODT(On Die Termination)

On Die Termination (ODT), is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for $\times$ 8 configurations via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is turned off and not supported in self-refresh mode.
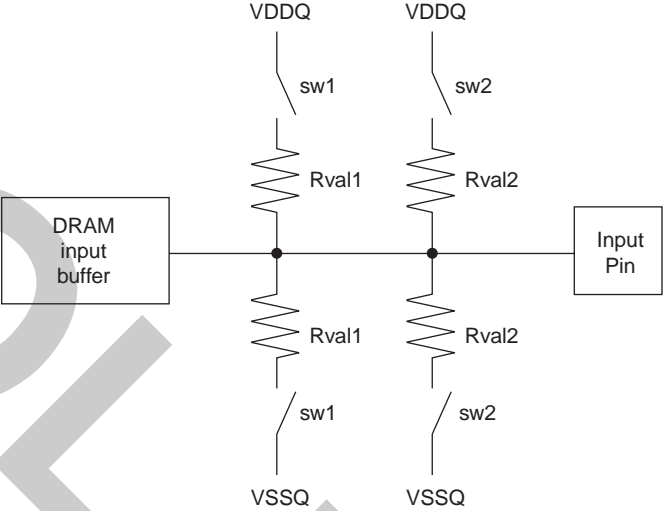
Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by Rtt (nominal) in EMRS
Termination included on all DQs, DM, DQS, /DQS, RDQS and /RDQS pins.
Target Rtt (Ω) = (Rval1) / 2 or (Rval2) / 2

Functional Representation of ODT
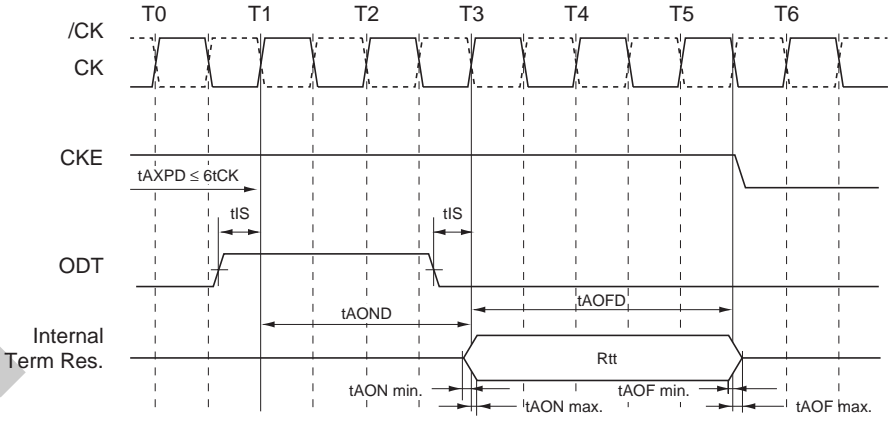
ODT Timing for Active and Standby Mode
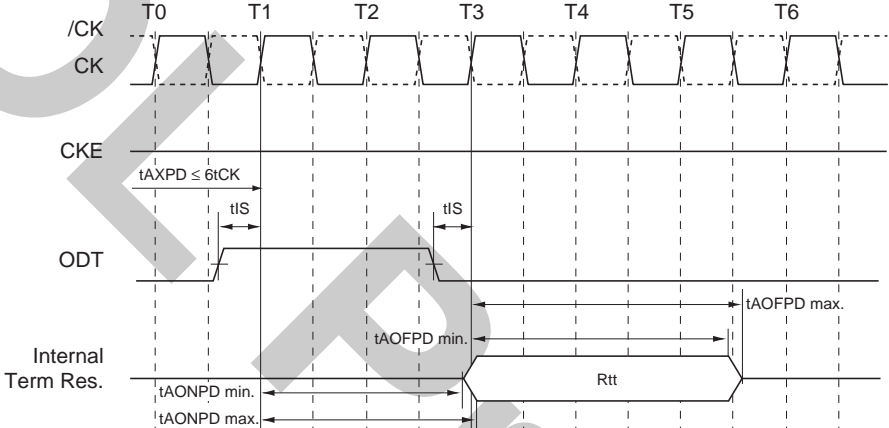
ODT Timing for Power down Mode

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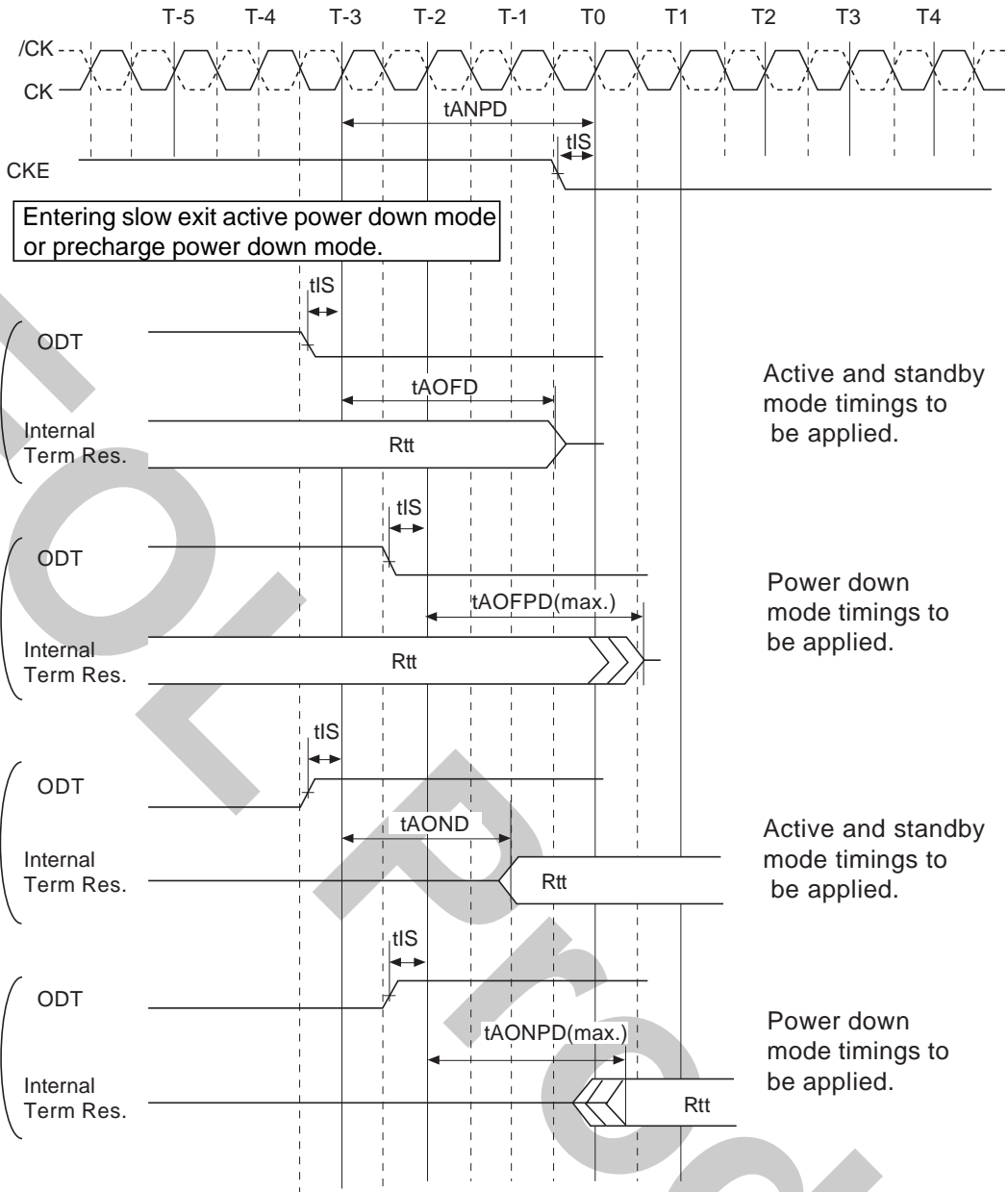
ODT Timing Mode Switch at Entering Power Down Mode
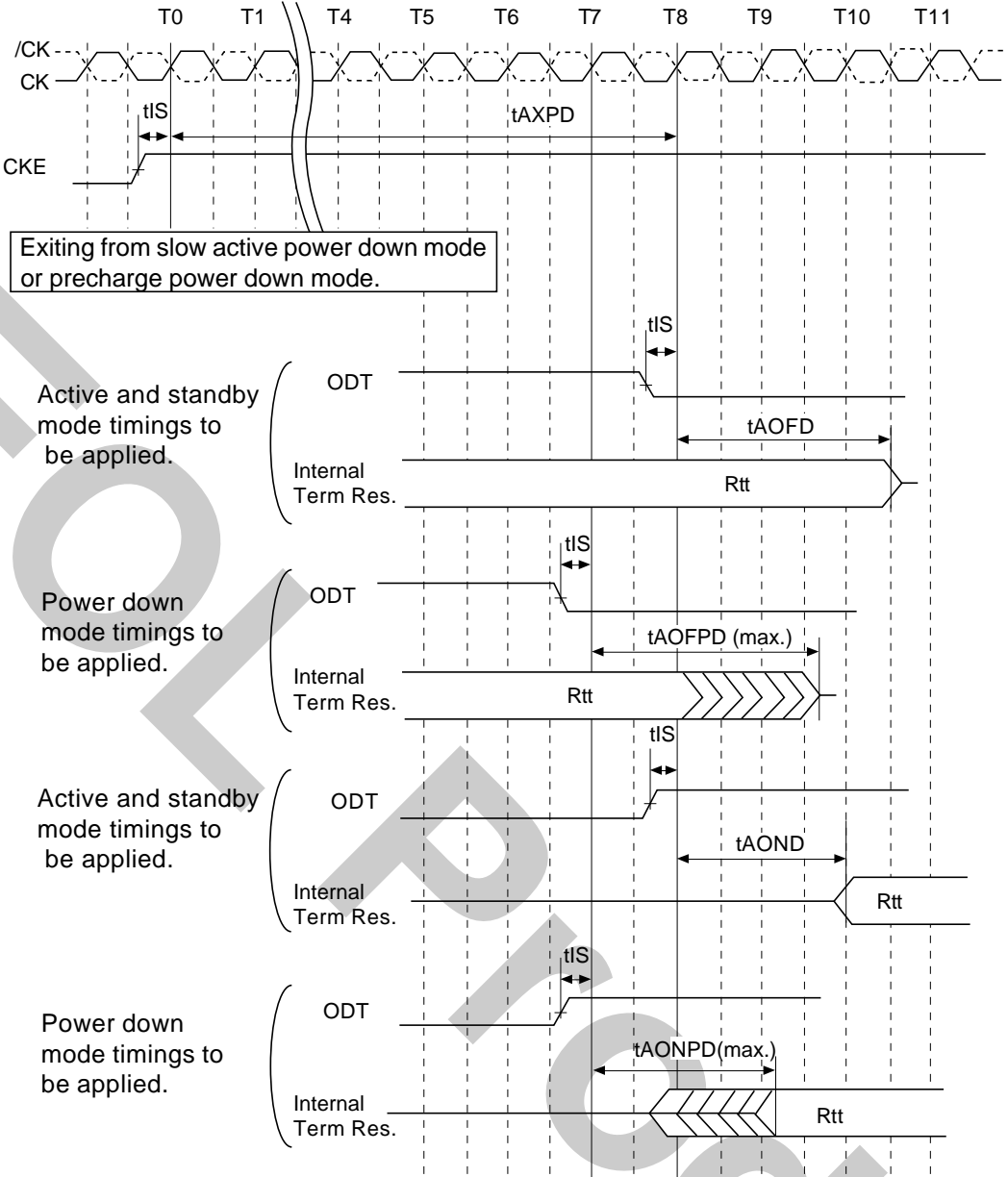
ODT Timing Mode Switch at Exiting Power Down Mode

Bank Activate Command [ACT]

The bank activate command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock. The bank addresses BA0 and BA1, are used to select the desired bank. The row address A0 through A13 is used to determine which row to activate in the selected bank. The Bank activate command must be applied before any read or write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCD (min.) specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCD (min.) is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the /RAS cycle time of the device (tRC), which is equal to tRAS + tRP. The minimum time interval between successive bank activate commands to the different bank is determined by (tRRD).
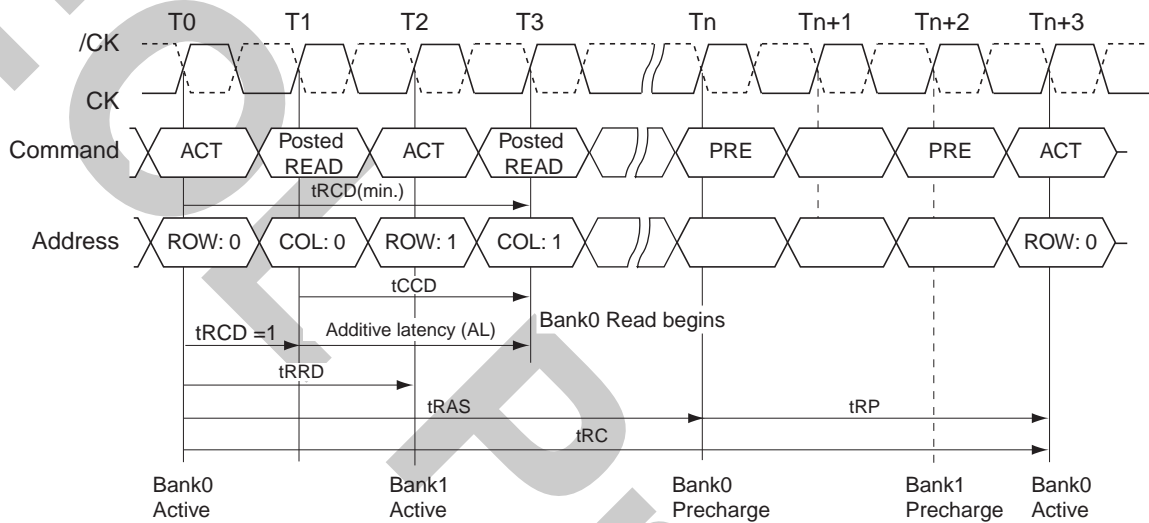
Bank Activate Command Cycle (tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2)

Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /RAS high, /CS and /CAS low at the clock's rising edge. /WE must also be defined at this time to determine whether the access cycle is a read operation (/WE high) or a write operation (/WE low).

The DDR2 SDRAM provides a fast column access operation. A single read or write command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32M bits × 4 I/O × 4 banks chip has a page length of 2048 bits (defined by CA0 to CA9, CA11). The page length of 2048 is divided into 512 uniquely addressable boundary segments (4 bits each). A 4 bits burst operation will occur entirely within one of the 512 groups beginning with the column address supplied to the device during the read or write command (CA0 to CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4-bit burst operation. The minimum /CAS to /CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

Posted /CAS

Posted /CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a /CAS read or write command to be issued immediately after the /RAS bank activate command (or any time during the /RAS-/CAS-delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the /CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCD (min), then AL (greater than 0) must be written into the EMRS. The Write Latency (WL) is always defined as RL − 1 (read latency −1) where read latency is defined as the sum of additive latency plus /CAS latency (RL = AL + CL).

Read Followed by a Write to the Same Bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4]

Read Followed by a Write to the Same Bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2]

ELPIDA
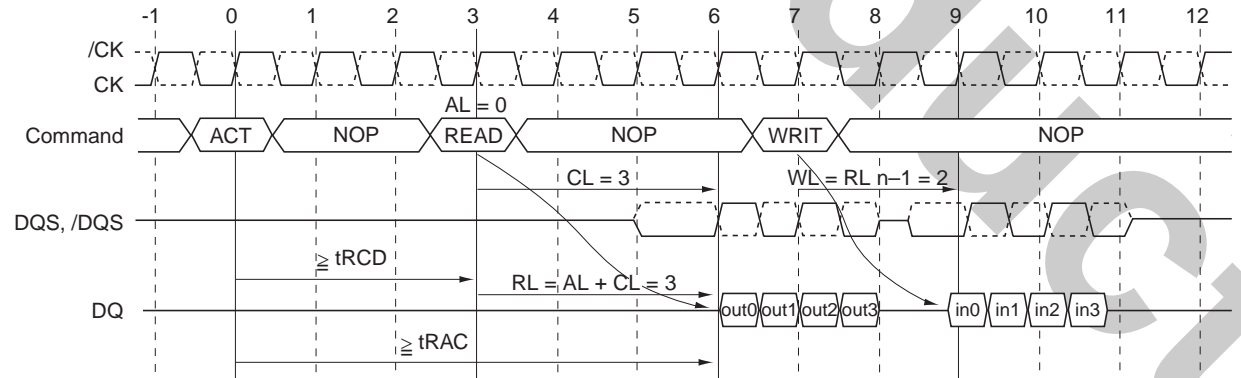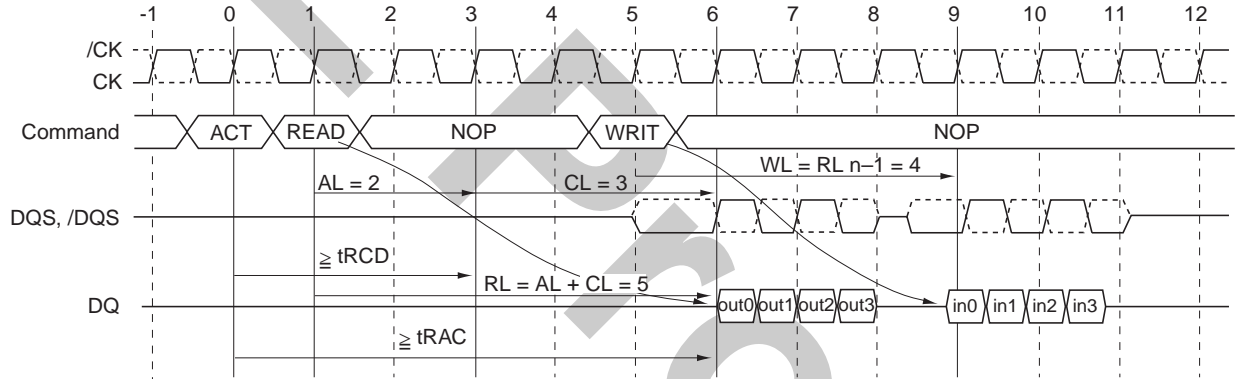
Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR2 SDRAM supports 4 bits burst and 8bits burst modes only. For 8 bits burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR-I SDRAM operation. Seamless burst read or write operations are supported.

Unlike DDR-I devices, interruption of a burst read or writes operation is limited to ready by Read or Write by Write at the boundary of Burst 4. Therefore the burst stop command is not supported on DDR2 SDRAM devices.

[Burst Length and Sequence]

Burst length	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4	000	0, 1, 2, 3	0, 1, 2, 3
	001	1, 2, 3, 0	1, 0, 3, 2
	010	2, 3, 0, 1	2, 3, 0, 1
	011	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: Page length is a function of I/O organization and column addressing
16M bits × 8 organization (CA0 to CA9); Page Length = 1024 bits

Burst Read Command [READ]

The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

The RL is equal to an additive latency (AL) plus /CAS latency (CL). The CL is defined by the mode register set (MRS), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the extended mode register set (EMRS).
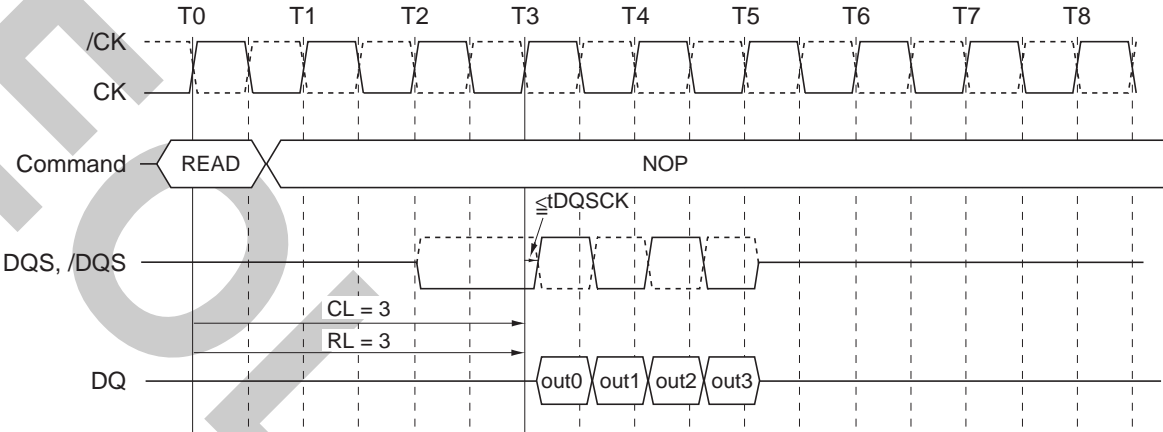
Burst Read Operation (RL = 3, BL = 4 (AL = 0 and CL = 3))
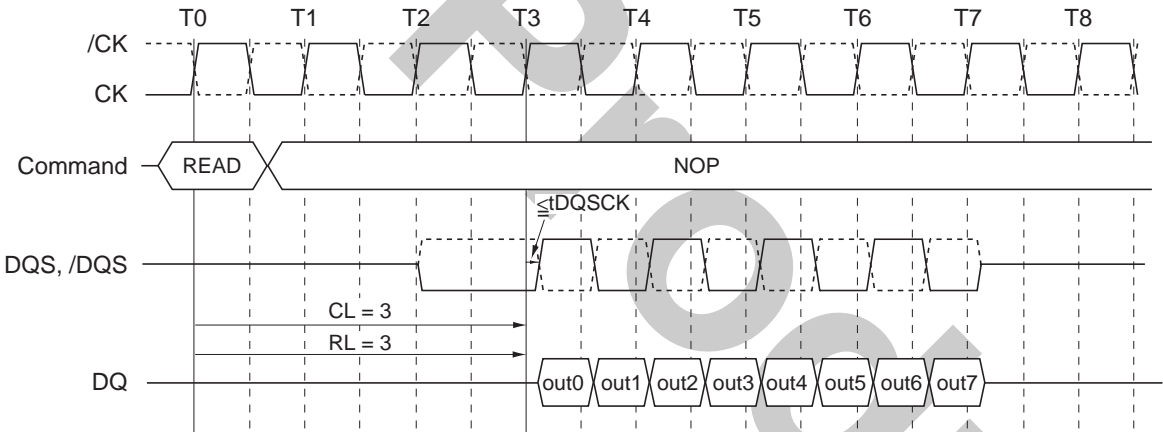
Burst Read Operation (RL = 3, BL = 8 (AL = 0 and CL = 3))
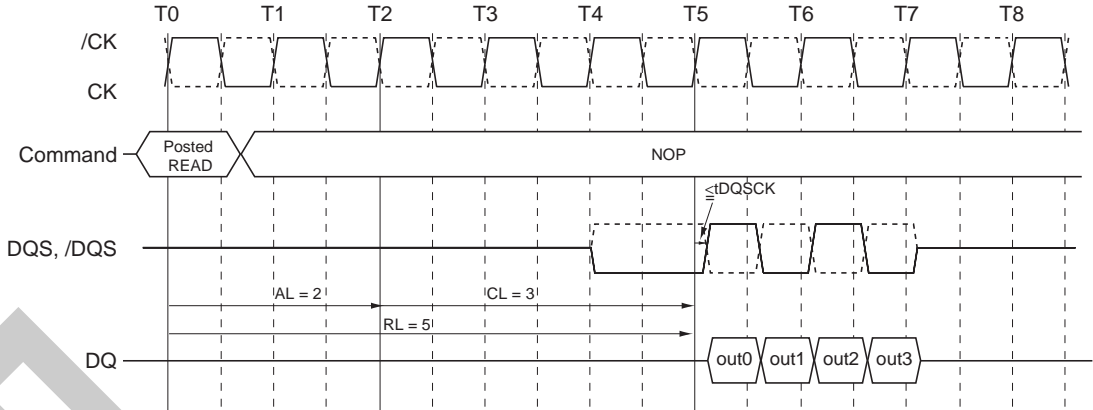
Burst Read Operation (RL = 5, BL = 4 (AL = 2, CL = 3))
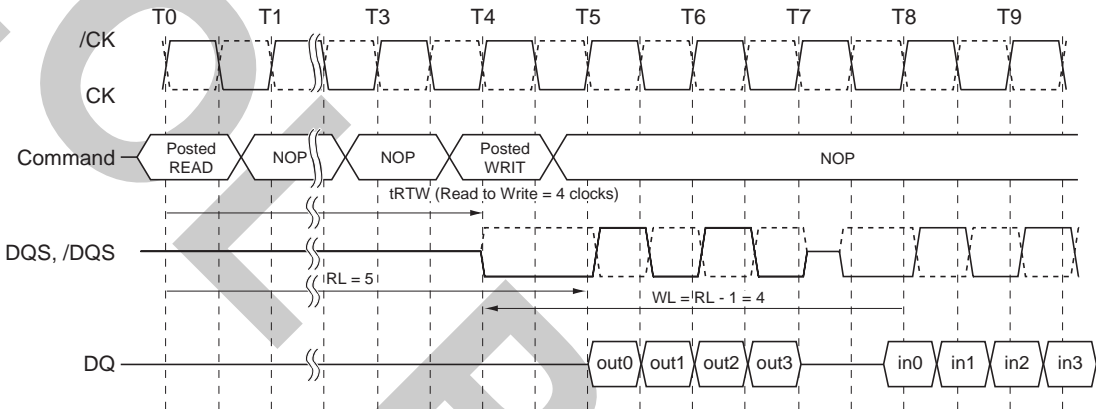
Burst Read Followed by Burst Write (RL = 5, WL = RL-1 = 4, BL = 4)

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks.
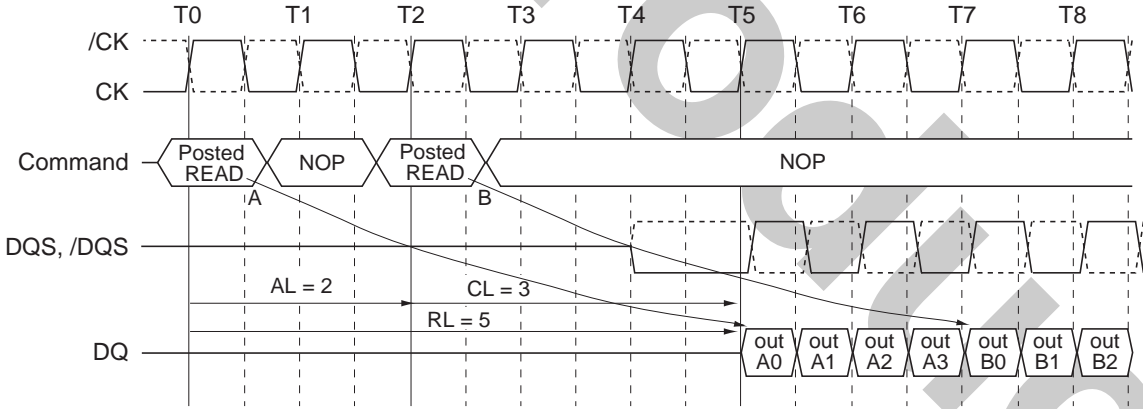
Seamless Burst Read Operation (RL = 5, AL = 2, and CL = 3)

Enabling a read command at every other clock supports the seamless burst read operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Burst interrupt is only allowed at this timing.
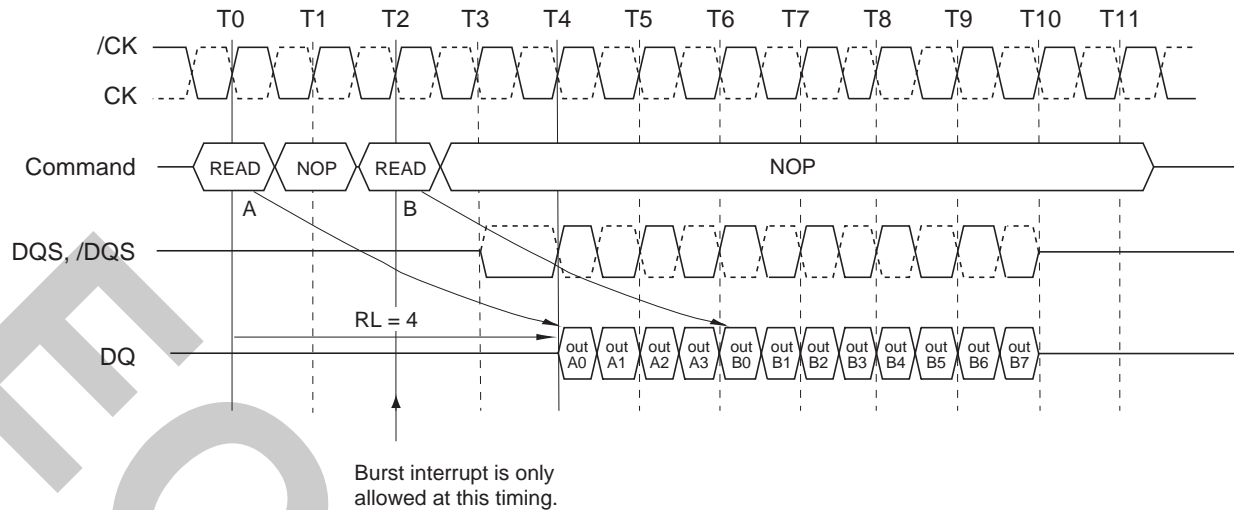
Burst Read Interrupt by Read

Notes :1. Read burst interrupt function is only allowed on burst of 8. burst interrupt of 4 is prohibited.

    2. Read burst of 8 can only be interrupted by another read command. Read burst interruption by write command or precharge command is prohibited.

    3. Read burst interrupt must occur exactly two clocks after previous read command. any other read burst interrupt timings are prohibited.

    4. Read burst interruption is allowed to any bank inside DRAM.

    5. Read burst with auto precharge enabled is not allowed to interrupt.

    6. Read burst interruption is allowed by another read with auto precharge command.

    7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum read to precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).

Burst Write Command [WRIT]

The Burst Write command is initiated by having /CS, /CAS and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to $(AL + CL -1)$. A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).
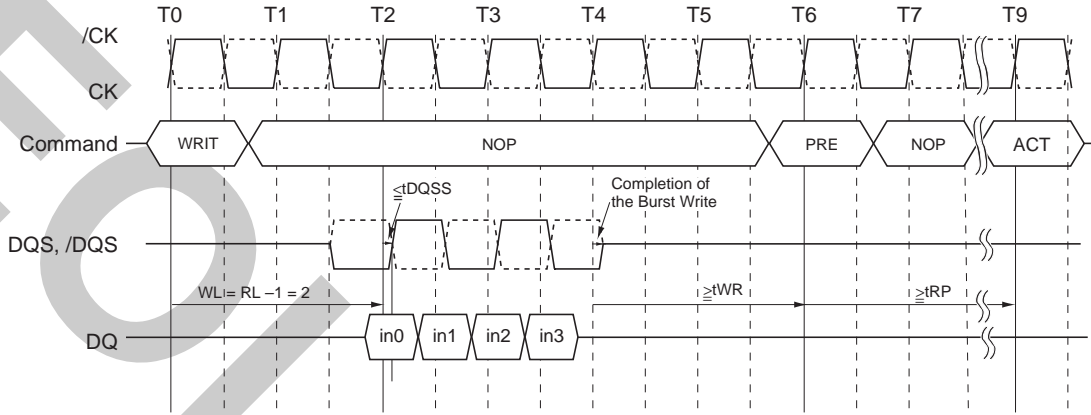
Burst Write Operation (RL = 3, WL = 2, BL = 4 tWR = 2 (AL=0, CL=3))
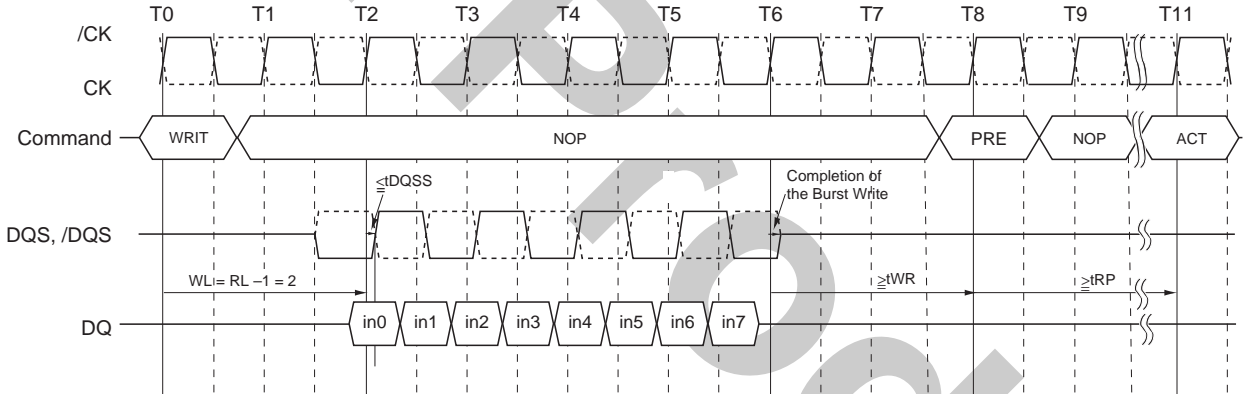
Burst Write Operation (RL = 3, WL = 2, BL = 8 (AL=0, CL=3))
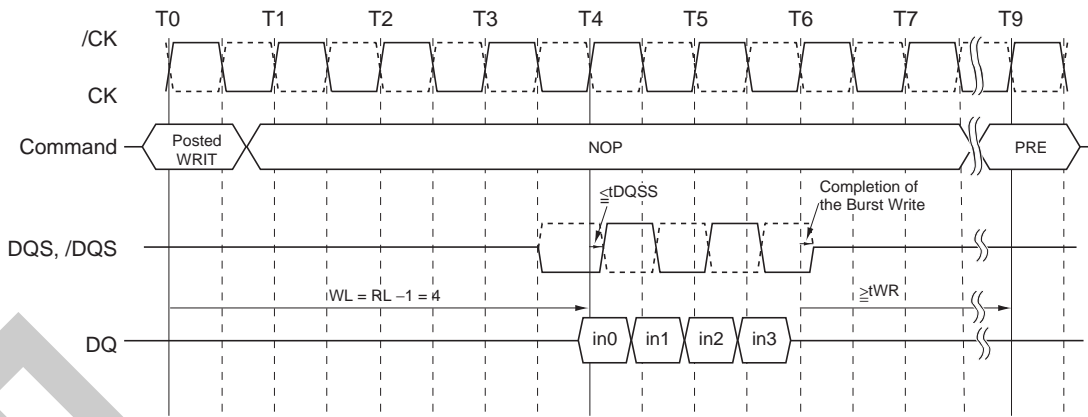
Burst Write Operation (RL = 5, WL = 4, BL = 4 tWR = 3 (AL=2, CL=3))
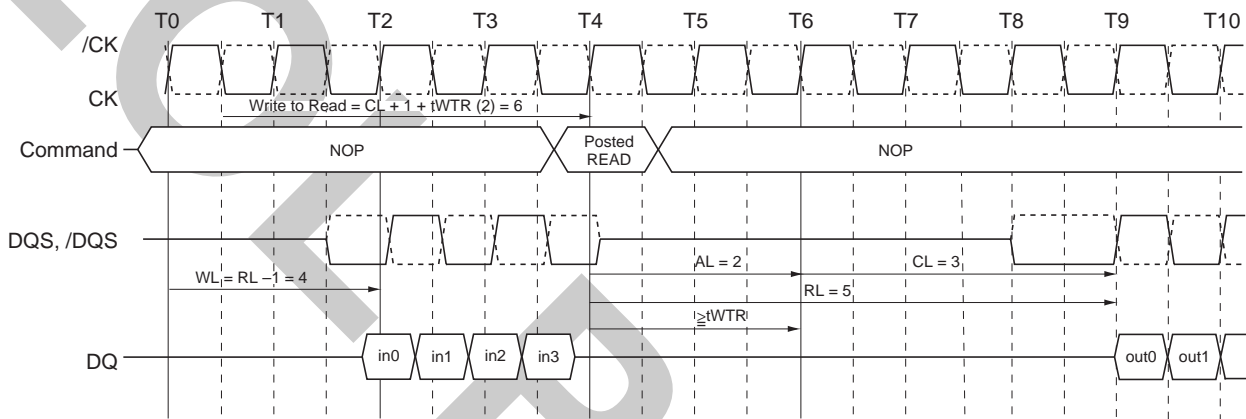
Burst Write Followed by Burst Read (RL = 5, BL = 4, WL = 4, tWTR = 2 (AL=2, CL=3))

The minimum number of clock from the burst write command to the burst read command is CL + 1 + a write to-read-turn-around-time (tWTR). This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array.
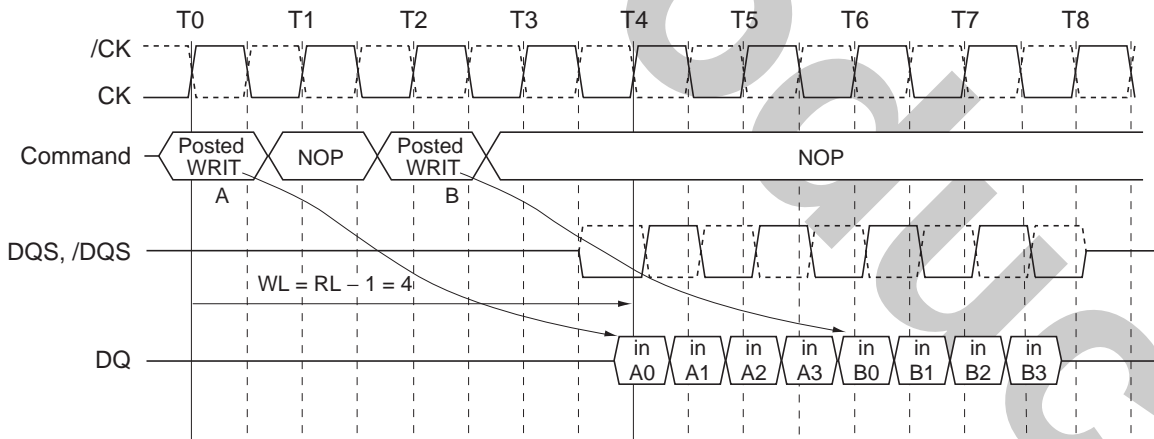
Seamless Burst Write Operation (RL = 5, WL = 4, BL = 4)

Enabling a write command every other clock supports the seamless burst write operation. This operation is allowed regardless of same or different banks as long as the banks are activated.
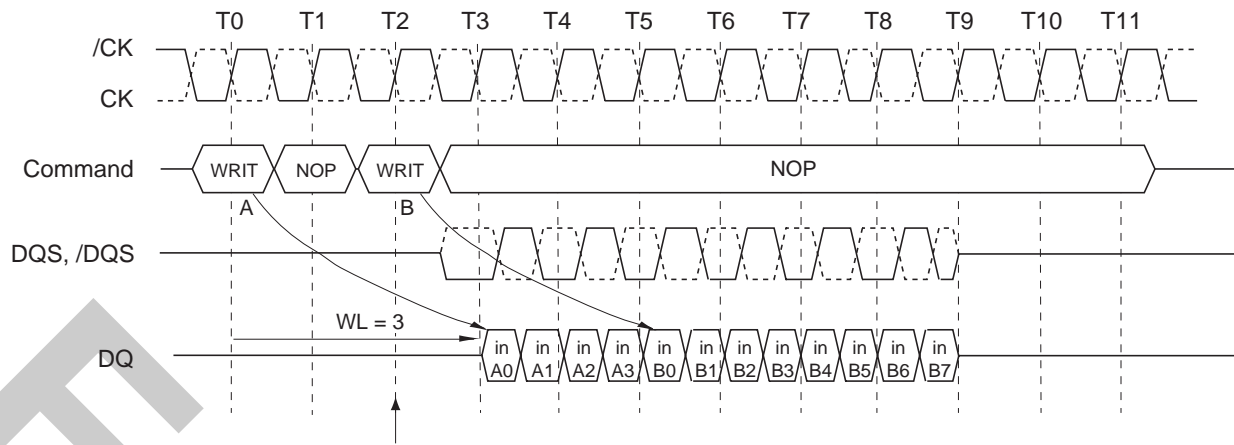
Write Interrupt by Write (WL = 3, BL = 8)

Notes :1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.

2. Write burst of 8 can only be interrupted by another write command. Write burst interruption by read command or precharge command is prohibited.

3. Write burst interrupt must occur exactly two clocks after previous write command. Any other write burst interrupt timings are prohibited.

4. Write burst interruption is allowed to any bank inside DRAM.

5. Write burst with auto precharge enabled is not allowed to interrupt.

6. Write burst interruption is allowed by another write with auto precharge command.

7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, minimum write to precharge timing is WL+BL/2+tWR where tWR starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, Consistent with the implementation on DDR-I SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.

Write mask latency = 0
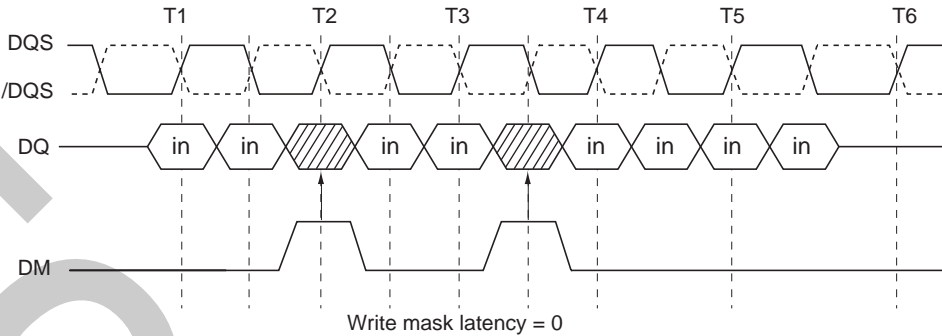
Data Mask Timing
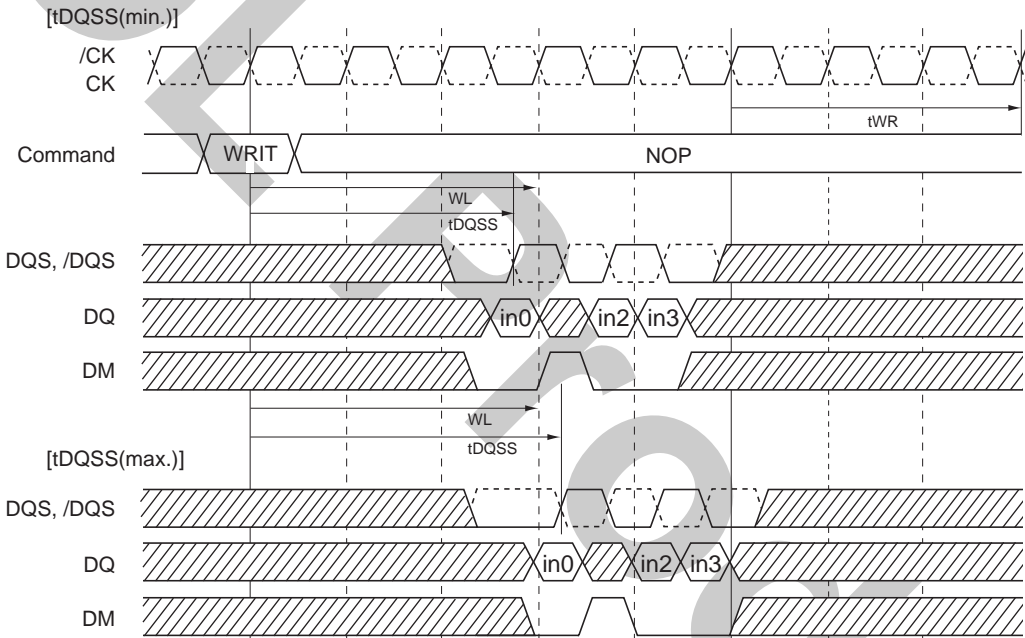
Data Mask Function, WL = 3, AL = 0 shown

Precharge Command [PRE]

The precharge command is used to precharge or close a bank that has been activated. The precharge command is triggered when /CS, /RAS and /WE are low and /CAS is high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 are used to define which bank to precharge when the command is issued.

[Bank Selection for Precharge by Address Bits]

A10	BA0	BA1	Precharged Bank(s)
L	L	L	Bank 0 only
L	H	L	Bank 1 only
L	L	H	Bank 2 only
L	H	H	Bank 3 only
H	×	×	All banks 0 to 3

Remark: H: VIH, L: VIL, ×: VIH or VIL

Burst Read Operation Followed by Precharge

Minimum read to precharge command spacing to the same bank = AL + BL/2 clocks

For the earliest possible precharge, the precharge command may be issued on the rising edge that is

"Additive latency (AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.
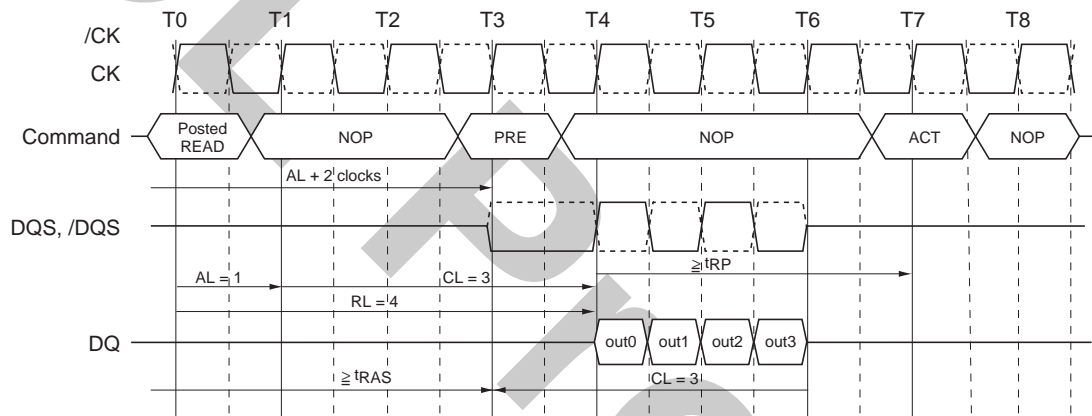
Burst Read Operation Followed by Precharge (RL = 4, BL = 4 (AL=1, CL=3))
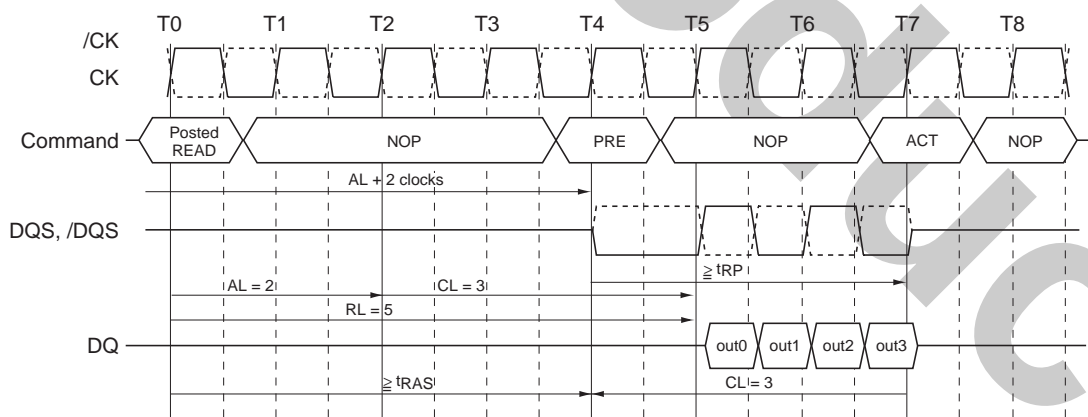
Burst Read Operation Followed by Precharge (RL = 5, BL = 4 (AL=2, CL=3))
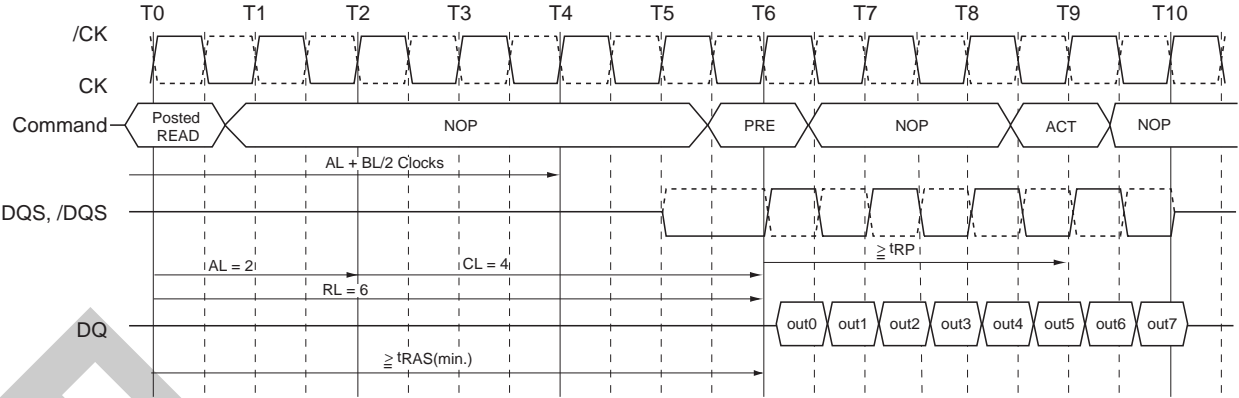
Burst Read Operation Followed by Precharge (RL = 6 (AL=2, CL=4, BL=8))

Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clocks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No precharge command should be issued prior to the tWR delay, as DDR2 SDRAM allows the burst interrupt operation only Read by Read or Write by Write at the boundary of burst 4.
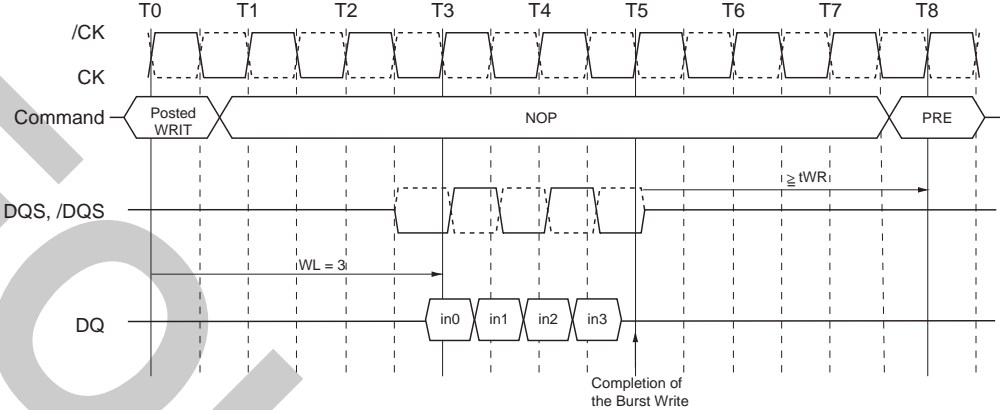
Burst Write Followed by Precharge (WL = (RL-1) =3)
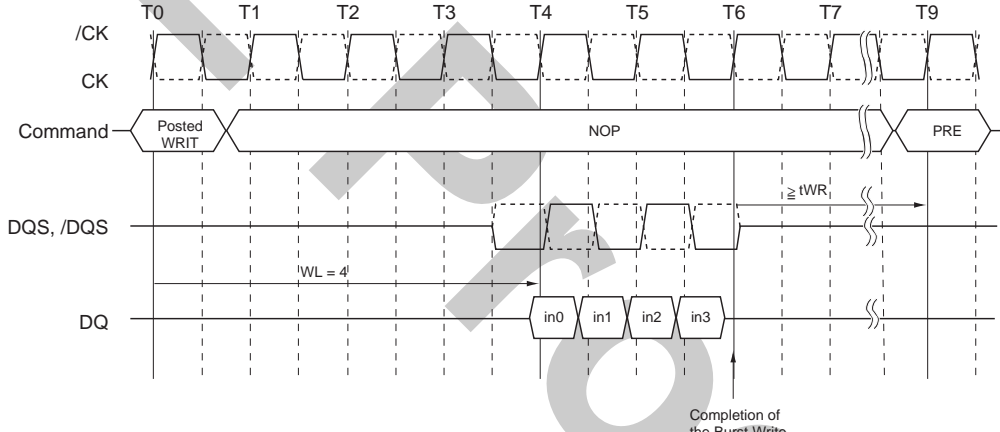
Burst Write Followed by Precharge (WL = (RL-1) = 4)
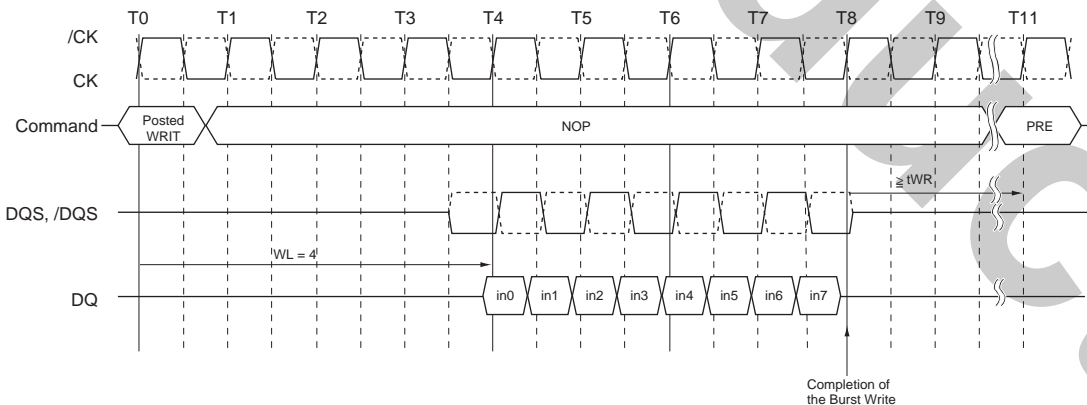
Burst Write Followed by Precharge (WL = (RL-1) = 4,BL= 8)

Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto-precharge function. When a read or a write command is given to the DDR2 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write Command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is /CAS latency (CL) clock cycles before the end of the read burst.

Auto-precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The /RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Burst Read with Auto Precharge [READA]

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an auto Precharge operation on the rising edge which is (AL + BL/2) cycles later from the read with AP command when the condition that. When tRAS (min) is satisfied. If tRAS (min.) is not satisfied at the edge, the start point so auto-precharge operation will be delayed until tRAS (min.) is satisfied. A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

(1) The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.
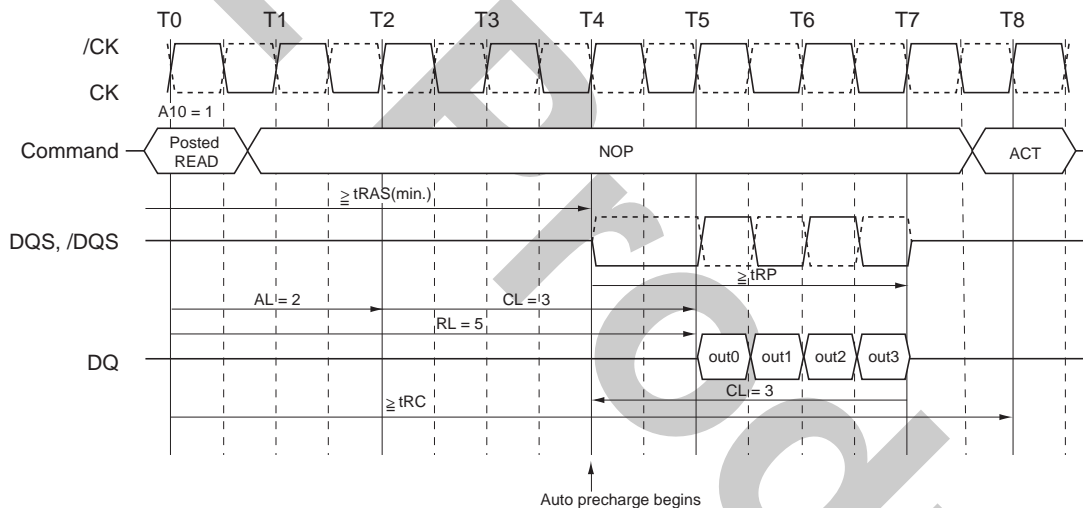
Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRC limit)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3))
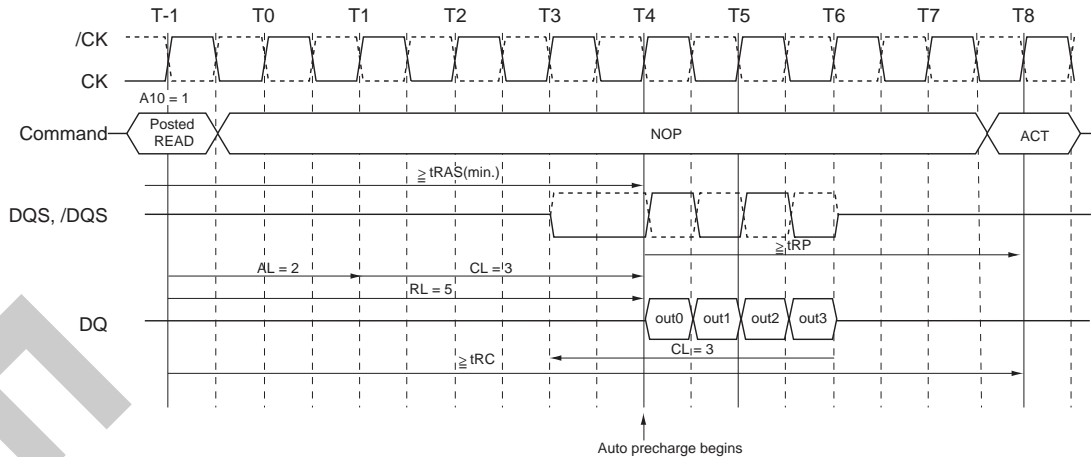
Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRAS lockout case)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3))
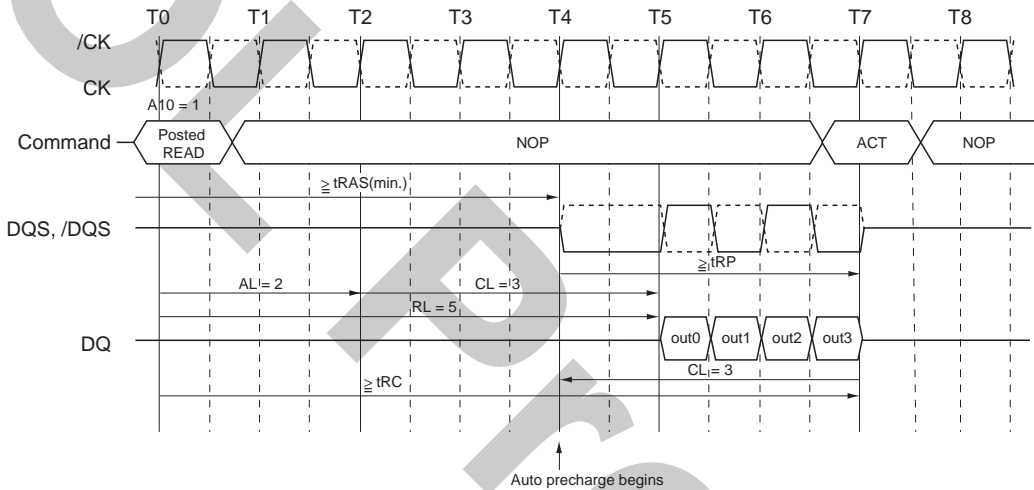
Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP limit)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3)
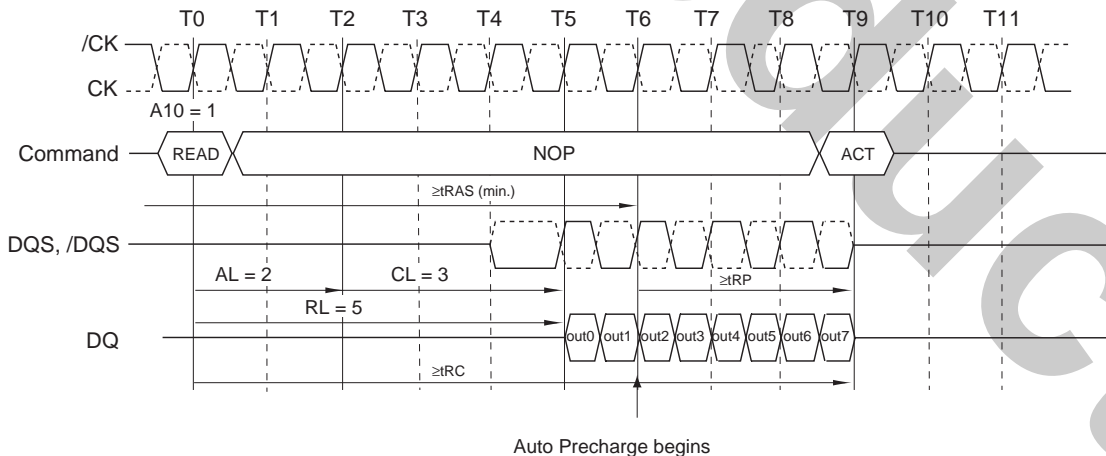
Burst Read with Auto Precharge Followed by an Activation to the Same Bank
(RL = 5, BL = 8 (AL = 2, CL = 3)

Burst Write with Auto-Precharge [WRITA]

If A10 is high when a write command is issued, the Write with auto-precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst writes plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The data-in to bank activate delay time (tWR + tRP) has been satisfied.

(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.
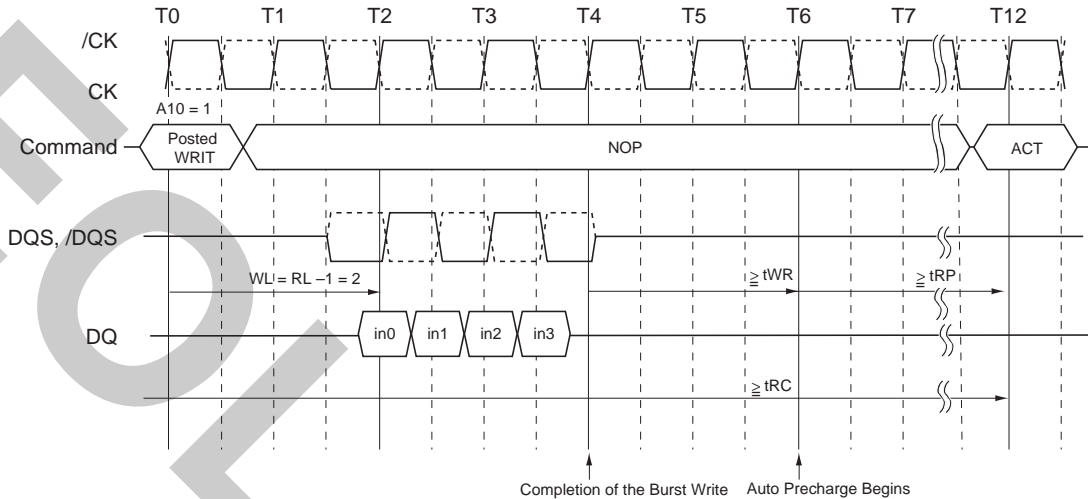
Burst Write with Auto-Precharge (tRC Limit) (WL = 2, tWR =2, tRP=3)
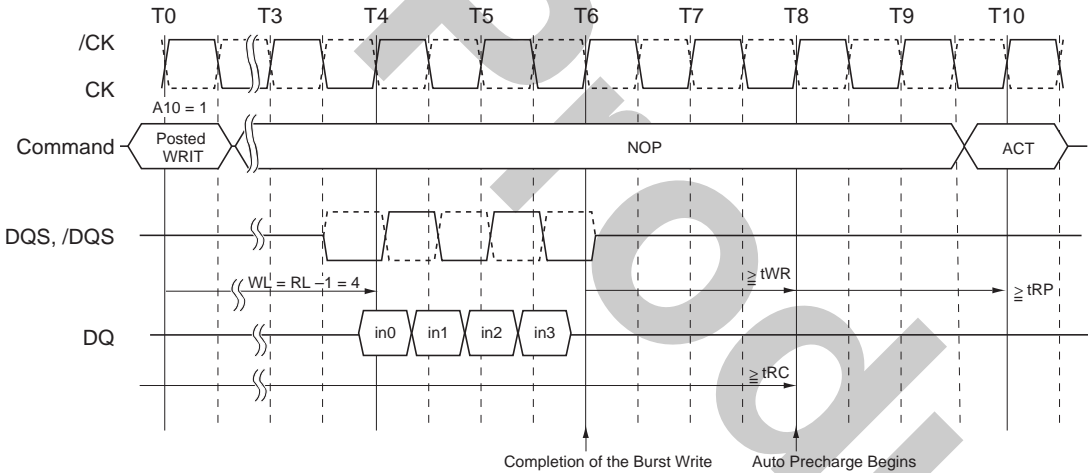
Burst Write with Auto-Precharge (tWR + tRP) (WL = 4, tWR =2, tRP=3)

T0 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13

/CK

CK

A10 = 1

Command — WRIT — NOP — ACT

DQS, /DQS

≥tWR   ≥tRP

WL = RL − 1 = 4

DQ   in0 in1 in2 in3 in4 in5 in6 in7

≥tRC

Auto Precharge begins.
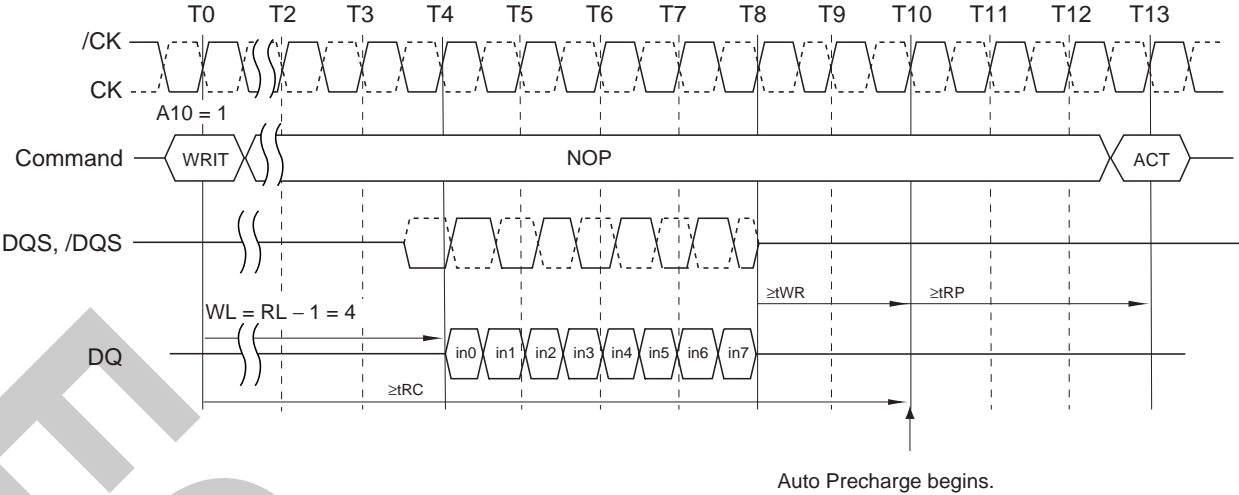
Burst Write with Auto Precharge Followed by an Activation to the Same Bank
(WL = 4, BL = 8, tWR = 2, tRP = 3)

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Refresh Requirements

DDR2 SDRAM requires a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit automatic refresh command, or by an internally timed event in self-refresh mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing.

Automatic Refresh Command [REF]

When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters the automatic refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the precharge time (tRP) before the auto refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the auto refresh command (REF) and the next activate command or subsequent auto refresh command must be greater than or equal to the auto refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any refresh command and the next Refresh command is $9 \times$ tREFI.
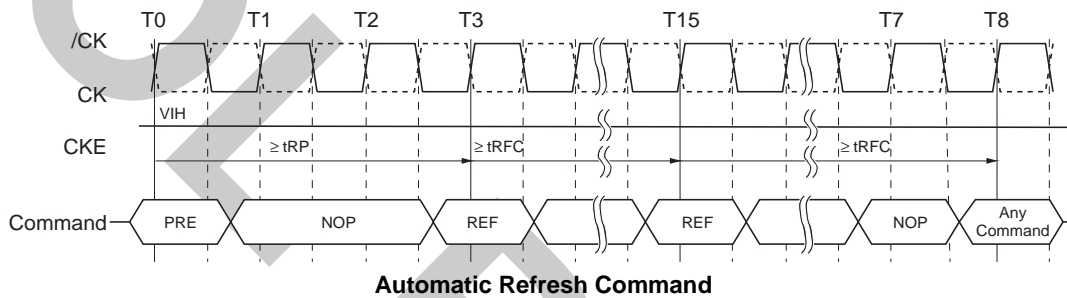
Automatic Refresh Command

Self Refresh Command [SELF]

The DDR2 SDRAM device has a built-in timer to accommodate self-refresh operation. The self-refresh command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock.

ODT must be turned off before issuing self refresh command, by either driving ODT pin low or using EMRS command. Once the command is registered, CKE must be held low to keep the device in self-refresh mode.

When the DDR2 SDRAM has entered self refresh mode all of the external signals except CKE, are "don't care". The clock is internally disabled during self-refresh operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit self refresh operation. Once self-refresh exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire self-refresh exit period tXSRD for proper operation. NOP or deselect commands must be registered on each positive clock edge during the self-refresh exit interval. ODT should also be turned off during tXSRD.
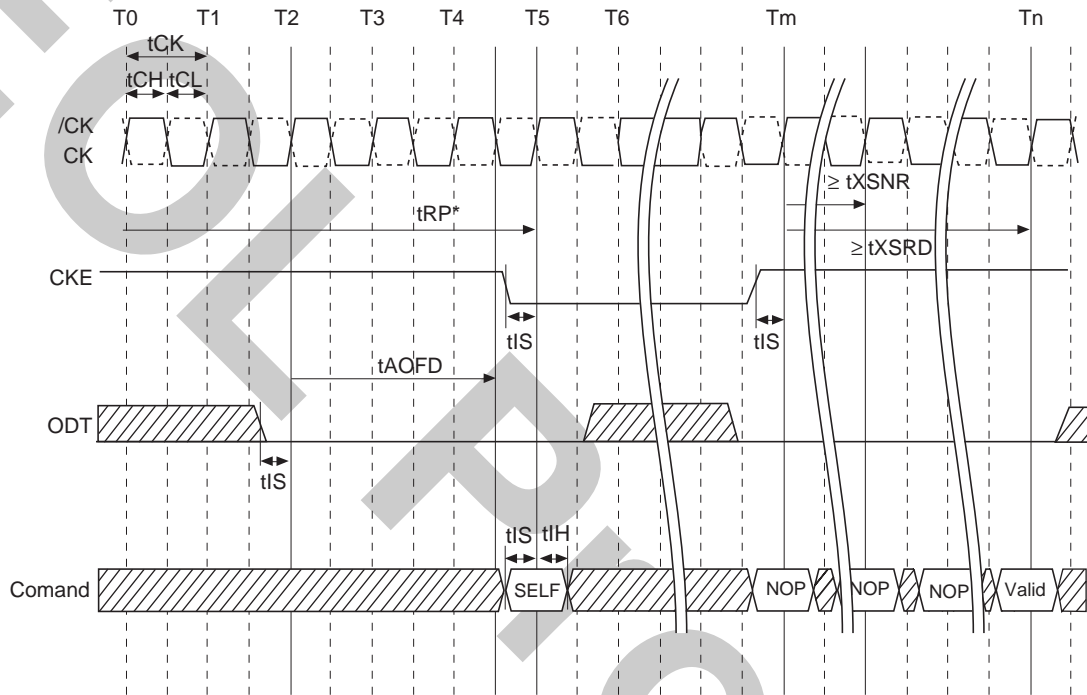
Notes: 1. Device must be in the "All banks idle" state prior to entering self refresh mode.
   2. ODT must be turned off tAOFD before entering self refresh mode, and can be turned on again when tXSRD timing is satisfied.
   3. tXSRD is applied for a read or a read with autoprecharge command.
   4. tXSNR is applied for any command except a read or a read with autoprecharge command.

Self Refresh Command

Power-Down [PDEN]

Power-down is synchronously entered when CKE is registered low (along with NOP or deselect command). CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care". CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes high. Power-down exit latency is defined at AC Characteristics table of this data sheet.
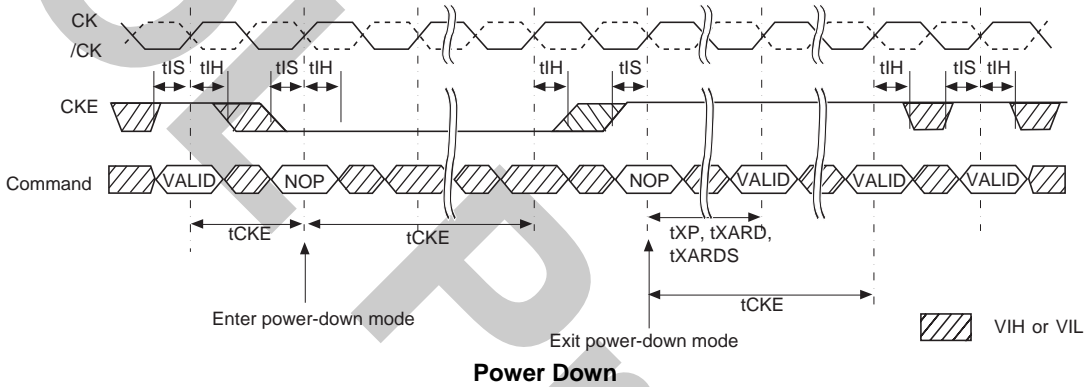
Power Down

Read to Power-Down Entry

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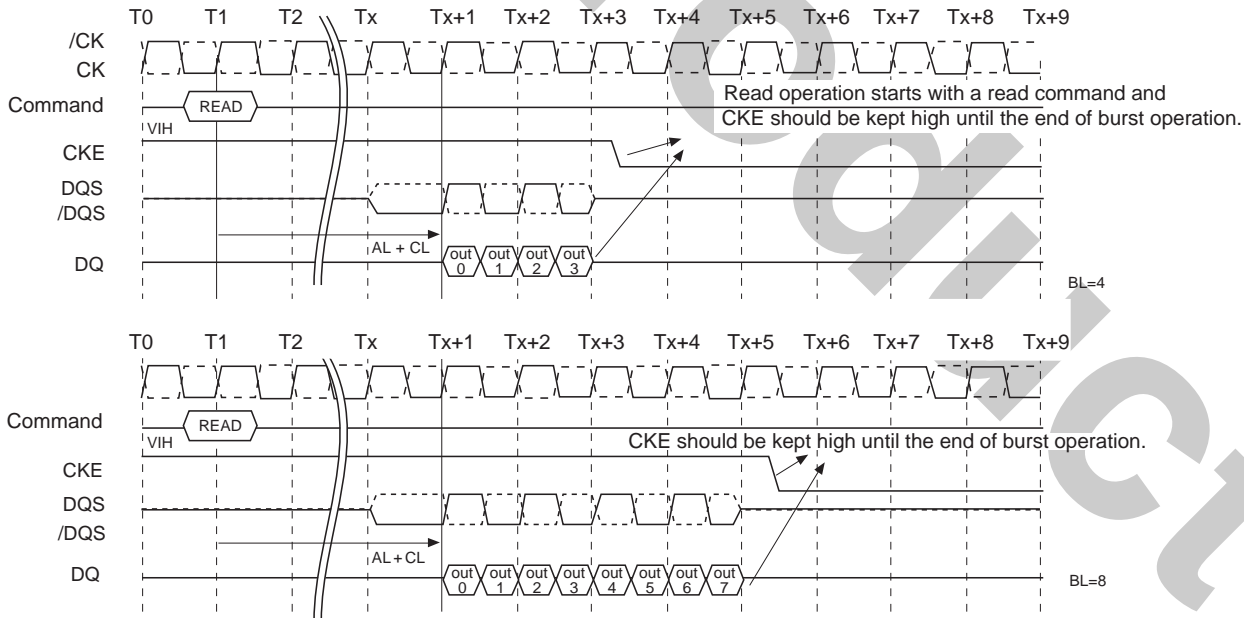
Read with Auto Precharge to Power-Down Entry
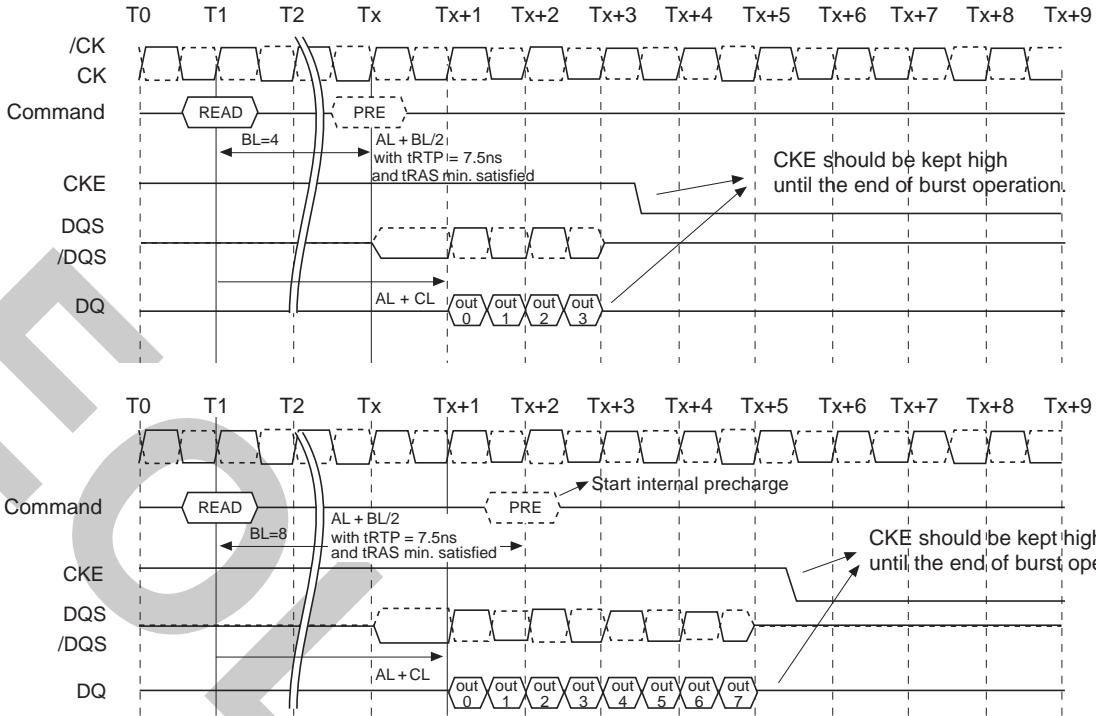
Write to Power-Down Entry
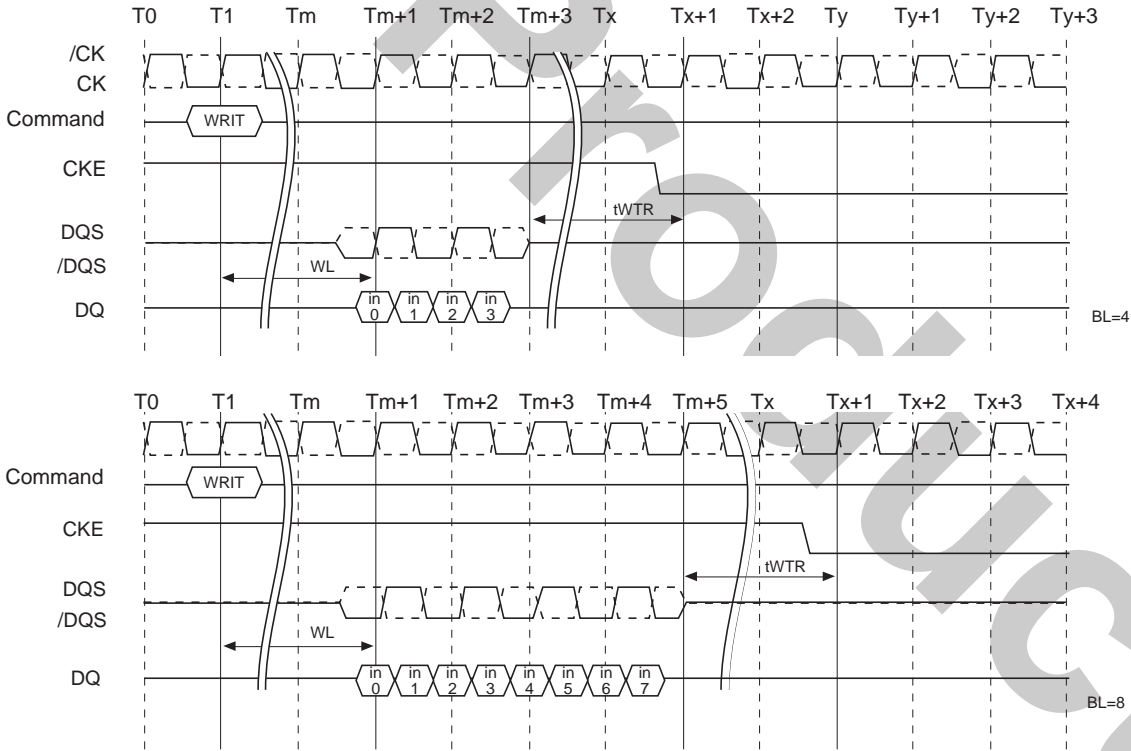
Write with Auto Precharge to Power-Down Entry
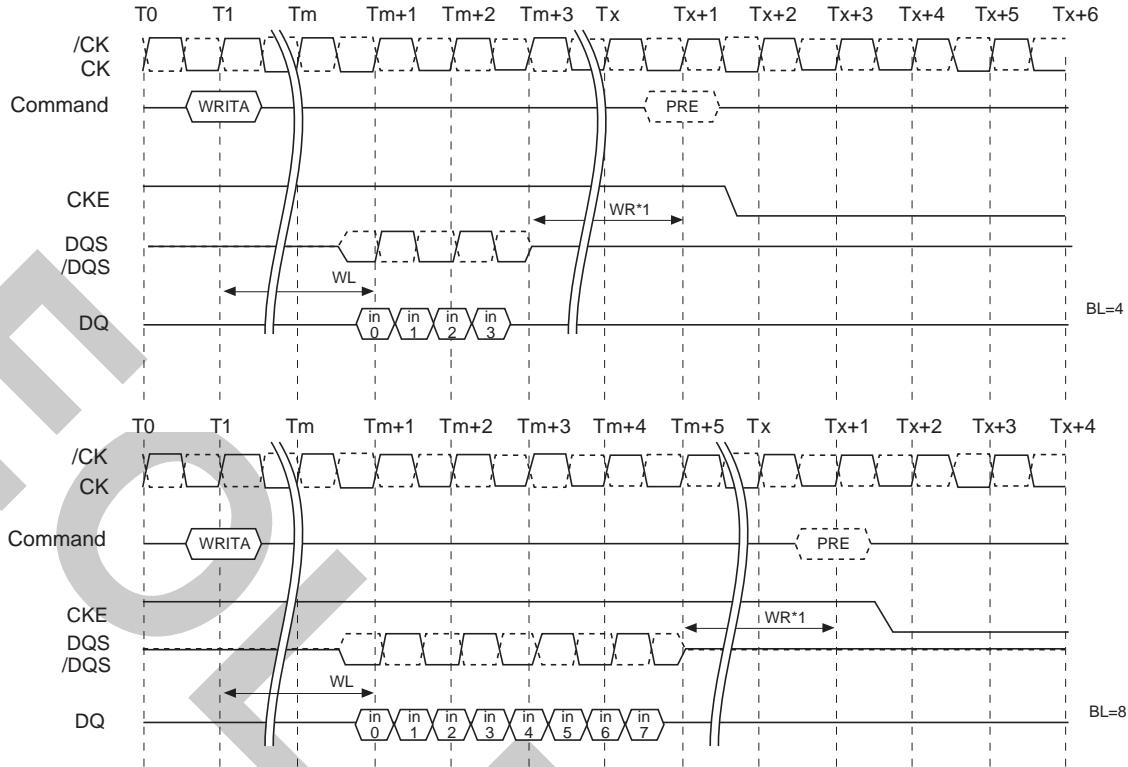
Note: 1. WR is programmed through MRS

Refresh command to Power-Down Entry
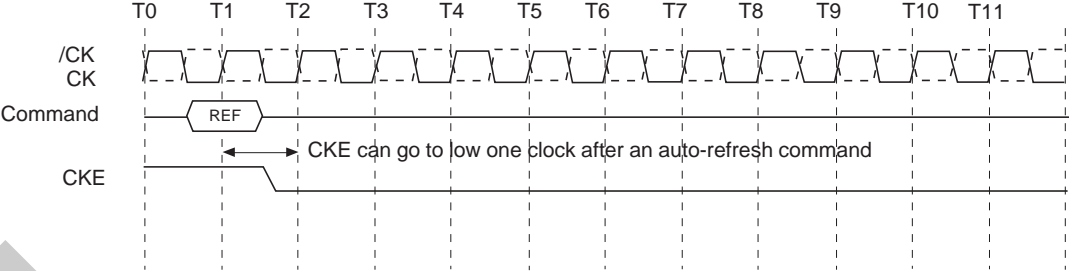
Active command to power down entry
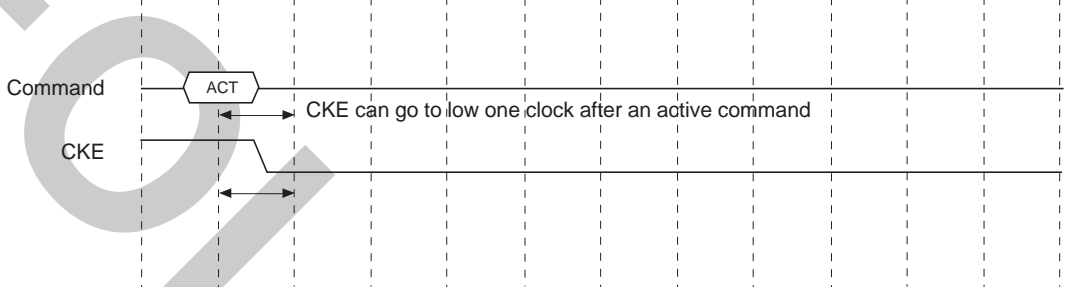
Precharge/Precharge all command to power down entry
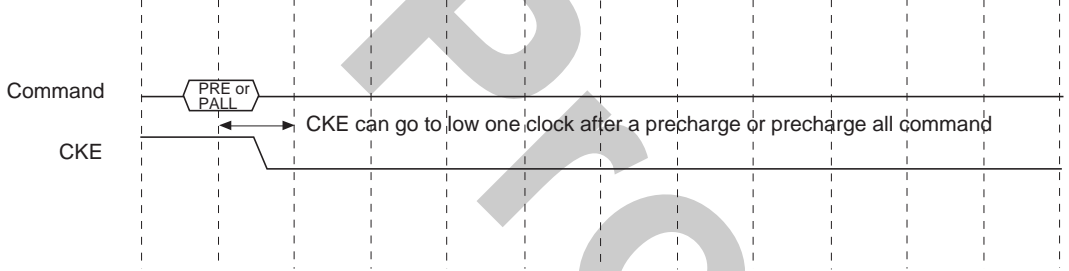
MRS/EMRS command to power down entry
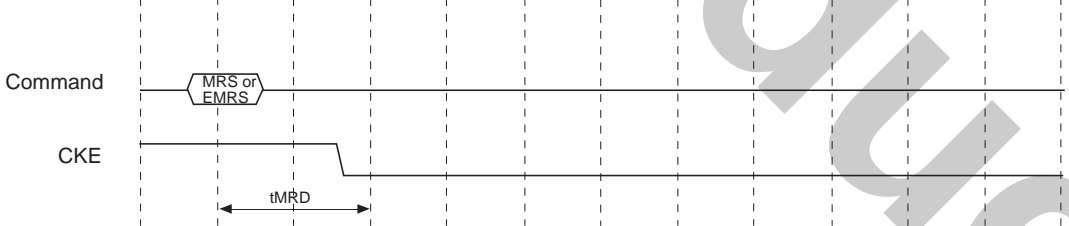
Asynchronous CKE Low Event

DRAM requires CKE to be maintained high for all valid operations as defined in this data sheet. If CKE asynchronously drops low during any valid operation DRAM is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy DRAM timing specification tDELAY before turning off the clocks.

Stable clocks must exist at the input of DRAM before CKE is raised high again. DRAM must be fully re-initialized (steps 4 through 13) as described in initialization sequence. DRAM is ready for normal operation after the initialization sequence. See AC Characteristics table for tDELAY specification

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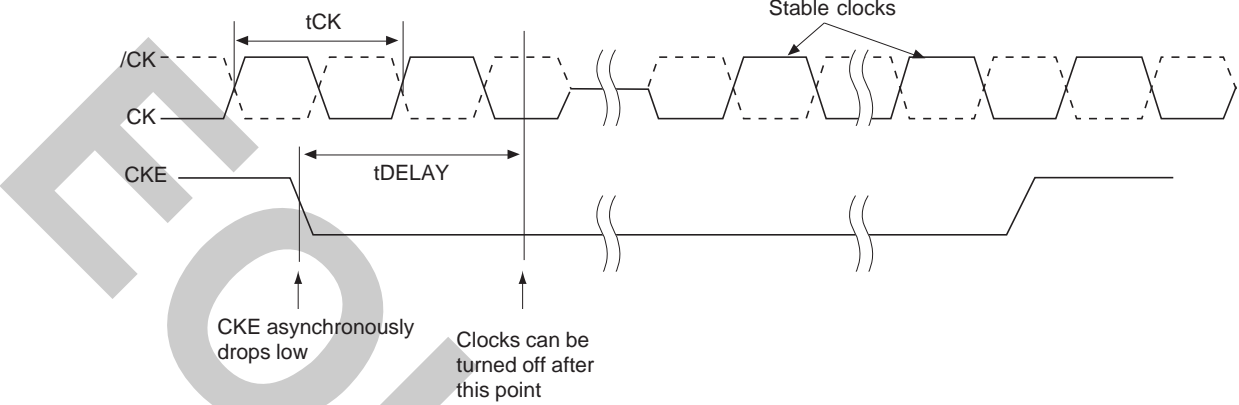
Input Clock Frequency Change during Precharge Power Down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic low level. A minimum of 2 clocks must be waited after CKE goes low before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable low levels.

Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via EMRS after precharge power down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL and soon. During DLL relock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency.

Clock Frequency Change in Precharge Power Down Mode
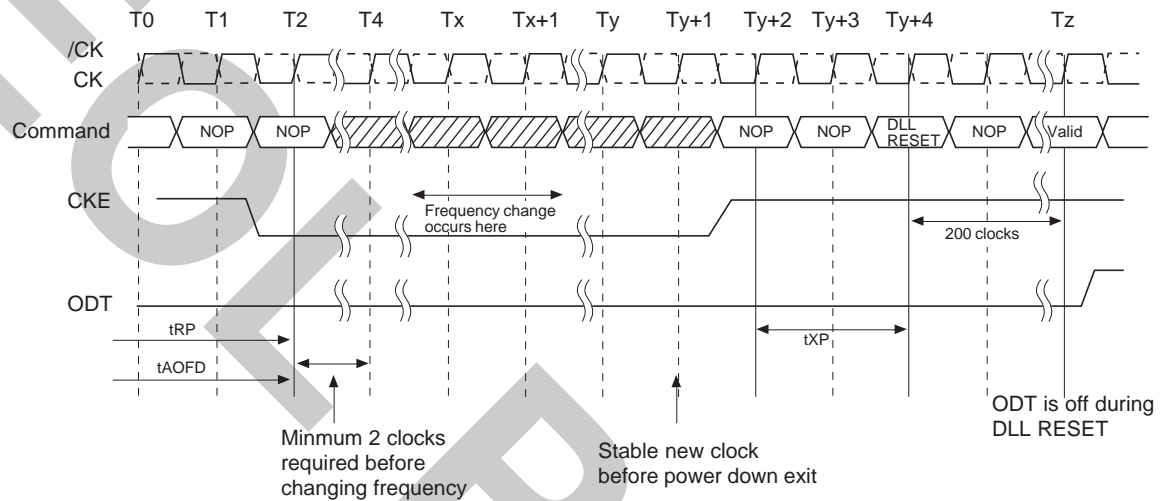
Burst Interruption
Interruption of a burst read or write cycle is prohibited.

No Operation Command [NOP]
The no operation command should be used in cases when the DDR2 SDRAM is in an idle or a wait state. The purpose of the no operation command is to prevent the DDR2 SDRAM from registering any unwanted commands between operations. A no operation command is registered when /CS is low with /RAS, /CAS, and /WE held high at the rising edge of the clock. A no operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command [DESL]
The deselect command performs the same function as a no operation command. Deselect Command occurs when /CS is brought high at the rising edge of the clock, the /RAS, /CAS, and /WE signals become don't cares.

Package Drawing

64-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm

ECA-TS2-0091-01

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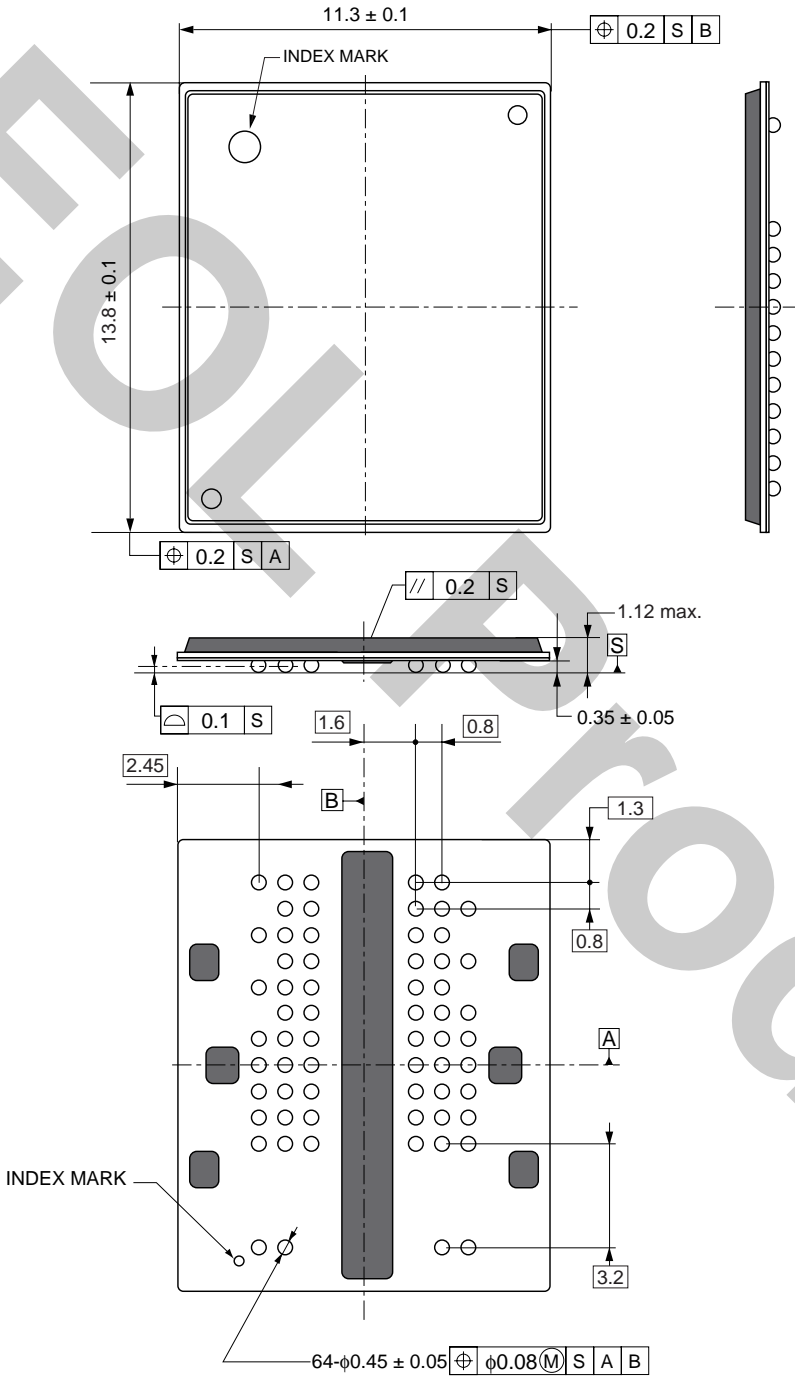
Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDE51XXABSE.

Type of Surface Mount Device

EDE5108ABSE: 64-ball FBGA < Lead free (Sn-Ag-Cu) >

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─────────── **NOTES FOR CMOS DEVICES** ───────────

① **PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107