Single-chip Type with Built-in FET Switching Regulator Series

High-efficiency Step-up Switching Regulator with Built-in Power MOSFET

BD9641NUV

No.09027EAT27

●Description

BD9641NUV is synchronous rectification 1ch boost Switching converter built in Power MOS FET. Input voltage is 2.5V～5.5V. Low power consumption can be achieved. And, because Back-gate control function is built-in, the load can be isolated from the input without external FET in shutdown mode.

●Features

1) PWM synchronous rectification method
2) Input voltage is 2.5V～5.5V
3) Switching frequency is 900kHz.
4) Built in under voltage lockout function
5) Built in protection circuit(short-circuit protection,Thermal shutdown)
6) Built in back gate control function
7) Output voltage can be set by external resistance.
8) Built in power MOS FET transistor
9) Built in soft start function
10) VSON010V3030 package

●Application

- For DSC/DVC motor
- For cellular phone
- For application using lithium cell

●Absolute maximum rating(Ta=25[℃])

Item	Symbol	Rating	Unit
Power-supply voltage	VBAT	-0.3～7	V
Power Dissipation	Pd	700※1	mW
Operating temperature range	Topt	-20～+70	℃
Storage temperature range	Tstg	-55～+150	℃
SW terminal current	Isw	1.8※2	A
Terminal allowable voltage	V_{IN}	-0.3～7	V
Junction temperature	Tjmax	+150	℃

※1 Derating in done 5.6[mW/℃] for operating above Ta=25 [℃].
(Mount on 1-layer 70.0[mm]×70.0[mm]×1.6[mm] board.)
※2 Do not exceed Pd.

●Operationg condition (Ta= -20～+70[℃])

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Power-supply voltage	VBAT	2.5	3.7	5.5	V
Output voltage setting range	VOUT	2.8	5	5.5	V

●Electric characteristics (Unless otherwise specified. VBAT=3.7[V], Ta=25[℃])

Item	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
[Device]						
Current consumption	ICC	-	0.9	1.8	mA	VBAT=3.7[V], No load
Shutdown current	ICCOFF	-	0	10	μA	VBAT=3.7[V],XSHDN=GND
XSHDN input current	IIH	4.63	9.25	18.5	μA	XSHDN Voltage=3.7[V]
[Step-up DC/DC blobk]						
Soft start time	TSOFT	1.25	2.5	5.0	ms	VOUT=5[V] 85%
FB terminal voltage	VFB	0.39	0.40	0.41	V	
Oscillation frequency	FOSC	675	900	1125	kHz	
Max duty cycle	DMAX	76.5	85	93.5	%	
PMOS ON resistance	RONP	-	0.4	0.65	Ω	VOUT=5[V]
NMOS ON resistance	RONN	-	0.35	0.60	Ω	VOUT=5[V]
[Voltage drop detection Block]						
UVLO Detecting voltage	VUVLO1	2.05	2.15	2.25	V	
UVLO Return voltage	VUVLO2	2.10	2.20	2.30	V	
[XSHDN block]						
XSHDN H Input voltage	VIH	1.5	-	-	V	VBAT=2.5～5.5[V]
XSHDN L Input voltage	VIL	-	-	0.3	V	
[GND short detection Block]						
Timer latch time	TLATCH	0.35	0.7	1.4	ms	
GND short detection voltage	VSHORT	0.1	0.2	0.3	V	

●Reference data(Unless otherwise noted, Ta=25[℃])

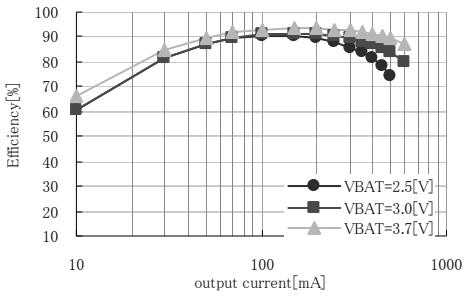


Fig.1 Output current - Efficiency characteristic
(5.015[V] Output voltage setting)
Efficiency= 94% (150mA)

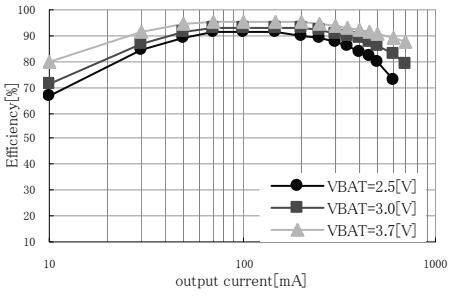


Fig.2 Output current - Efficiency characteristic
(4.2[V] Output voltage setting)
Efficiency = 96% (150mA)

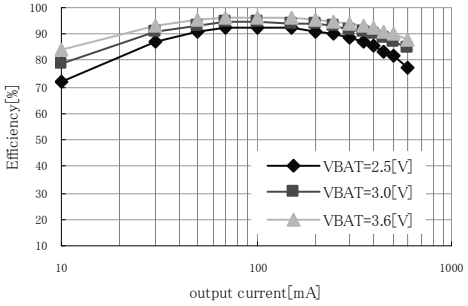


Fig.3 Output current - Efficiency characteristic
(3.6[V] Output voltage setting)
Efficiency = 95% (100mA)

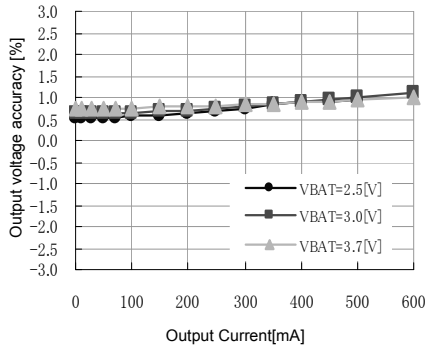


Fig.4 Output current－
Output voltage accuracy characteristic
(5.015[V] Output voltage setting)

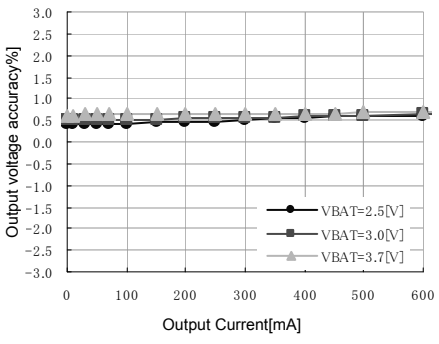


Fig.5 Output current－
Output voltage accuracy characteristic
(4.2[V] Output voltage setting)

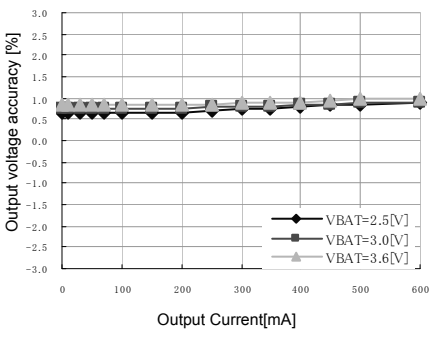
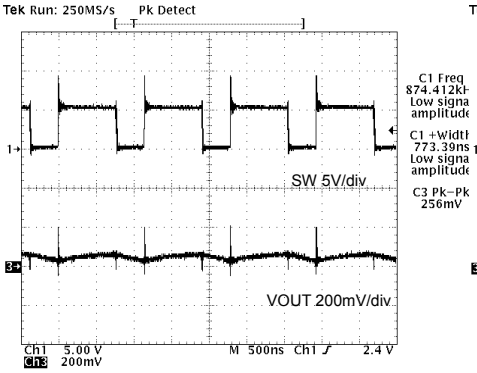
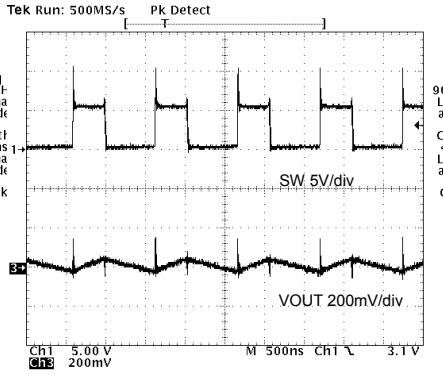


Fig.6 Output current－
Output voltage accuracy characteristic
(3.6[V] Output voltage etting)



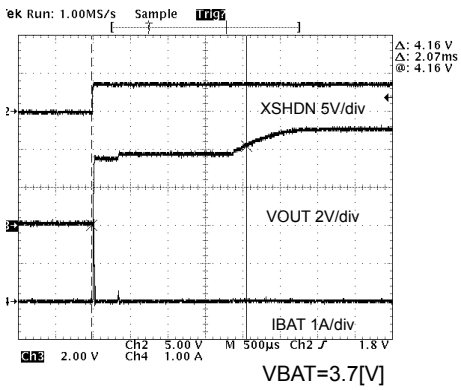
VBAT=3.7[V]
VOUT=5.015[V]
IOUT=400[mA]

Fig.7 Output voltage wave form



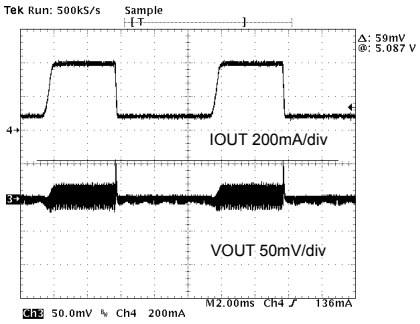
VBAT=2.5V
VOUT=5.015[V]
IOUT=400[mA]

Fig.8 Output voltage wave form



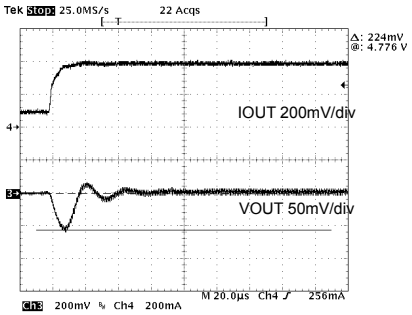
VBAT=3.7[V]
VOUT =5.015[V]
IOUT=0[mA]

Fig.9 Start wave form



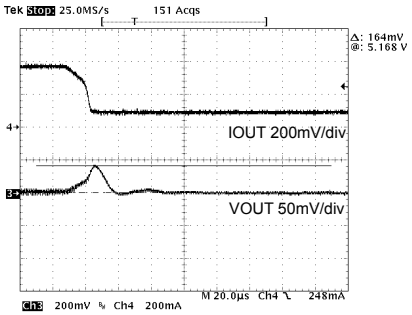
VBAT=3.7[V]
VOUT=5.015[V]
IOUT=100[mA] ⇔ 400[mA]

Fig.10 Load transient response wave form



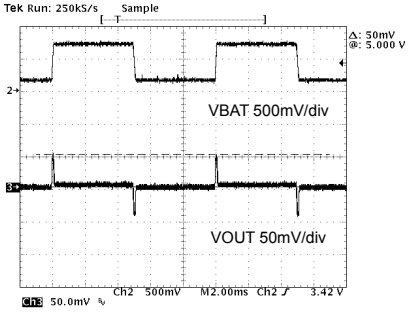
VBAT=3.7[V]
VOUT=5.0VIT=100[mA]→4
00[mA]

Fig.11 Load transient response wave form



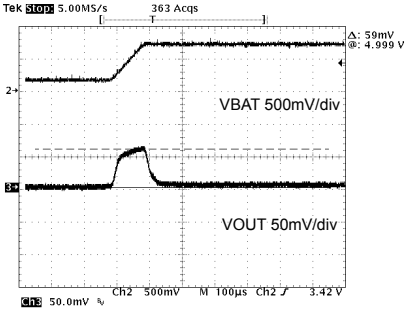
VBAT=3.7[V]
VOUT=5.015[V]
IOUT=400[mA]→100[mA]

Fig.12 Load transient response wave form



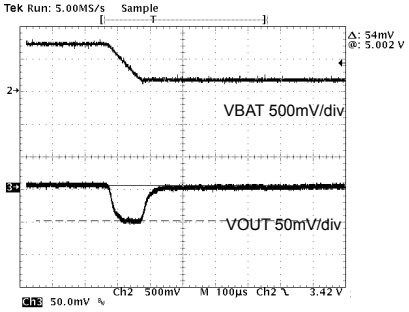
VBAT=3.1[V]⇔3.7[V]
VOUT=5.015[V]
IOUT=0[mA]

Fig.13 Power-line transient response wave form



VBAT=3.1[V]→3.7[V]
VOUT=5.015[V]
IOUT=0[mA]

Fig.14 Power-line transient response wave form



VBAT=3.7[V]→3.1[V]
VOUT=5.015[V]
IOUT=0[mA]

Fig.15 Power-line transient response wave form

●Block Diagram

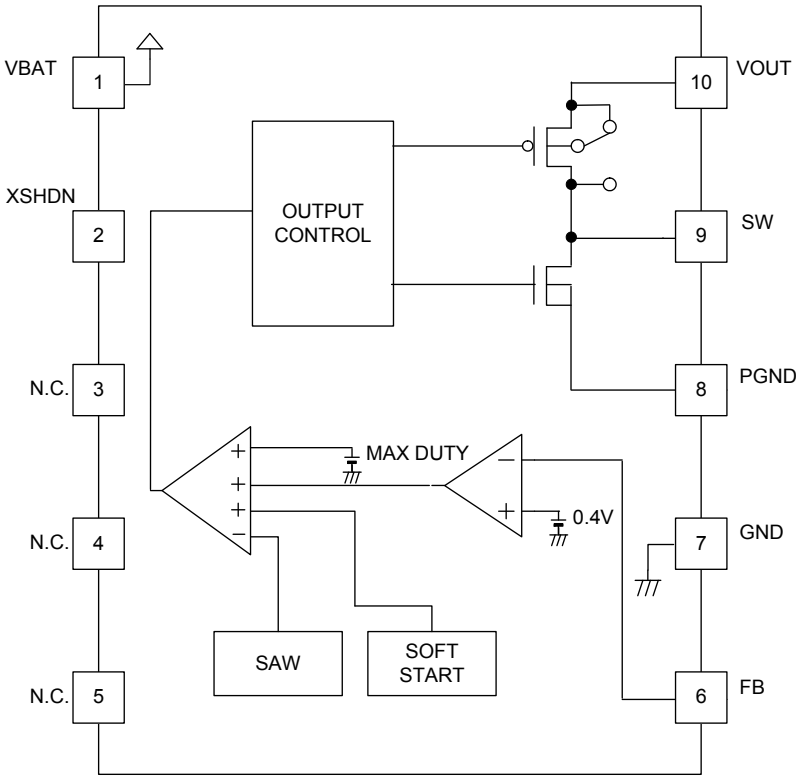
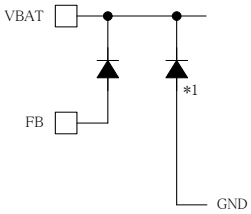
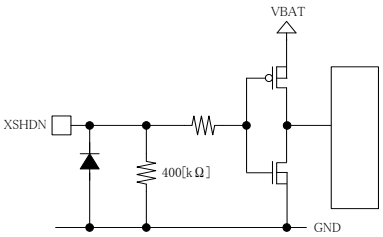
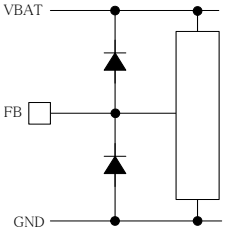
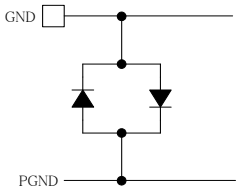
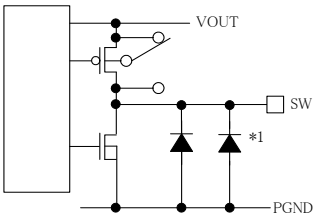
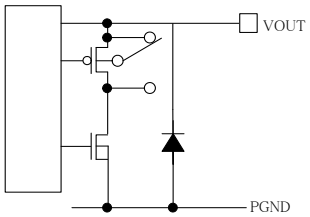


Fig.13 Block Diagram

●Pin layout and function

Terminal No	Terminal Name	Function
1	VBAT	Power supply input terminal
2	XSHDN	Chip shut down terminal (Shut down at XSHDN=GND)
3	N.C.	
4	N.C.	
5	N.C.	
6	FB	Feed back terminal
7	GND	GND terminal
8	PGND	GND terminal for power MOS
9	SW	Switching terminal
10	VOUT	DC/DC converter output voltage terminal

●Description of input / output terminal

Terminal No.	Terminal Name	Equivalent Circuit	Function
1	VBAT		Power input terminal *1 Clamp for protecting from E.S.D
2	XSHDN		TTL level input terminal *1 Clamp for protecting from E.S.D
6	FB		Analog input terminal
7,8	GND PGND		GND terminal
9	SW		Power MOS driver for synchronous rectification *1 Clamp for protecting from E.S.D
10	VOUT		DC/DC output terminal *1 Clamp for protecting from E.S.D

●Functional Description

1. DC/DC converter

The device integrates Power MOS FET to realize a synchronous rectifier.
The device begins starting up with the soft start when XSHDN=H and VBAT rises to UVLO return voltage (2.20[V] typ) built-in this IC (Fig.14).
According to the load, the PWM duty is kept variable and the output voltage are kept constant.
The device needs inductor and capacitor for boost, bypass capacitor between power supply and GND, resistance divider and capacitor at the feedback loop.
The maximum output load current is 530mA. (Input voltage 2.9V or more)

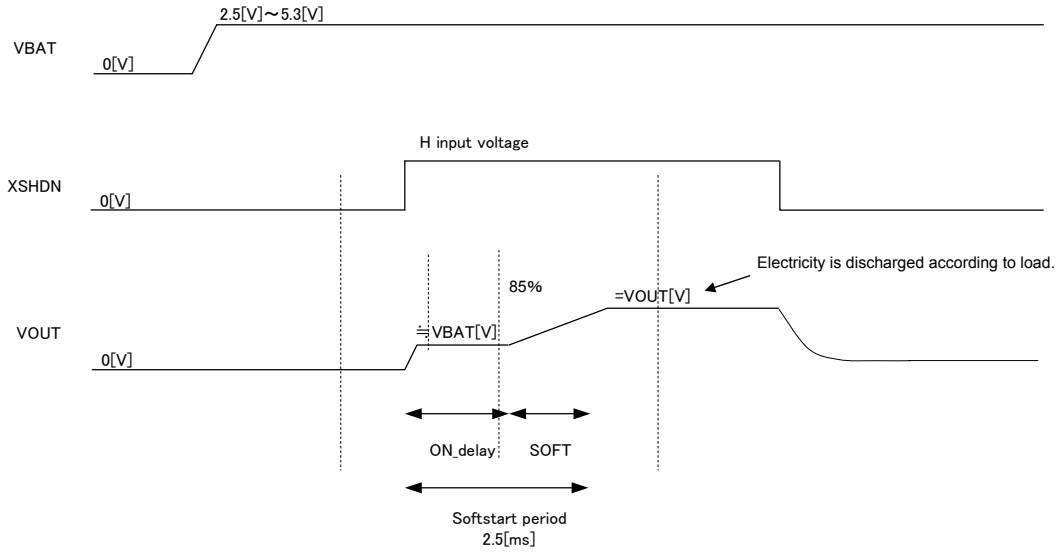
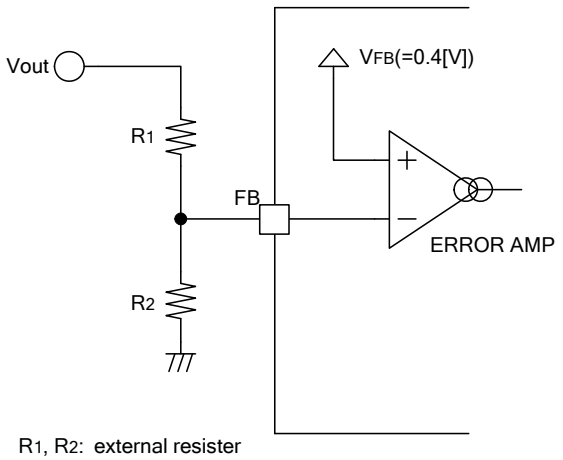


Fig.14 DC/DC converter start wave form

2. About output voltage setting

Output voltage of DC/DC converter is shown by the following expressions.

$$Vout = \frac{R1 + R2}{R2} \times V_{FB} \qquad (V_{FB}=0.4V)$$



R1, R2: external resister
VFB: internal reference voltage(=0.4[V])

Fig.15 Output voltage setting

3. Back gate control function

Back gate control function is built into the IC. It can be isolated VOUT from the power supply.
Back gate control function is a function to intercept the output by connecting the back gate of PMOS with the SW side at XSHDN=L (shutdown) and timer latch.

4. Shut down function
The device becomes shutdown condition when XSHDN terminal is GND. Then, the back gate of PMOS is connected to the SW side by the function of back gate control, and the VOUT output is isolated from the power supply.
The device becomes normal operation after the soft start when XSHDN terminal is VBAT.
The VBAT terminal and the XSHDN terminal must be used by below condition with start-up.

Shut down release wave form of BD9641NUV IC

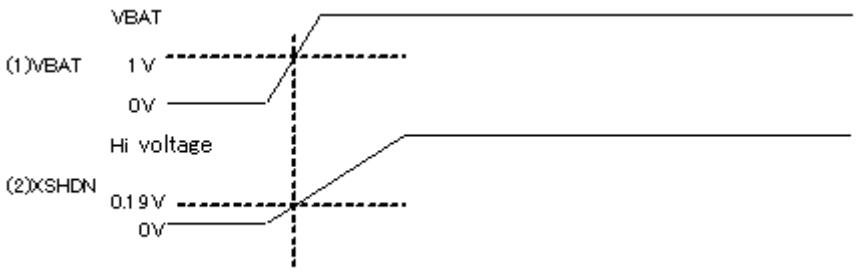


Fig.16 Start-up operation

CONDITION : (1) The time when VBAT reaches 1V
(2) XSHDN is less than 0.19V

For example, when VBAT and XSHDN is rised voltage at once, the device is set CR for rising time of VBAT to insert CR filter such as Fig.17.

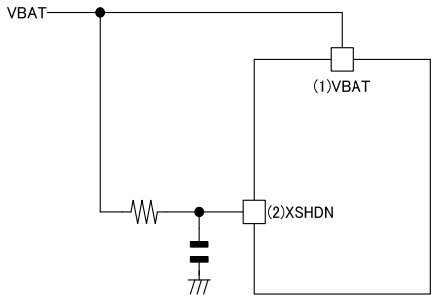


Fig.17 Example of external circuit

5. Thermal shutdown function
The switching is stopped when the temperature of the chip rises in addition exceeding Tjmax, and both PMOS and NMOS of the SW output are turned off.
It usually returns to operation after software starts again when the temperature of the chip decreases.

6. UVLO function
If VBAT voltage is less than 2.15[V](typ.), switching is stopped so as to prevent irregular operation of IC due to under voltage, and PMOS and NMOS of SW terminal turns off. If VBAT voltage return to over 2.20[V](typ.), the shutdown function is released, and it is restarted.

●Ground short circuit protection function
FB terminal voltage is watched. If it is less than detected voltage of ground short circuit protection(0.2[V]typ.), timer circuit of IC operates. When the condition continues into 0.7[ms] by timer latch circuit, the device latches with Power NMOS off.
Then backgate control of IC is worked VOUT output is isolated from the power supply.
The release of latch are XSHDN=GND or restart-up of the power source.

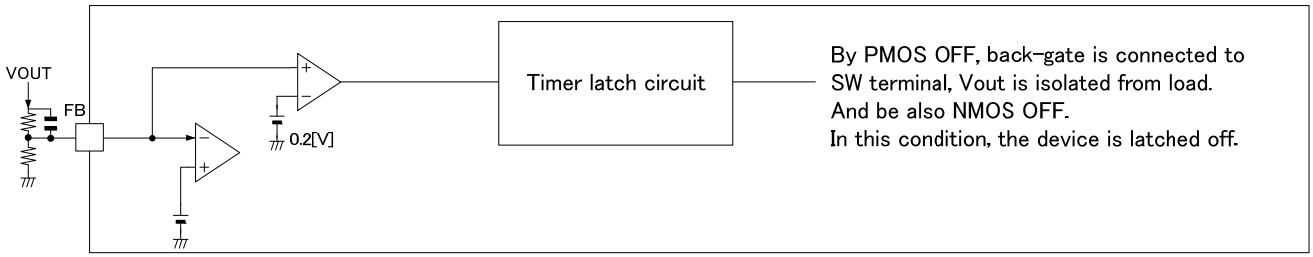


Fig.18 Ground short circuit protection function

●Application circuit figure

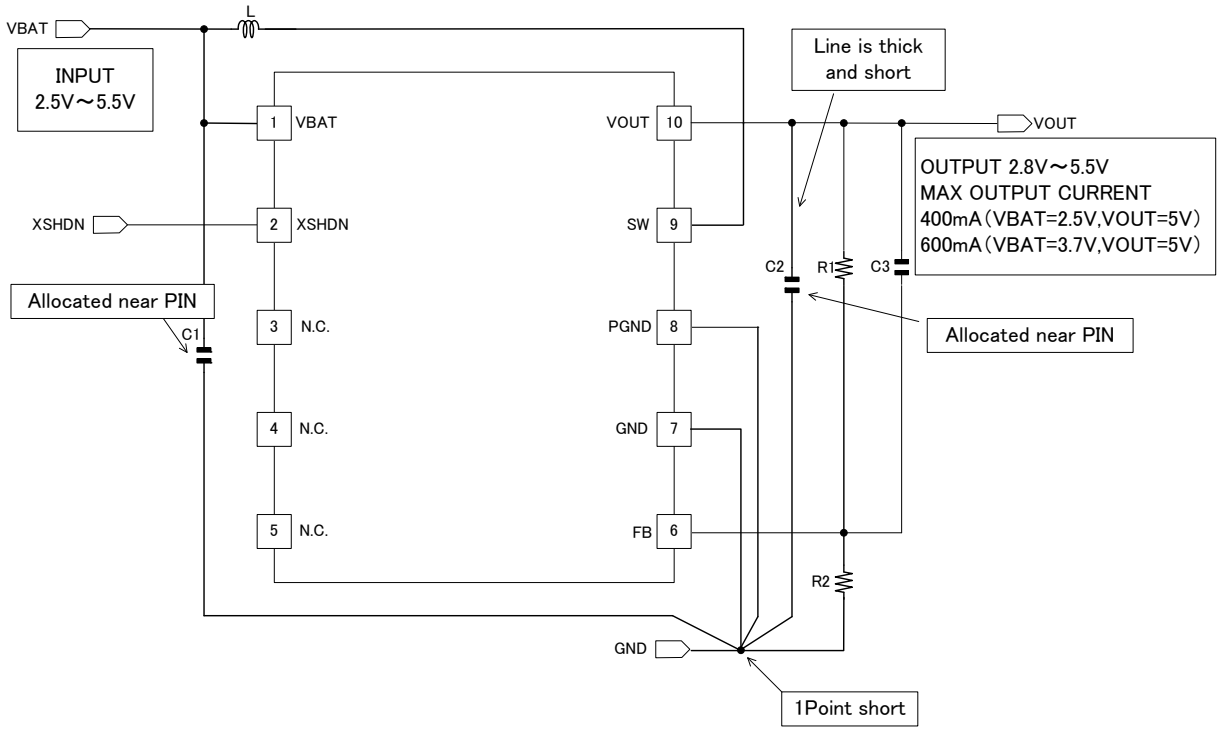


Fig.19 Application circuit figure

○Constant of external parts (recommend value) Case of output voltage is 5.015[V]

Recommended inductor

	Maker	Part number	Inductance
L	Taiyo Yuden	NR4018T3R3M	3.3μH

The peak current of the inductor does not to exceed allowable current of inductor, please.

Recommended capacitor

	Maker	Part number	Inductance
C_1	Taiyo Yuden	LMK212BJ106MG	10μF
C_2	Taiyo Yuden	JMK107BJ106KG	10μF
C_3	Taiyo Yuden	TMK063CH680JP	68pF

Resistor value

	Resistor value
R_1	150kΩ
R_2	13kΩ

Output voltage VOUT：

$$VOUT = \frac{R_1 + R_2}{R_2} \times 0.4\ [V]$$

It is decided, the accuracy of output voltage is changed by resister accuracy of R1, R2.

●Notes for Use

1. About PCB layout
   - ・VBAT terminal must connect to the power supply on the board.
   - ・PGND,GND must be connected to ground on the board.
   - ・The line of VBAT, PGND, GND terminal is thick and short, and the impedance is low, please.
   - ・Please stick the bare pad of reverse package to the board with solder to GND pattern on the PCB. In the case of unconnected, head radiation characteristics is fallen and package power (permissible dissipation)is fallen.
   - ・The output voltage of DC/DC converter draw from both ends of capacitor near output ,please.
   - ・DC/DC converter is affected the performance according to board pattern or neighboring parts. So please consider the design of neighboring circuit.

2. About neighboring circuit
   - ・Please use ceramic capacitor of low ESR to bypass capacitor between power supply and GND. And allocate it to as near as possible to the pin.
   - ・Please allocate external parts such as inductor , capacitor and so on, as near as possible to IC.
   - ・Please draw output voltage from the both ends of capacitor. Especially, please connect the wire which is run large current thick and short.
   - ・Because of output short of CH1, over current run to the external diode, it is possible to destroy IC. Please not to run over current by the physical provision such as using Poly-switch, fuse and so on.

3. About start-up
   - ・Please keep light load when starting-up IC.

4. Notes for absolute maximum rating
   - ・Exceeding supply voltage and operating Temp over Absolute Maximum Ratings may cause degradation of IC and even may destroy the IC. if special mode such that exceeding Absolute Maximum Ratings is expected, please have safe countermeasure such as adding POLY SWITCH and fuse to avoid from over stressing.

5. Notes for heat design
   - ・Do not exceed the power dissipation (PD) of the package specification rating under actual operation.

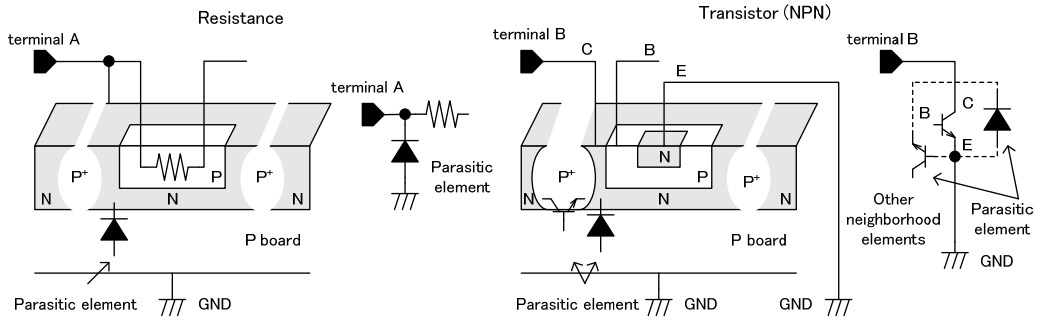
6. Short circuit mode between terminals and wrong mounting
   - ・While mounting IC on the board, check direction and position of the IC. If inadequately mounted, the IC may destroy. Moreover this IC might be destroyed when dust short the terminals between pins or pin and ground. Avoid the VOUT-GND short-circuit.
7. Radiation
   - ・Strong electromagnetic radiation can cause operation failures.

8. Notes for Thermal shutdown (TSD)
   - ・Main purpose of TSD is to shutting IC down from runaway effect. It is not to compensate or to protect set device. Therefore, please do not continuously operate the IC after TSD circuit is activated and/or premise operations such that TSD circuit function being used.

9. Notes for test of mounted print board
   - ・While connecting capacitor to Low impedance pins, please discharge capacitor by one process by another to prevent stressing the IC. While mounting and removing the IC to/from the Board in the inspection process, be sure to turn off the power supply at each actions. Moreover equip ground earth in assembling process for ESD protection and handle with care during the test and/or transportation.

10. Notes for each input terminal

・This IC is a monolithic IC, and has P^+ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by applying lower voltage than GND (P substrate) to input terminals. Moreover, please apply each input terminal with lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage being applied.



Example of simple structure of IC

11. Used application

・The IC is designed for DSC/DVC.

・Please consult with sales representative when you consider using to the machine, device except above application.

●Power Dissipation

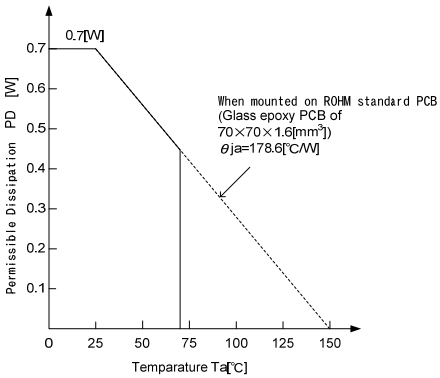


Fig.20 Permissible Dissipation

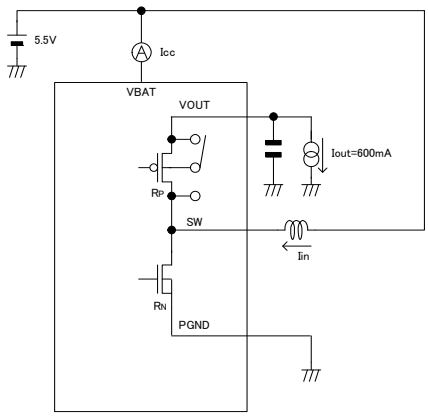


Fig.21 About calculation of permissible dissipation

・Example of calculate of power dissipation
(Input voltage=2.5[V], Output voltage=5.5[V], Output current=400[mA])

・The loss of Power Tr : Pd(DC)
(Rp:PMOS ON resistance R_N:NMOS ON resistance D:Switching duty of SW terminal η:Efficiency)

$$Pd(DC) = (Rp \times (1 - D) + Rn \times D) \times Iin^2 \times \frac{1 - \eta}{\eta}$$

$$= \{Rp \times (1 - D) + Rn \times D\} \times (Iout \times Vout / Vin)^2 \times \frac{1 - \eta}{\eta}$$

$$= \{0.65 \times (1 - 0.7) + 0.6 \times 0.7\} \times (0.4 \times 5.5 / 2.5)^2 \times \frac{1 - 0.7}{0.7}$$

$$= 0.615 \times 0.7744 \times \frac{1 - 0.7}{0.7} = 0.204(W)$$

・The loss of internal consumed power of IC : Pd(Icc)
Pd(Icc)=Vcc×Icc (Vcc：power supply voltage Icc：Consuming current)
=5.5×0.001=0.0055

Therefore, the power dissipation caused in IC : Pd=Pd(DC)+Pd(Icc)=0.210(W)

Please examine the design of circuit not to exceed the power dissipation described.

(*) Please connect surely the bare pad of reverse package to the board to use solder.

●Ordering Name Selection

B	D	9	6	4	1	N	U	V	-	E	2

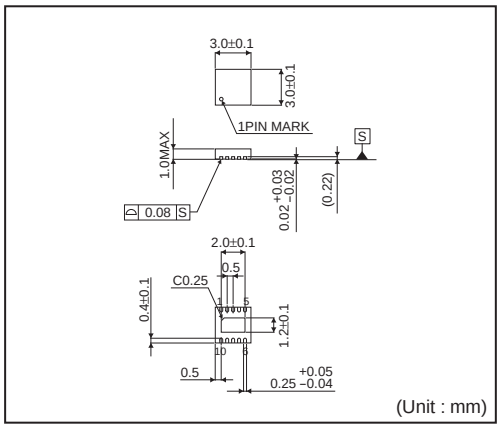
Part No. (BD)

Part No. (9641)

Package
NUV: VSON010V3030

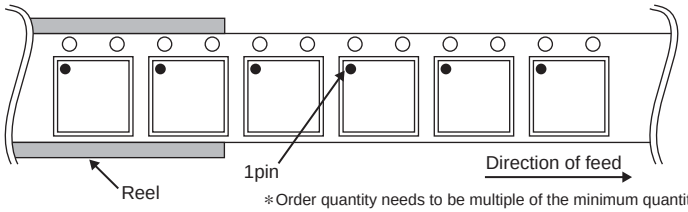
Packaging and forming specification
E2: Embossed tape and reel
(VSON010V3030)

VSON010V3030



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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