EN71NS128B0 Base MCP
Stacked Multi-Chip Product (MCP) Flash Memory and RAM
128 Megabit (8M x 16-bit) CMOS 1.8 Volt-only Simultaneous Operation Burst Mode Flash Memory and
32 Megabit (2M x 16-bit) Pseudo Static RAM

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7V to 1.95V**
- **High performance**
  - 70 ns @ random access
  - 7 ns @ burst access (108MHz)
- **Package**
  - 8 x 9.2mm 56 ball FBGA
- **Operating Temperature**
  - 25°C to +85°C

General Description

The EN71NS series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- E29NS128 (Burst mode) Flash memory die.
- Pseudo SRAM.

For detailed specifications, Please refer to the individual datasheets listed in the following table.

Device	Document
NOR Flash	EN29NS128
Pseudo SRAM	ENPSS32

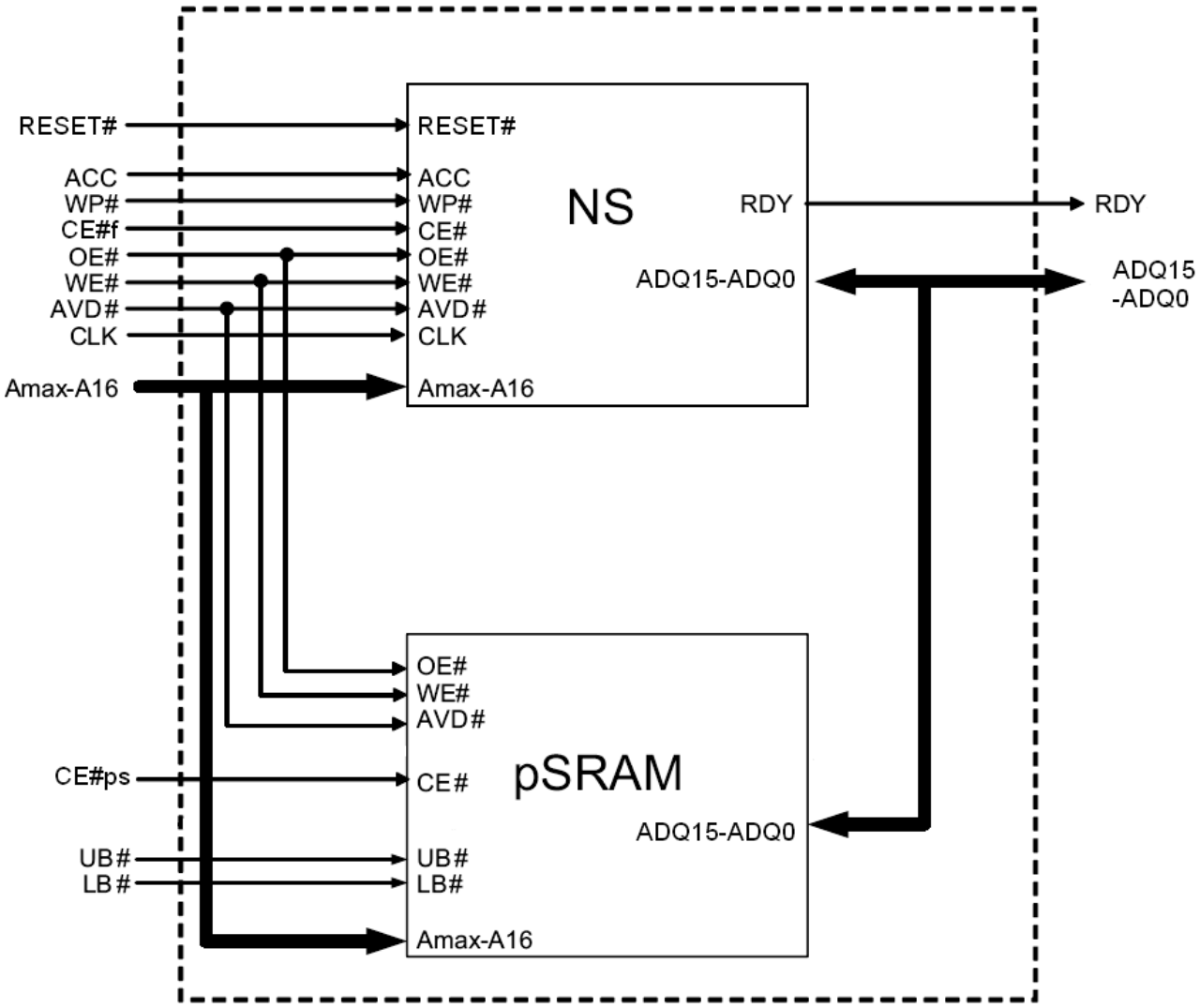
Product Selector Guide

128 Mb Flash Memories

Device-Model#	EN71NS128B0	**pSRAM density**	32M pSRAM
Flash Access time	70ns at Async. Mode 7ns at Burst Read	**pSRAM Access time**	70ns at Async. Mode 7ns at Burst Read
pSRAM Burst mode max frequency	108MHz	**pSRAM Burst mode max frequency**	108MHz
Package	56-ball FBGA		

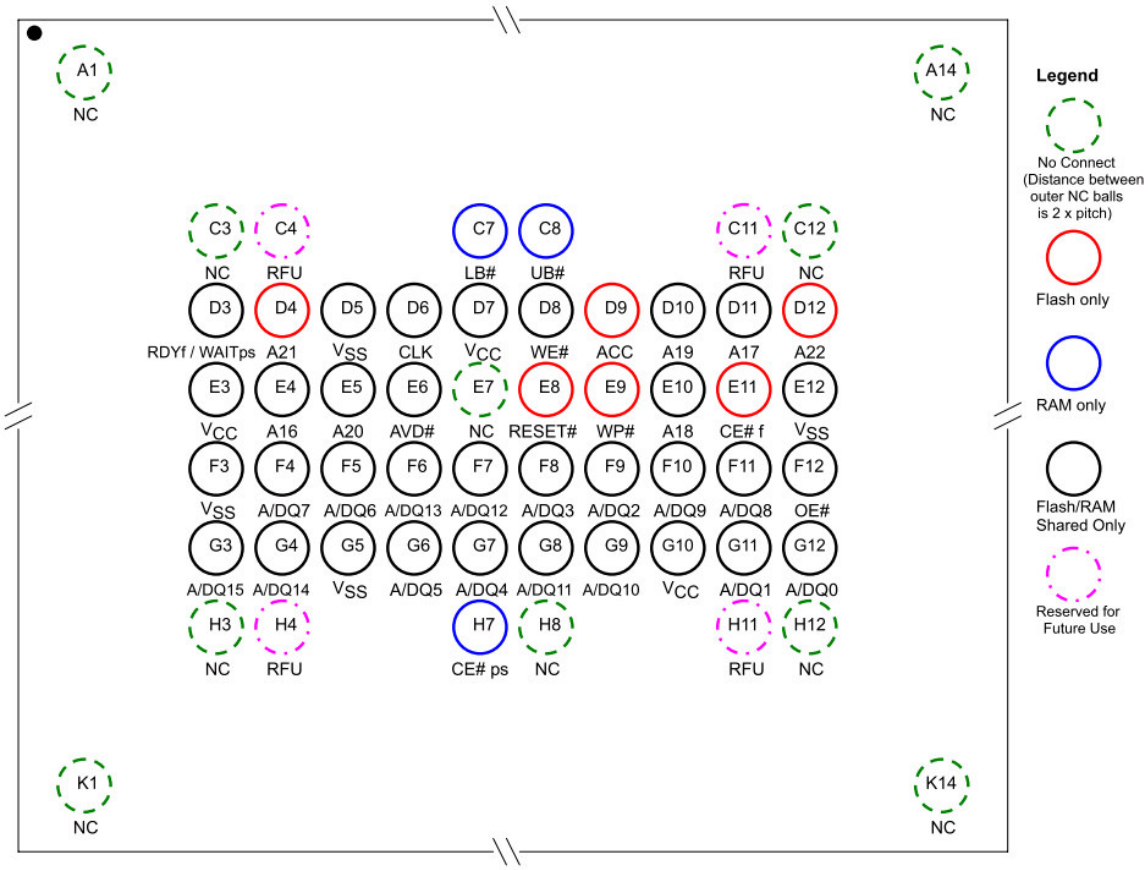
MCP Block Diagram

NOR FLASH + PSRAM DIAGRAM



Note: Amax = A22

Connection Diagram



MCP	Flash-only Addresses	Shared Addresses	Shared ADQ Pins
EN71NS128B0	A22 – A21	A20 – A16	ADQ15 – ADQ0

Pin Description

Signal	Description
A22–A16	Address Inputs
A/DQ15–A/DQ0	Multiplexed Address / Data input / output
CE#	Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE#	Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE#	Write Enable Input.
VCCQ/VCC	Device Power Supply (1.65 V–1.95 V).
VSSQ/GND	Ground
NC	No Connect; not connected internally
RDY	Ready output; indicates the status of the Burst read. V_{OL} = data invalid, V_{OH} = data valid.
CLK	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits A21–A16 are address only). V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH} = device ignores address inputs
RESET#	Hardware reset input. V_{IL} = device resets and returns to reading array data
WP#	Hardware write protect input. V_{IL} = disables writes to SA129-130. Should be at V_{IH} for all other conditions.
ACC	At 11 V, accelerates programming; automatically places device in Accelerated Program mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions. (Applying high voltage on MCP package is prohibited; otherwise, internal RAM may be damaged easily!)
CRE	Control register enable: when CRE is high, WRITE operations laod the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
LB#	Lower byte enable. DQ7~DQ0
UB#	Upper byte enable. DQ8~DQ15
WAIT	Provides data-valid feedback during burst READ and WRITE operations, WAIT is used to arbitrate collisions between refresh and wrapping within the burst length. WAIT should be ignored during asynchronous operation. WAIT is High-Z when CE# is HIGH

Operating Mode (For Asynchronous mode)

Mode	CLK	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT	A19/A18	A/DQ[0:15]	Power
READ	X	⌐¬	L	L	H	L	L	Low-Z	X	Data out	Active
WRITE	X	⌐¬	L	X	L	L	L	High-Z	X	Data in	Active
Standby	H or L	X	H	X	X	L	X	High-Z	X	High-Z	Standby
No operation	X	X	L	X	X	L	X	Low-Z	X	X	Idle
Configuration register WRITE	X	⌐¬	L	H	L	H	X	Low-Z	CRE code	OP Code	Active
Configuration register READ	X	⌐¬	L	L	H	H	L	Low-Z	CRE code	Config. reg. out	Active

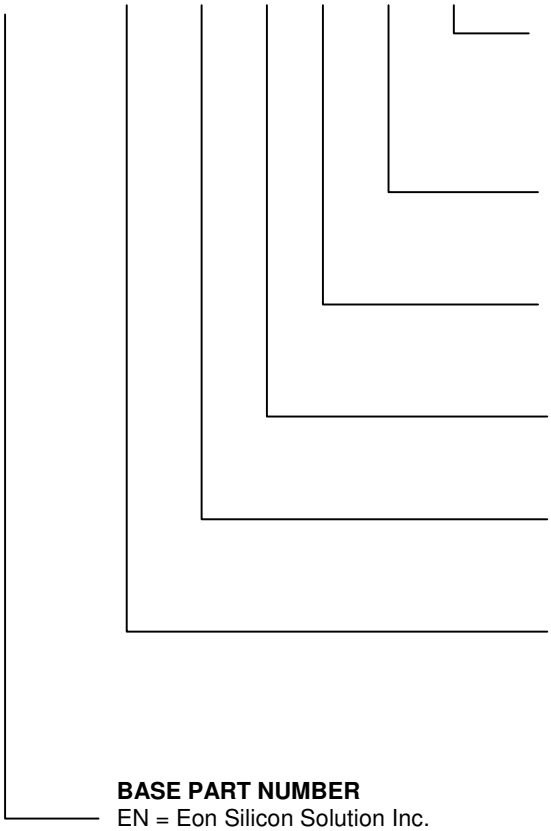
Operating Mode (For Synchronous Burst mode)

Mode	CLK	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT	A19/A18	A/DQ[0:15]	Power
Asynchronous READ	H or L	⌐¬	L	L	H	L	L	Low-Z	X	Data out	Active
Asynchronous WRITE	H or L	⌐¬	L	X	L	L	L	High-Z	X	Data in	Active
Standby	H or L	X	H	X	X	L	X	High-Z	X	High-Z	Standby
No operation	H or L	X	L	X	X	L	X	Low-Z	X	X	Idle
Initial burst READ	⌐¬	L	L	X	H	L	L	Low-Z	X	Address	Active
Initial burst WRITE	⌐¬	L	L	H	L	L	X	Low-Z	X	Address	Active
Burst continue	⌐¬	H	L	X	X	X	L	Low-Z	X	Data in or Data out	Active
Configuration register WRITE	⌐¬	L	L	H	L	H	X	Low-Z	CRE code	OP Code	Active
Configuration register READ	⌐¬	L	L	L	H	H	L	Low-Z	CRE code	Config. reg. out	Active

Note: X=don't care. H=logic high. L=logic low. V= Valid data

ORDERING INFORMATION

EN29NS 128 B0 - 7 D W P



PACKAGING CONTENT
(Blank) = Conventional
P = RoHS compliant

TEMPERATURE RANGE
W = Wireless (-25°C to +85°C)

PACKAGE
D = 56-Ball Very Thin Fine Pitch BGA (VFBGA)
0.50mm pitch, 9.2mm x 8mm package

BURST READ ACCESS TIME
7 = 7ns

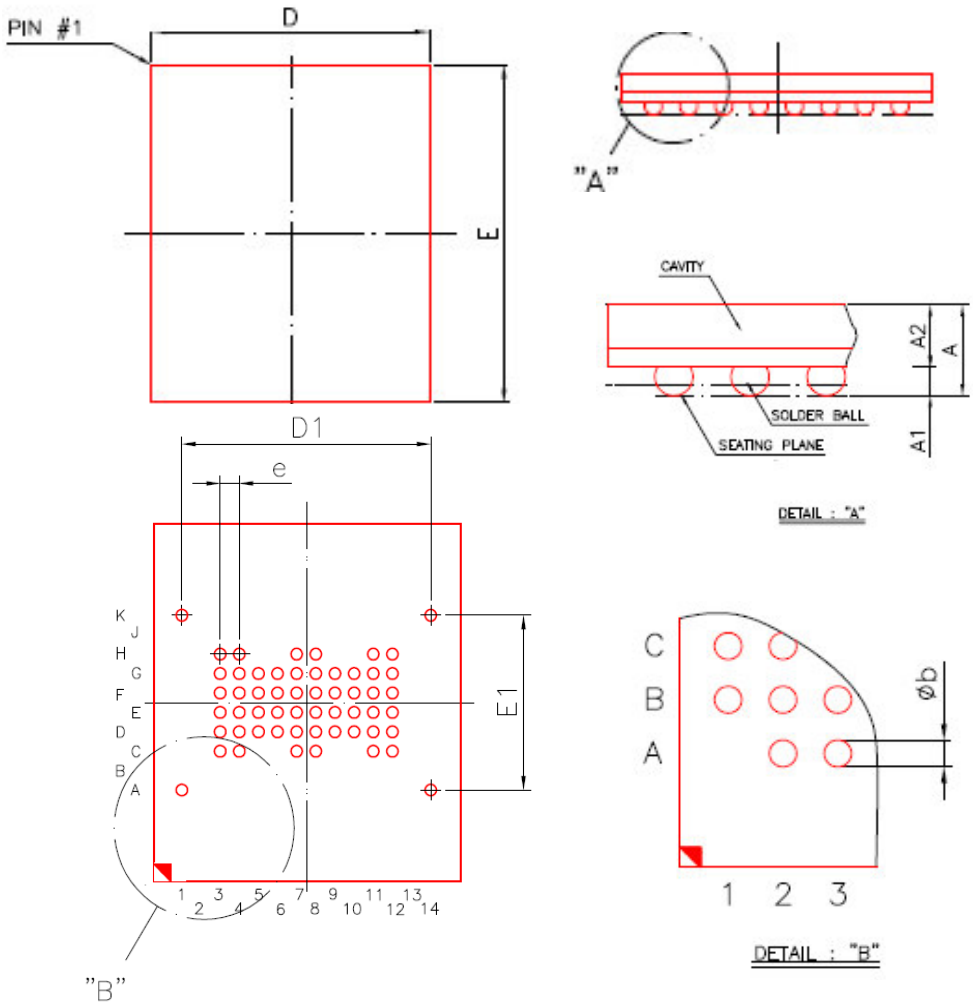
Pseudo SRAM density
B0 = 32Mb

DENSITY
128 = 128Megabit (8M x 16 Bit)

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
29NS = Simultaneous Read/Write, Burst Mode Flash Memory with Multiplexed I/O 1.8V Operation

PACKAGE MECHANICAL

56-ball Thin Fine-Pitch Ball Grid Array (TFBGA) 8 x 9.2 mm Package



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.16	0.21	0.26
A2	0.84	0.89	0.94
D	7.90	8.00	8.10
E	9.10	9.20	9.30
D1	- - -	6.50	- - -
E1	- - -	4.50	- - -
e	- - -	0.50	- - -
b	0.25	0.30	0.35

Note : 1. Coplanarity: 0.1 mm

THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

Revisions List

Revision No	Description	Date
A	Initial Release	2009/07/24