FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12625-3E

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95R203

MB95R203

■ DESCRIPTION

The MB95R203 is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Selectable Main clock source
    Main OSC clock (Up to 10 MHz, Maximum Machine clock frequency is 5 MHz)
    External clock (Up to 20 MHz, Maximum Machine clock frequency is 10 MHz)
    Internal main CR clock (Typ 1 MHz, Machine clock frequency is 1 MHz)
  - Selectable Sub clock source
    Sub OSC clock (32 kHz)
    Sub internal CR clock (Typ : 100 kHz, Min : 50 kHz, Max : 200 kHz)

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2009.8

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- Timer
  - 8/16-bit composite timer
  - Timebase timer
  - Watch prescaler
- UART/SIO
  - Offers clock asynchronous (UART) or clock synchronous (SIO) serial data transfer
  - Full duplex double buffer
- I^2C
  - Built-in wake-up function
- External interrupt
  - Interrupt by the edge detection (Select rising edge/falling edge/both edges)
  - Can be used to recover from low-power consumption modes (also called standby mode)
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolutions can be selected
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Timebase timer mode
- I/O port : Max 16
  - General-purpose I/O ports (Max) :
    CMOS I/O : 12, N-ch open drain : 4
- On-chip debug
  - 1 wire serial control
  - Support serial writing. (Asynchronous mode)
- Hardware/Software watchdog timer
  - Built-in Hardware watchdog timer
- Low voltage detection circuit (LVD)
  - Low voltage detection reset circuit
  - Circuit to monitor FRAM power supply
- Clock supervisor counter (CSV)
  - Built-in Clock supervise function
- Programmable input voltage levels of port
  - CMOS input level / hysteresis input level
- FRAM
  - Non-volatile memory
  - 8 Kbytes of FRAM integrated on-chip
- FRAM memory security function
  - Protects the content of FRAM memory

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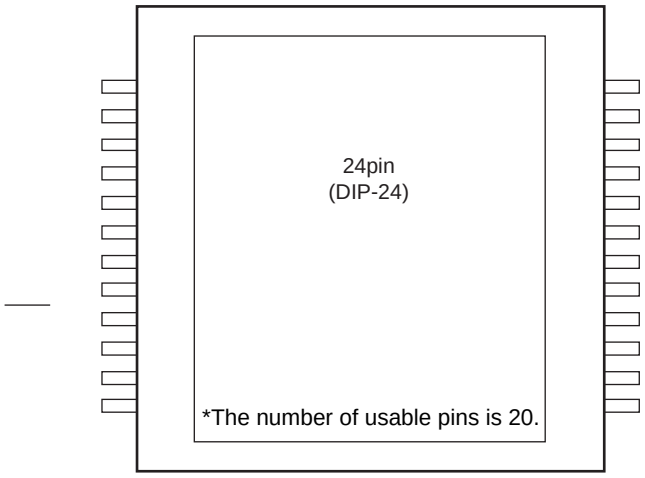
Part number / Parameter	MB95R203
Watch prescaler	Eight different time intervals can be selected.
FRAM	Non-volatile memory Number of read/write cycles : (Min)10^{10} times (Typ)10^{11} times Data retention characteristics : 10 years (+ 55 °C) Read security function Function to monitor FRAM power supply
Standby Mode	Sleep mode, Stop mode, Watch mode, timebase timer mode
Package	SDIP-24, SOP-20

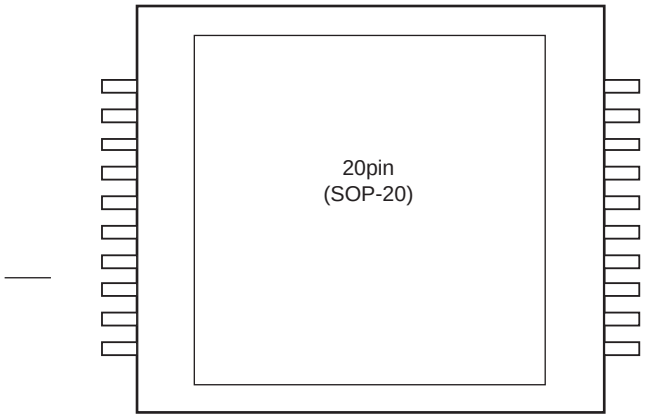
■ PIN ASSIGNMENT

(TOP VIEW)



(DIP-24P-M07)

(TOP VIEW)



(FPT-20P-M09)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O Circuit type*	Function
SDIP24	SOP20			
1	1	X0	B	Main clock input oscillation pin
3	2	X1	B	Main clock input/output oscillation pin
4	3	Vss	—	Power supply pin (GND)
5	4	PG2/X1A	C	General-purpose I/O port This pin is also used as Sub clock input/output oscillation pin.
6	5	PG1/X0A	C	General-purpose I/O port This pin is also used as Sub clock input oscillation pin.
7	6	Vcc	—	Power supply pin
8	7	P65/SCL	I	General-purpose I/O port This pin is also used as I^2C clock I/O.
9	8	PF2/$\overline{RST}$	A	General-purpose I/O port This pin is also used as reset pin
10	9	P62/TO10	D	General-purpose I/O port High current port This pin is also used as 8/16-bit composite timer ch.1 output.
12	10	P63/TO11	D	General-purpose I/O port This pin is also used as 8/16-bit composite timer ch.1 output. High current port
13	11	P64/SDA/EC1	I	General-purpose I/O port This pin is also used as I^2C data I/O. This pin is also used as 8/16-bit composite timer ch.1 clock input.
15	12	P00/AN00	E	General-purpose I/O port This pin is also used as A/D converter analog input.
16	13	P01/AN01	E	General-purpose I/O port This pin is also used as A/D converter analog input.
17	14	P02/INT02/AN02/ UCK	E	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO clock I/O.
18	15	P03/INT03/AN03/ UO	E	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO data output.
19	16	P04/INT04/AN04/ UI/HCLK1/EC0	F	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. This pin is also used as UART/SIO data input. This pin is also used as 8/16-bit composite timer ch.0 clock input.

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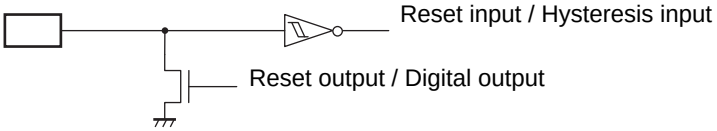
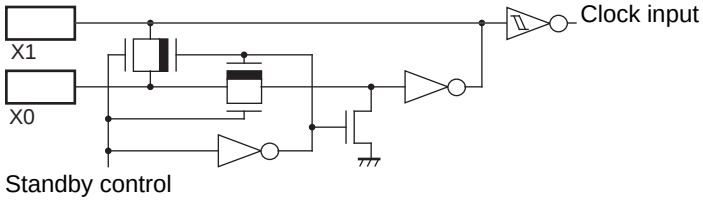
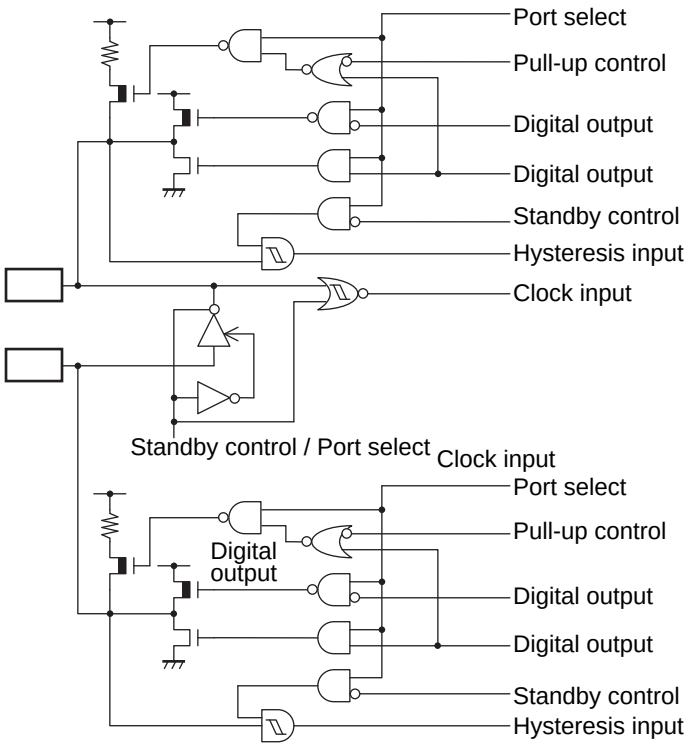
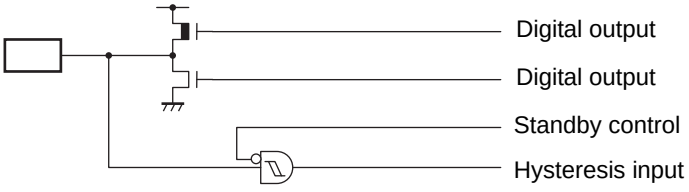
Pin no.		Pin name	I/O Circuit type*	Function
SDIP24	SOP20			
20	17	P05/INT05/AN05/ TO00/HCLK2	E	General-purpose I/O port This pin is also used as external interrupt input. This pin is also used as A/D converter analog input. The pins are also used as 8/16-bit compound timer ch.0 output. This pin is also used as the external clock input.
21	18	P06/INT06/TO01	G	General-purpose I/O port High current port This pin is also used as external interrupt input. This pin is also used as 8/16-bit compound timer ch.0 output.
22	19	P07/INT07	G	General-purpose I/O port This pin is also used as external interrupt input.
24	20	P12/EC0/DBG	H	General-purpose I/O port This pin is also used as DBG input pin. This pin is also used as 8/16-bit composite timer ch.0 clock input.
2, 11, 14, 23	—	NC	—	Internal connect pin. Be sure this pin is left open.

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance : approx. 10 MΩ • CMOS output • Hysteresis input • With pull-up control
D		• CMOS output • Hysteresis input

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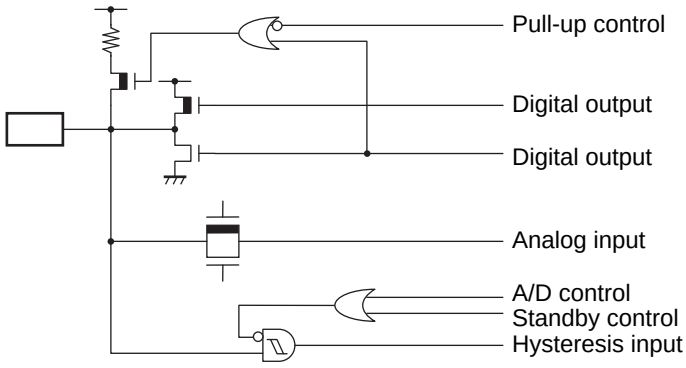
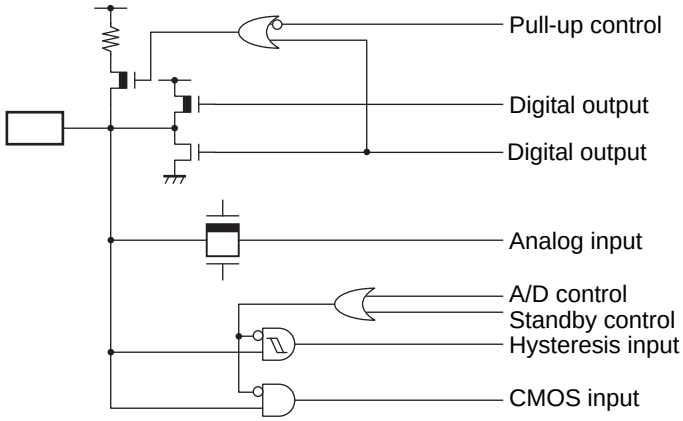
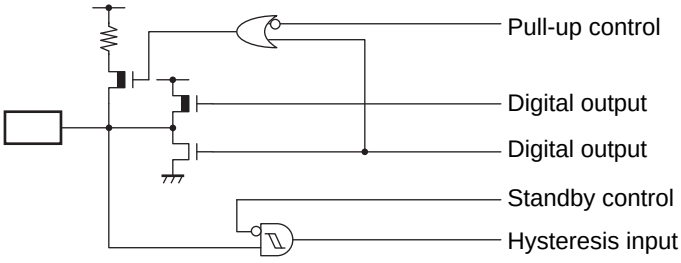
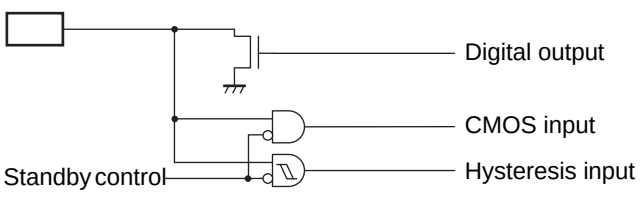
Type	Circuit	Remarks
E		• CMOS output • Hysteresis input • With pull-up control
F		• CMOS output • Hysteresis input • CMOS input • With pull-up control
G		• Hysteresis input • CMOS output • With pull-up control
H	• Hysteresis input Digital output	• N-ch open drain output • Hysteresis input
I		• N-ch open drain output • CMOS input • Hysteresis input

■ NOTES ON DEVICE HANDLING

- Preventing Latch-up

  Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.
  Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.
  When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

- Stable Supply Voltage

  Supply voltage should be stabilized.
  A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.
  For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz / 60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

- Do not use a sample used in program development as mass-produced product.

■ PIN CONNECTION

• Treatment of Unused Input Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance. It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

• DBG Pin

Connect the DBG pin directly to external Pull-up.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the DBG pins to V_{CC} or V_{SS} pins.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

• $\overline{\text{RST}}$ Pin

Connect the $\overline{\text{RST}}$ pin directly to Pull-up.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the $\overline{\text{RST}}$ pins to V_{CC} or V_{SS} pins.

The $\overline{\text{RST}}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output can be enabled by the RSTOE bit of the SYSC register, and the reset input function or the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

• Example of DBG / $\overline{\text{RST}}$ connection diagram

Pull-up resistor recommended resistance
For DBG pin : R = 4.7 kΩ
For $\overline{\text{RST}}$ pin : R = 10 kΩ

■ RESTRICTIONS

- Data written to FRAM before IR reflow is not guaranteed to retain after IR reflow.
  (Data written to FRAM might be broken by heart processing at IR reflow.)

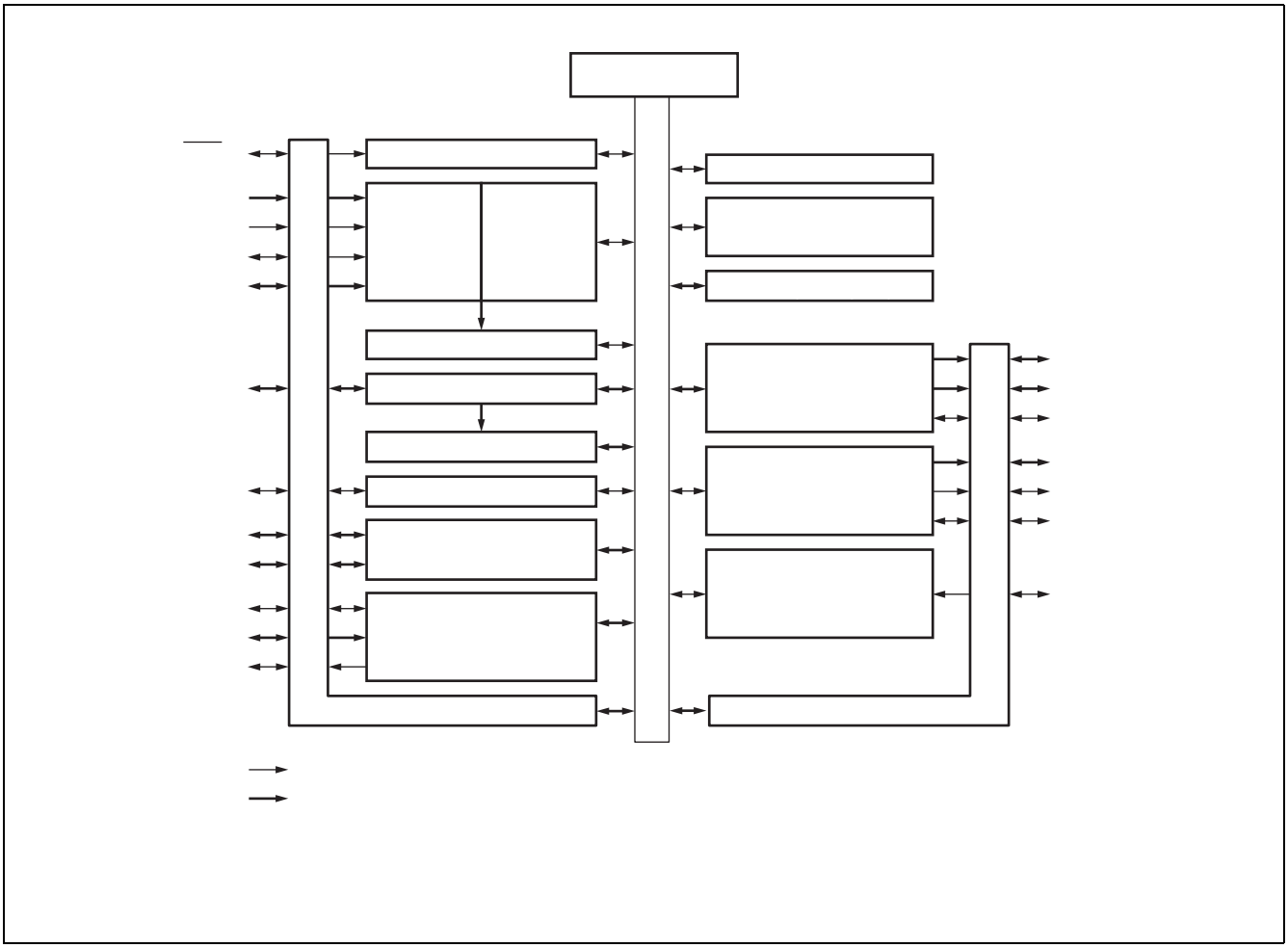
■ NOTES ON DEBUG

- Although the [Upload Flash Memory] button is enabled, clicking it does not start the actual processing.
- When you click on the [Erase Flash Memory] button on SOFTUNE Workbench, data is overwritten into the FRAM area, as shown below.

Address	Data to be overwritten
$F554_H$	55_H
$FAAA_H$	$A0_H$
$FFBC_H$	Indeterminate
$FFBD_H$	Indeterminate
Entire FRAM except the above	FF_H

- Be very careful not to apply voltages to the pins PF2/$\overline{RST}$ in excess of the absolute maximum ratings. Especially when handling devices in the environment compatible to the package, such as MB95F200H/210H and so on, the voltage may be erroneously applied to the pins PF2/$\overline{RST}$ in excess of the maximum rating and it may cause thermal breakdown of the device.

■ BLOCK DIAGRAM

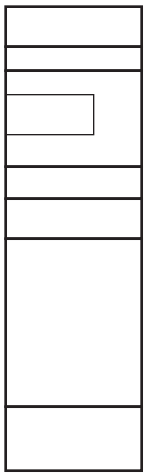


■ CPU CORE

1. Memory space

Memory space of the MB95R203 is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95R203 shown below.

- Memory Map



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	—	(disabled)	—	—
0007H	SYCC	System clock control register	R/W	XXXXXX11B
0008H	STBC	Standby control register	R/W	00000XXXB
0009H	RSRR	Reset source register	R	XXXXXXXXB
000AH	TBTC	Timebase timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	SYCC2	System clock control register 2	R/W	XX100011B
000EH to 0015H	—	(disabled)	—	—
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H to 0027H	—	(disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0034H	—	(disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000B
0037H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000B
0038H	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000B
0039H	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000B

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Address	Register abbreviation	Register name	R/W	Initial value
0F99H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000B
0F9BH	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000B
0F9CH to 0FBDH	—	(disabled)	—	—
0FBEH	PSSR0	UART/SIO prescaler select register	R/W	00000000B
0FBFH	BRSR0	UART/SIO baud rate setting register	R/W	00000000B
0FC0H to 0FC2H	—	(disabled)	—	—
0FC3H	AIDRL	A/D input disable register lower	R/W	00000000B
0FC4H to 0FE3H	—	(disabled)	—	—
0FE4H	CRTH	CR-trimming register upper	R/W	1XXXXXXXB
0FE5H	CRTL	CR-trimming register lower	R/W	000XXXXXB
0FE6H, 0FE7H	—	(disabled)	—	—
0FE8H	SYSC	System control register	R/W	11000-11B
0FE9H	CMCR	Clock monitor control register	R/W	--000000B
0FEAH	CMDR	Clock monitor data register	R/W	00000000B
0FEBH	WDTH	Watchdog ID register upper	R/W	XXXXXXXXB
0FECH	WDTL	Watchdog ID register lower	R/W	XXXXXXXXB
0FEDH	—	(disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	-----0--B
0FEFH to 0FFFH	—	(disabled)	—	—

- R/W access symbols
  - R/W : Readable / Writable
  - R : Read only
  - W : Write only

- Initial value symbols
  - 0 : The initial value of this bit is “0”.
  - 1 : The initial value of this bit is “1”.
  - X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc	Vss – 0.3	Vss + 4.0	V	
Input voltage*1	V_{I1}	Vss – 0.3	Vss + 4.0	V	Other than P64, P65*2
	V_{I2}	Vss – 0.3	Vss + 6.0	V	P64, P65
Output voltage*1	V_O	Vss – 0.3	Vss + 4.0	V	*2
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63
	I_{OL2}		15		P05, P06, P62 and P63
“L” level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
	I_{OLAV2}		12		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
“H” level maximum output current	I_{OH1}	—	–15	mA	Other than P05, P06, P62 and P63
	I_{OH2}		–15		P05, P06, P62 and P63
“H” level average current	I_{OHAV1}	—	–4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		–8		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Total average output current = operating current × operating ratio (Total of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	–20	+ 70	°C	
Storage temperature	Tstg	–20	+ 85	°C	

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*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : V_{I1} and Vo should not exceed V_{CC} + 0.3 V. V_{I1} must not exceed the rating voltage.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	Vcc	2.7	3.6	V	In normal operating
		3.0	3.6		On-chip debug mode
		2.6	3.6		Hold condition in STOP mode
Operating temperature	T_A	–20	+70	°C	Other than on-chip debug mode
		+5	+35	°C	On-chip debug mode

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P04	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (Hysteresis input) is selected
	V_{IH2}	P64, P65	*1	0.7 V_{CC}	—	V_{SS} + 5.5	V	When CMOS input level (Hysteresis input) is selected
	V_{IHS1}	P00 to P07, P12, P62, P63, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P64, P65	*1	0.8 V_{CC}	—	V_{SS} + 5.5	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04, P64, P65	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	When CMOS input level (Hysteresis input) is selected
	V_{ILS}	P00 to P07, P12, P62 to P65, PG1, PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P64, P65	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	PF2, P12	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P62 to P65, PF2, P12	I_{OH} = –4.0 mA	2.4	—	—	V	
	V_{OH2}	P05, P06, P62, P63	I_{OH} = –8.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62, P63	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63	I_{OL} = 12.0 mA	—	—	0.4	V	

(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current (Hi-Z output leak current)	I_{LI}	Other than ports P64, P65	0.0 V < V_I < V_{CC}	–5	—	+ 5	µA	When pull-up resistance is disabled
Open-drain output leak current	I_{LIOD}	P64, P65	0.0 V < V_I < V_{SS} + 5.5 V	—	—	+ 5	µA	
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than Vcc, Vss	f = 1 MHz	—	5	15	pF	
Power supply current*2	I_{CC}	Vcc (External clock operation)	F_{CH} = 20 MHz, F_{MP} = 10 MHz Main clock mode (divided by 2)	—	6	9	mA	
				—	8	12	mA	At A/D conversion
	I_{CCS}		F_{CH} = 20 MHz, F_{MP} = 10 MHz Main sleep mode (divided by 2)	—	3	5	mA	
	I_{CCL}		F_{CL} = 32 kHz, F_{MPL} = 16 kHz Sub clock mode (divided by 2) T_A = +25 °C	—	30	70	µA	
	I_{CCLS}		F_{CL} = 32 kHz, F_{MPL} = 16 kHz Sub sleep mode (divided by 2) T_A = +25 °C	—	5	40	µA	
	I_{CCT}		F_{CL} = 32 kHz, Watch mode Main stop mode T_A = +25 °C	—	3	18	µA	
	I_{CCMCR}	Vcc	F_{CRH} = 1 MHz, F_{MP} = 1 MHz Main CR clock mode	—	2	—	mA	
	I_{CCSCR}		Sub CR clock mode (divided by 2) T_A = +25 °C	—	80	300	µA	

(Continued)

(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCTS}	Vcc (External clock operation)	F_{CH} = 10 MHz, Timebase timer mode T_A = +25 °C	—	1	3	mA	
	I_{CCH}		Sub stop mode T_A = +25 °C	—	1	10	µA	
	I_{CRH}	V_{CC}	Current consumption of internal main CR oscillator	—	0.2	0.3	mA	
	I_{CRL}		At oscillating 100 kHz current consumption of internal sub CR oscillator	—	20	72	µA	

*1 : P04, P64, P65 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR) .

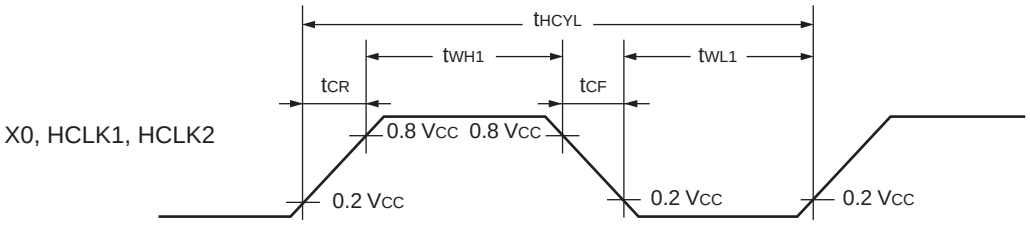
*2 :
- The power-supply current is determined by the external clock. when Internal CR are selected, the power-supply current will be a value of adding current consumption of internal CR oscillator (I_{CRL}) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

4. AC Characteristics

(1) Clock Timing

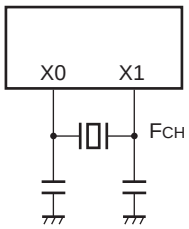
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	When the main oscillation circuit is used
		X0, X1, HCLK1, HCLK2		1	—	20	MHz	When the main external clock is used
	F_{CRH}	—		0.95	1	1.05	MHz	When the main internal CR clock is used (3.0 V ≤ V_{CC} ≤ 3.6 V, + 5 °C ≤ T_A ≤ + 35 °C)
	F_{CL}	X0A, X1A		—	32.768	—	MHz	When the sub oscillation circuit is used
				—	32.768	—	kHz	When the sub external clock is used
	F_{CRL}	—		50	100	200	kHz	When the sub internal CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	100	—	1000	ns	When the main oscillation circuit is used
		X0, X1, HCLK1, HCLK2		50	—	1000	ns	When the main external clock is used
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub clock
Input clock pulse width	t_{WH1}	X0, HCLK1, HCLK2		20	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%
	t_{WL1}							
	t_{WH2}	X0A		—	15.2	—	µs	
	t_{WL2}							
Input clock rise time and fall time	t_{CR}	X0, X0A, HCLK1, HCLK2		—	—	5	ns	When the external clock is used
	t_{CF}							
Internal CR oscillation start time	t_{CRHWK}	—		—	—	10	µs	When the main-internal CR clock is used
	t_{CRLWK}	—		—	—	10	µs	When the sub-internal CR clock is used

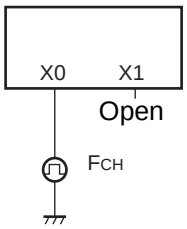


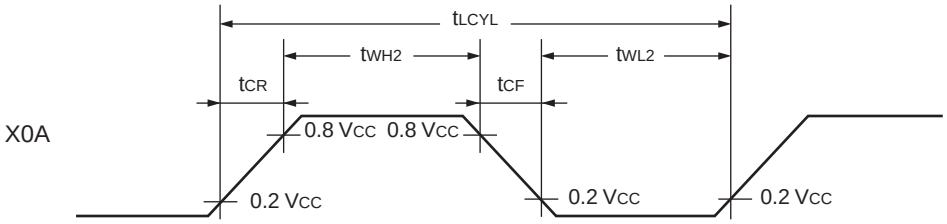
- Figure of main clock input port external connection

When using a crystal or Ceramic oscillator



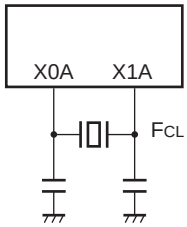
When using external clock



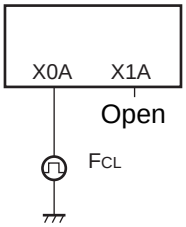


- Figure of sub clock input port external connection

When using a crystal or Ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before division)	t_{SCLK}	—	100	—	2000	ns	When using main external clock Min : F_{CH} = 20 MHz, divided by 2 Max : F_{CH} = 1 MHz, divided by 2
			—	1	—	µs	When using main CR oscillation clock F_{CRH} = 1 MHz
			—	61	—	µs	When using sub oscillation clock F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When using sub oscillation clock F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	10	MHz	When using main oscillation clock
			—	1	—	MHz	When using main CR oscillation clock
	F_{SPL}		—	16.384	—	kHz	When using sub oscillation clock
			—	50	—	kHz	When using sub CR clock
Machine clock cycle time*2 (Minimum instruction execution time)	t_{MCLK}	—	100	—	32000	ns	When using main oscillation clock Min : F_{SP} = 10 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			1	—	16	µs	When using main CR clock Min : F_{SP} = 1 MHz, no division Max : F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When using sub oscillation clock Min : F_{SPL} = 16.384 kHz, no division Max : F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When using sub CR clock Min : F_{SPL} = 50 kHz, no division Max : F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	10	MHz	When using main oscillation clock
			0.0625	—	1	MHz	When using main CR clock
	F_{MPL}		1.024	—	16.384	kHz	When using sub oscillation clock
			3.125	—	50	kHz	When using sub CR clock
FRAM clock cycle time*3 (Minimum instruction execution time)	t_{FCLK}	—	300	—	96000	ns	When using main oscillation clock Min : F_{SP} = 10 MHz, divided by 3 Max : F_{SP} = 0.5 MHz, divided by 48
			3	—	48	µs	When using main CR clock Min : F_{SP}=1 MHz, divided by 3 Max : F_{SP}=1 MHz, divided by 48
			183	—	2929.7	µs	When using sub oscillation clock Min : F_{SPL} = 16.384 kHz, divided by 3 Max : F_{SPL} = 16.384 kHz, divided by 48
			60	—	960	µs	When using sub CR clock Min : F_{SPL} = 50 kHz, divided by 3 Max : F_{SPL} = 50 kHz, divided by 48

(Continued)

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
FRAM clock frequency	F_{FCLK}	—	0.010	—	3.3	MHz	When using main oscillation clock
			0.0208	—	0.3333	MHz	When using main CR clock
	F_{FCLKL}		0.341	—	5.461	kHz	When using sub oscillation clock
			1.042	—	16.667	kHz	When using sub CR clock

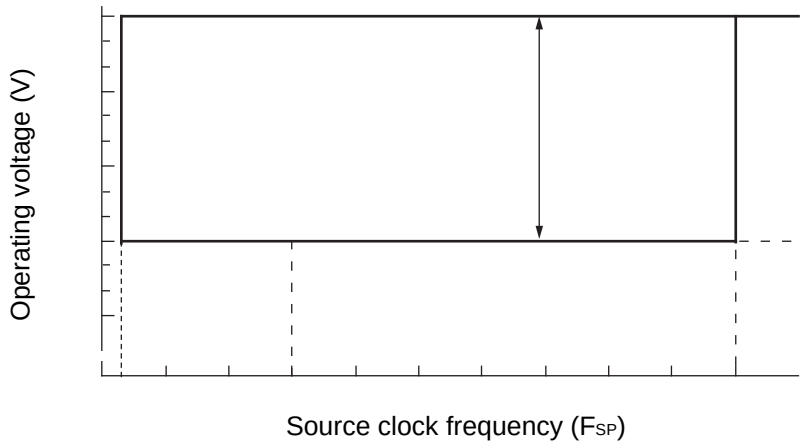
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.
- Main clock divided by 2
- Main CR clock
- Sub clock divided by 2
- Sub CR clock divided by 2

*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

*3 : The clock in case of operating code on FRAM, or Read/Write access to FRAM. Its value is machine clock divided by 3.

- Outline of clock generation block

• Operating voltage - Operating frequency (When T_A = − 20 °C to + 70 °C)



(3) External Reset

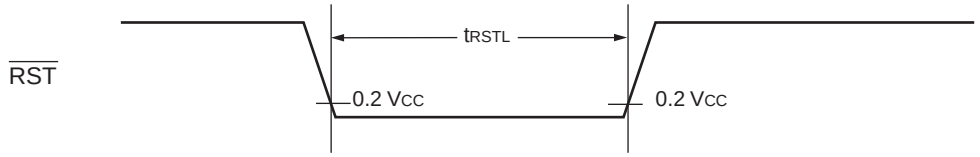
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode
		100	—	µs	At time-base timer mode

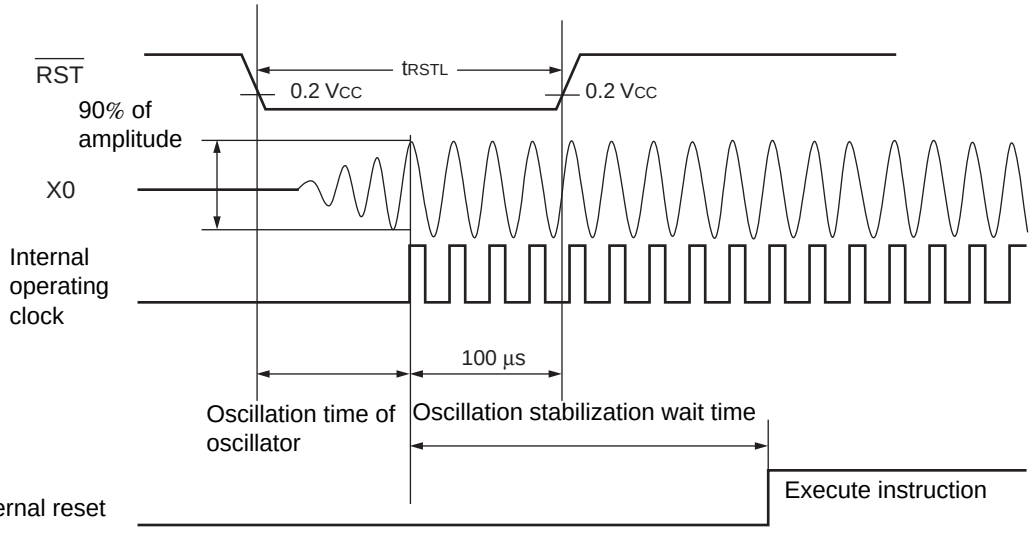
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

- At normal operating



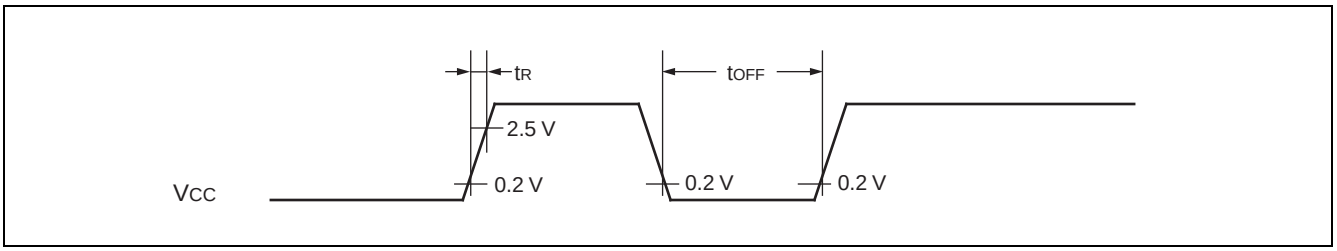
- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



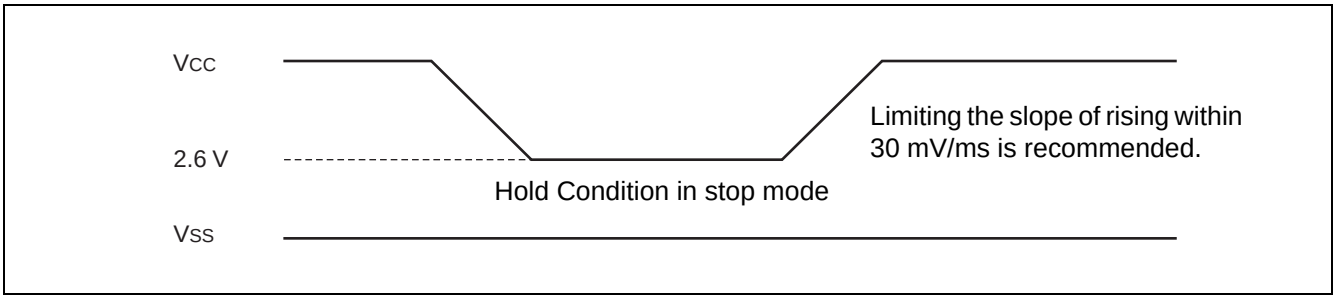
(4) Power-on Reset

(Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Waiting time until power-on



Note: Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

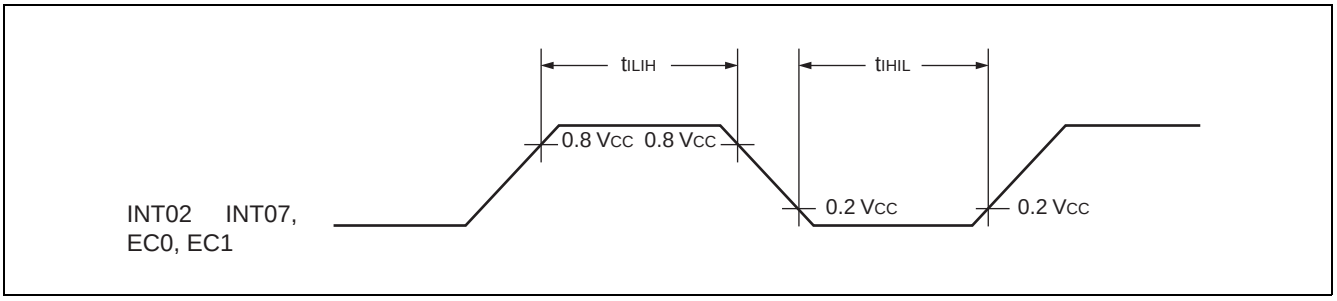


(5) Peripheral Input Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse	t_{ILIH}	INT02 to INT07, EC0, EC1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



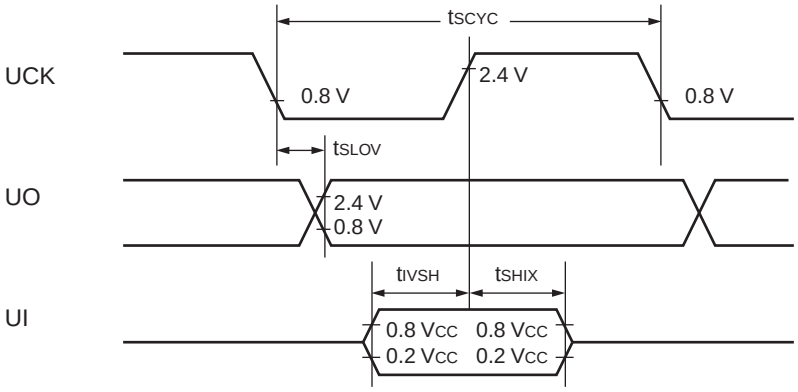
(6) UART/SIO, Serial I/O Timing

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

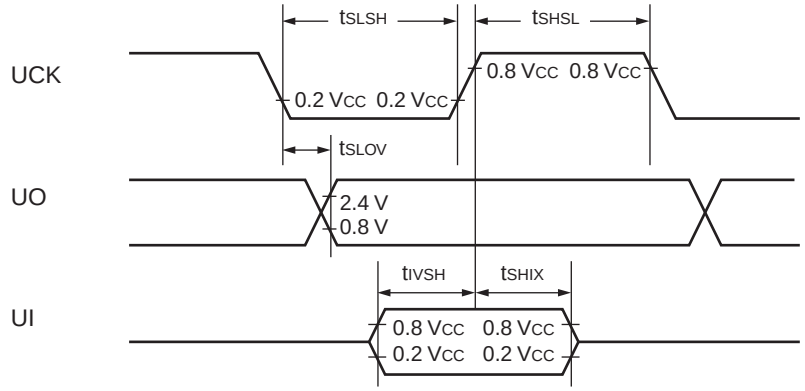
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK,UI		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		0	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK, UI		2 t_{MCLK}*	—	ns
UCK ↑→ valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for details on t_{MCLK}.

• Internal shift clock mode



• External shift clock mode



(7) I²C Timing

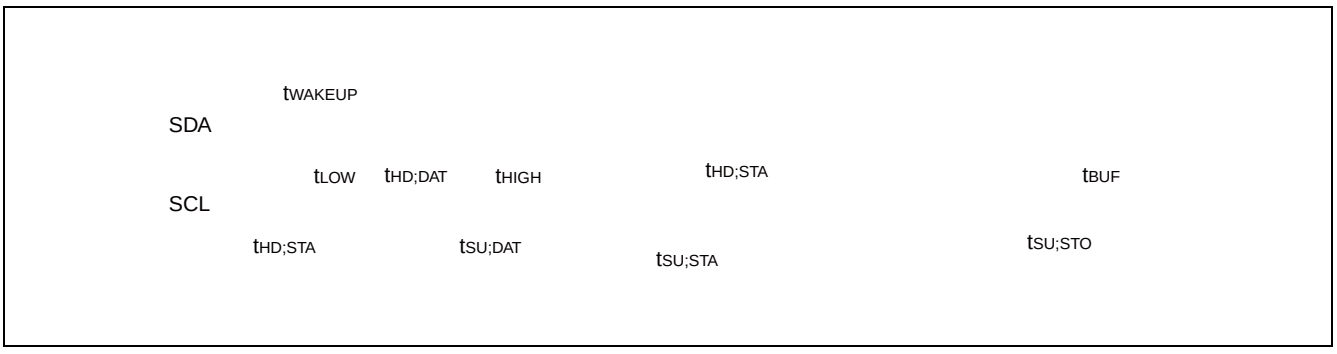
(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	t_{SCYC}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL SDA		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↓	$t_{SU;STO}$	SCL SDA		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL SDA		4.7	—	1.3	—	µs

*1 : R, C : Pull-up resistance and load capacitance of the SCL and SDA lines.

*2 : The maximum value of $t_{HD;DAT}$ is applicable only if the device does not extend the “L” width (t_{LOW}) of the SCL signal.

*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met.



(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Condi-tions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		(nm / 2) t_{MCLK} – 20	(nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL SDA		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applid.
Stop condition setup time	$t_{SU;STO}$	SCL SDA		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL SDA		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL SDA		(2 nm + 4) t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL SDA		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL SDA		(–2 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between cleaning interrupt and SCL rising	$t_{SU;INT}$	SCL		(nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL		4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL SDA		4 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception

(Continued)

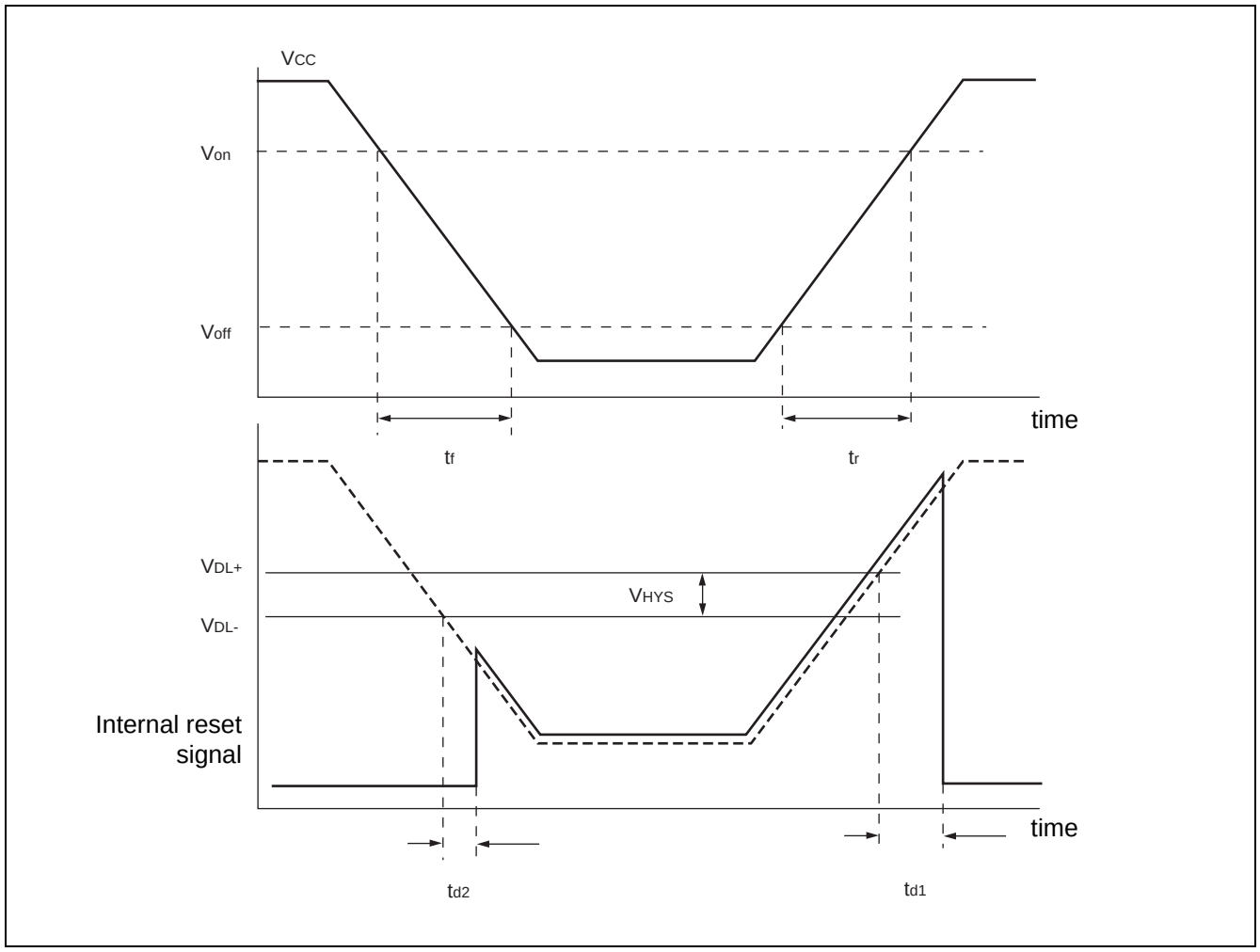
(Continued)

(Vcc = 3.3 V, Vss = 0.0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL SDA	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL SDA		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL SDA		2 t_{MCLK} – 20	—	ns	During reception
Data hold time	$t_{HD;DAT}$	SCL SDA		2 t_{MCLK} – 20	—	ns	In slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	In slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL SDA		0	—	ns	During reception
Data setup time	$t_{SU;DAT}$	SCL SDA		t_{MCLK} – 20	—	ns	During reception
SDA ↓ → SCL ↑ (when using wakeup function)	t_{WAKEUP}	SCL SDA		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

*1 : R, C : Pull-up resistance and load capacitance of the SCL and SDA lines.

*2 :
- Refer to " (2) Source Clock/Machine Clock" for details on t_{MCLK}.
- m is the CS4 and CS3 bits (bit 4 and bit 3) of the I²C clock control register (ICCR0) .
- n is the CS2 to CS0 bits (bit 2 to bit0) of the I²C clock control register (ICCR0) .
- The actual I²C timing is determined by the machine (t_{MCLK}) and the values of m and n configured in bits CS4 to CS0 of the I²C clock control register (ICCR0) .
- Standard-mode :
  m and n can be set in the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The machine clock to be used is determined by the settings of m and n as follows.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
- Fast-mode :
  m and n can be set in the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The machine clock to be used is determined by the settings of m and n as follows.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

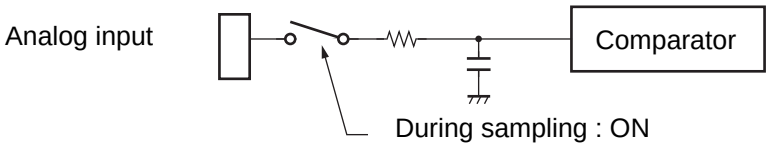

VCC
Von
Voff
time
tf
tr
VDL+
VHYS
VDL-
Internal reset signal
time
td2
td1

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

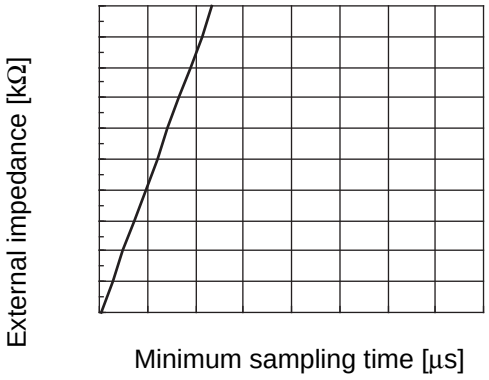


2.7 V ≤ Vcc ≤ 3.6 V : R ≒ 1.7 kΩ (Max) , C ≒ 14.5 pF (Max)

Note : The values are reference values.

- The relationship between external impedance and minimum sampling time.

[External impedance = 0 kΩ to 100 kΩ]



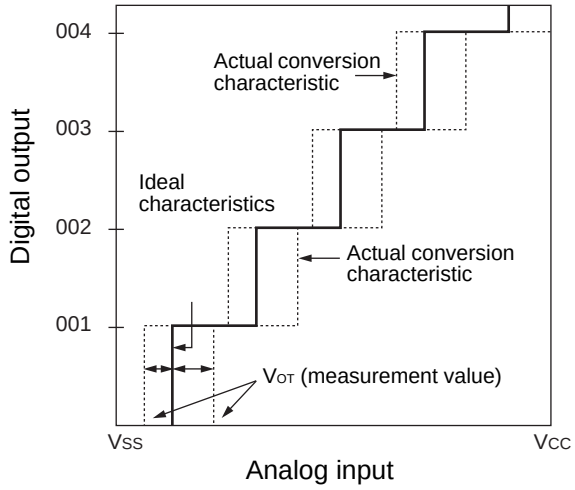
[External impedance = 0 kΩ to 20 kΩ]

- **About errors**

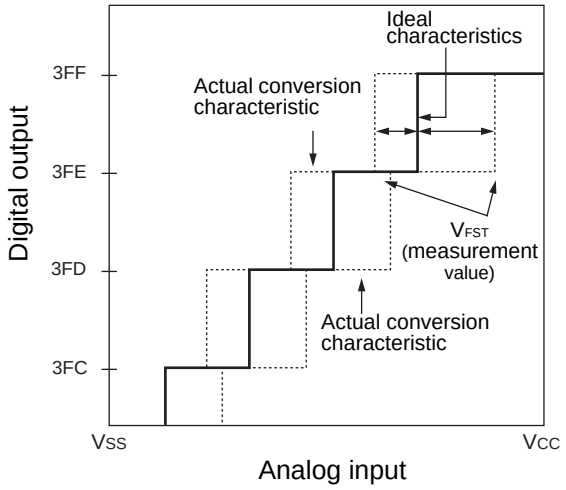
$|V_{CC} - V_{SS}|$ becomes smaller, values of relative errors grow larger.

(Continued)

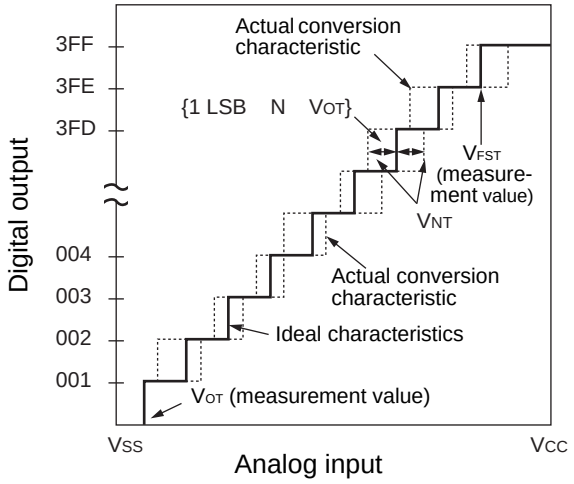
Zero transition error



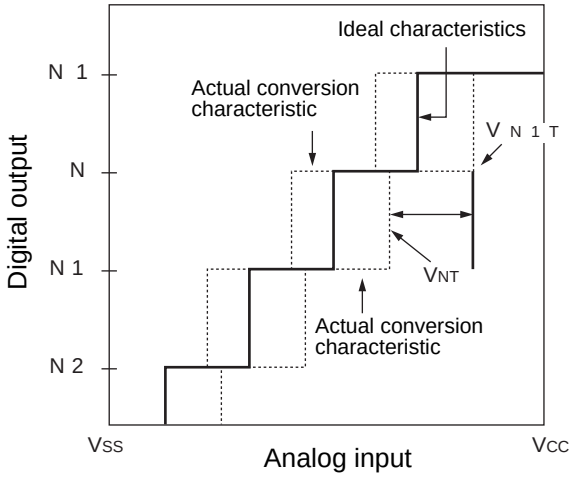
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error In digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N - 1) to N.
V_{OT} (Ideal value) = V_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = V_{CC} – 2.0 LSB [V]

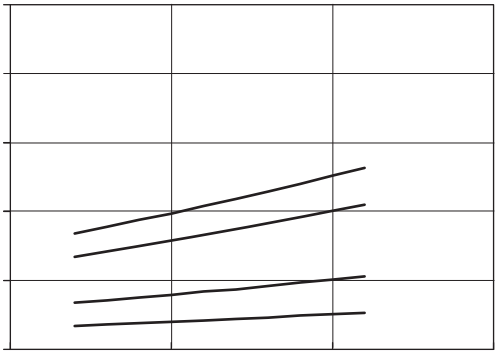
6. FRAM Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Number of read/write cycle	10^{10}	10^{11}	—	cycle	

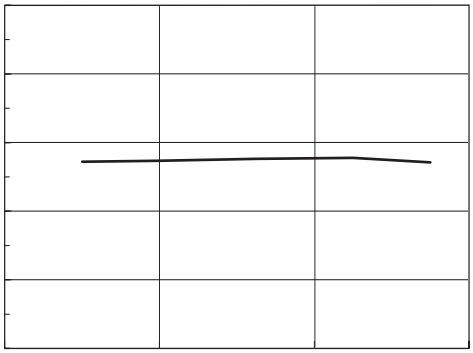
■ EXAMPLE CHARACTERISTICS

- Power supply current and temperature

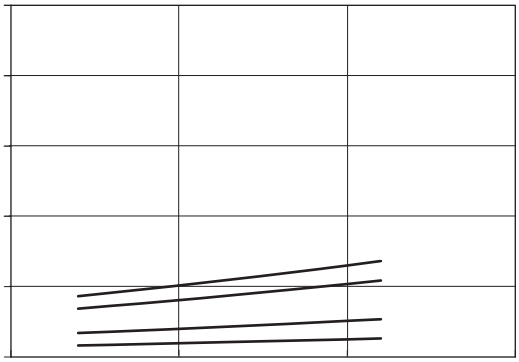
I_{CC} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 3, 8, 10 MHz (divided by 2)
Main clock mode, at external clock operating



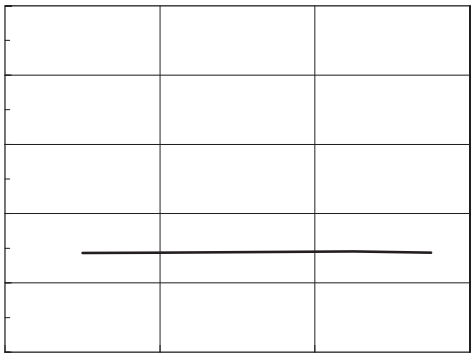
I_{CC} – T_A
V_{CC} = 3.6 V, F_{MP} = 10 MHz (divided by 2)
Main clock mode, at external clock operating



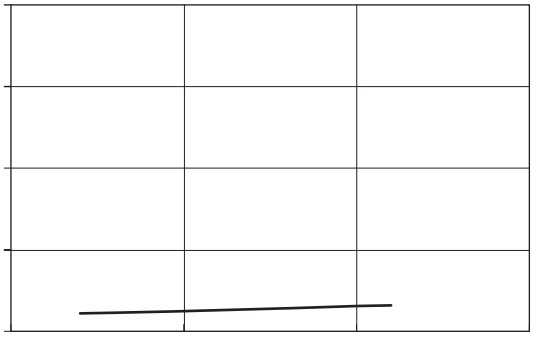
I_{CCS} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 3, 8, 10 MHz (divided by 2)
Main sleep mode, at external clock operating



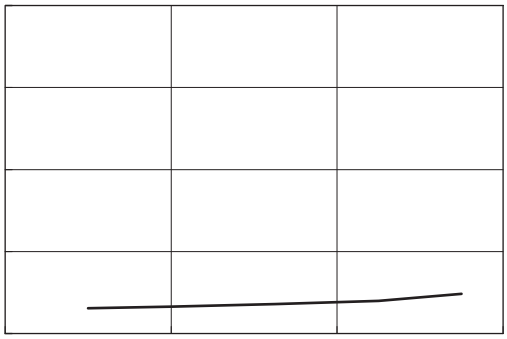
I_{CCS} – T_A
V_{CC} = 3.6 V, F_{MP} = 10 MHz(divided by 2)
Main sleep mode, at external clock operating



I_{CCL} – V_{CC}
T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Sub clock mode, at external clock operating

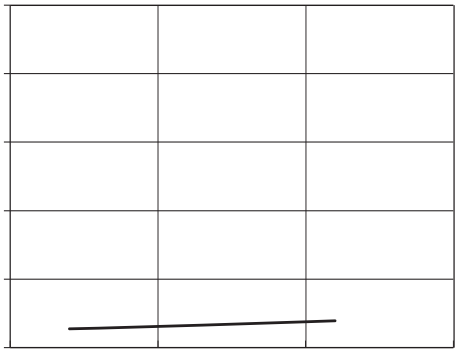


I_{CCL} – T_A
V_{CC} = 3.6 V, F_{MPL} = 16 kHz (divided by 2)
Sub clock mode, at external clock operating

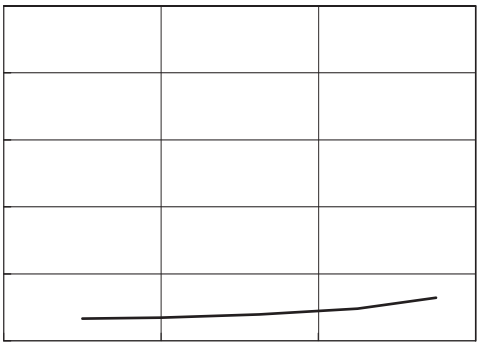


(Continued)

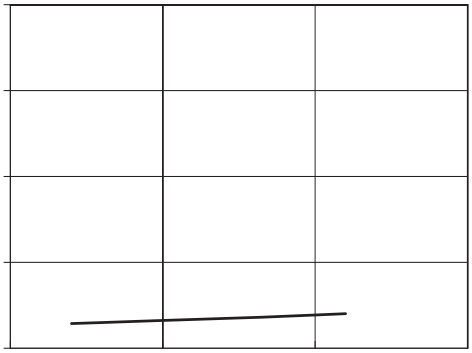
I_{CCLS} – V_{CC}
T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating



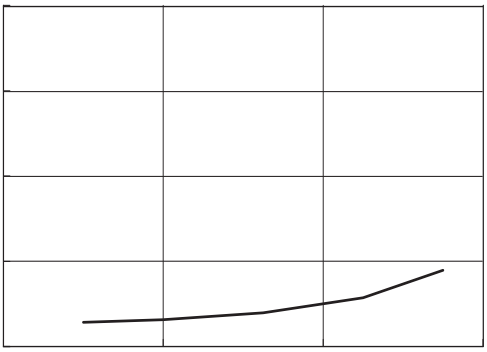
I_{CCLS} – T_A
V_{CC} = 3.6 V, F_{MPL} = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating



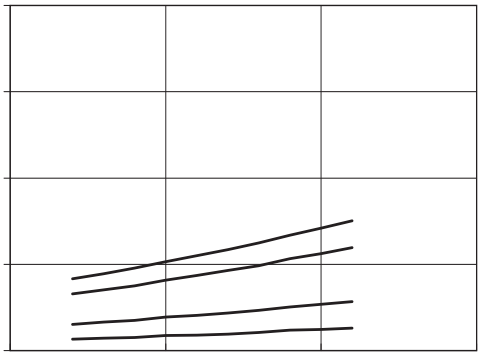
I_{CCT} – V_{CC}
T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Clock mode, at external clock operating



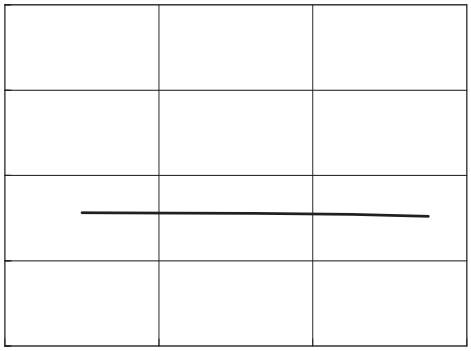
I_{CCT}
V_{CC} = 3.6 V, F_{MPL} = 16 kHz (divided by 2)
Clock mode, at external clock operating



I_{CTS} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 4, 8, 10 MHz (divided by 2)
Time-base timer mode, at external clock operating



I_{CTS} – T_A
V_{CC} = 3.6 V, F_{MP} = 10 kHz (divided by 2)
Time-base timer mode, at external clock operating



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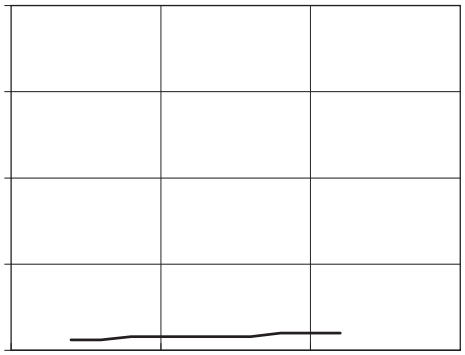
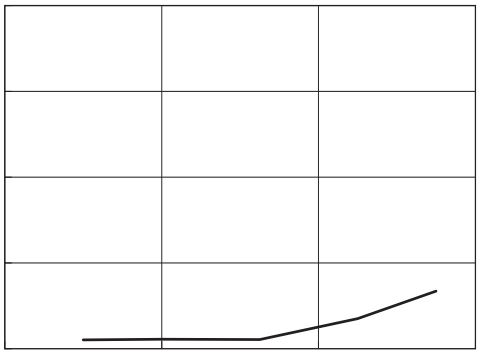
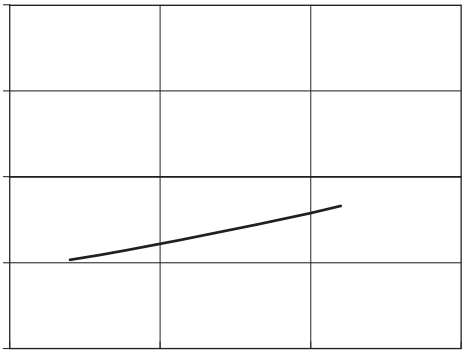
I_{CCH} – V_{CC}
T_A = + 25 °C, F_{MPL} = (stop)
Sub stop mode, at external clock stopping



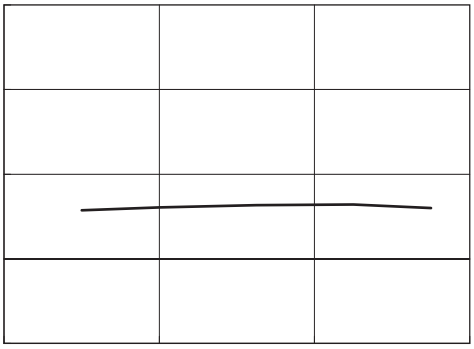
I_{CCH} – T_A
V_{CC} = 3.6 V, F_{MPL} = (stop)
Sub stop mode, at external clock stopping



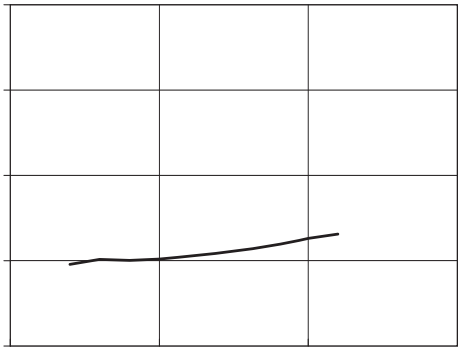
I_{CCMCR} – V_{CC}
T_A = + 25 °C, F_{MP} = 1 MHz (No divided)
Main clock mode, at internal main CR clock operating



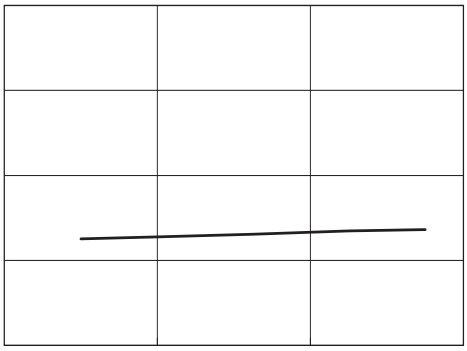
I_{CCMCR} – T_A
V_{CC} = 3.6 V, F_{MP} = 1 MHz (No divided)
Main clock mode, at internal main CR clock operating



I_{CCSCR} – V_{CC}
T_A = + 25 °C, F_{MPL} = 50 kHz (divided by 2)
Sub clock mode, at internal sub CR clock operating

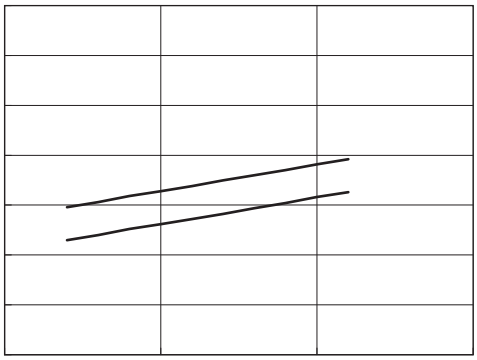


I_{CCSCR} – T_A
V_{CC} = 3.6 V, F_{MPL} = 50 kHz (divided by 2)
Sub clock mode, at internal sub CR clock operating



- Input voltage

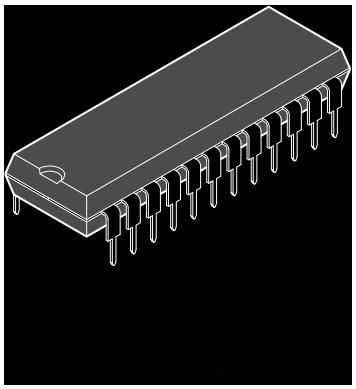
V_{IHI1}, V_{IH2}, V_{IHS1}, V_{IHS2}, V_{IHM} – V_{CC} and
V_{IL}, V_{ILS}, V_{ILM} – V_{CC}
T_A = + 25 °C

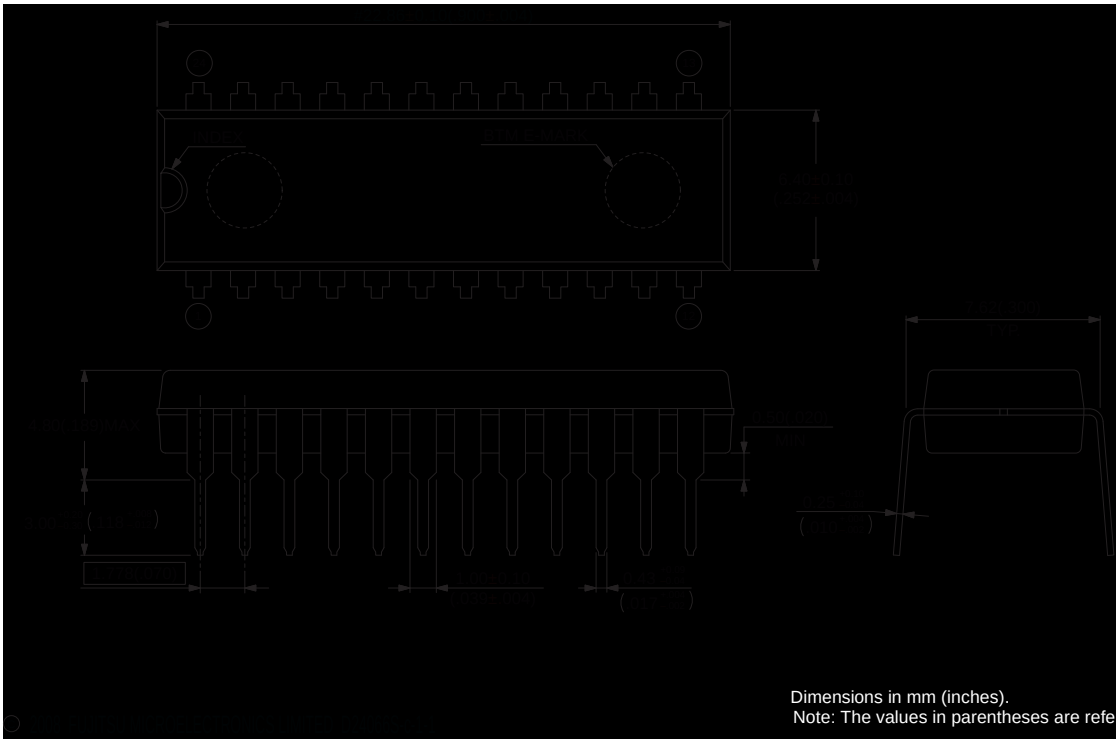


■ ORDERING INFORMATION

Part number	Package	Remarks
MB95R203P-G-SH-JNE2	24-pin plastic SDIP (DIP-24P-M07)	
MB95R203PF-G-JNE2	20-pin plastic SOP (FPT-20P-M09)	

■ PACKAGE DIMENSIONS





Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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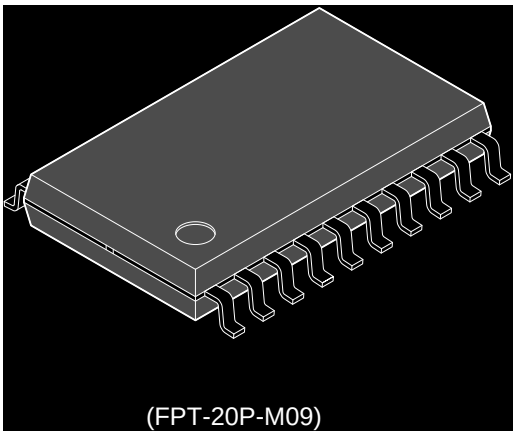
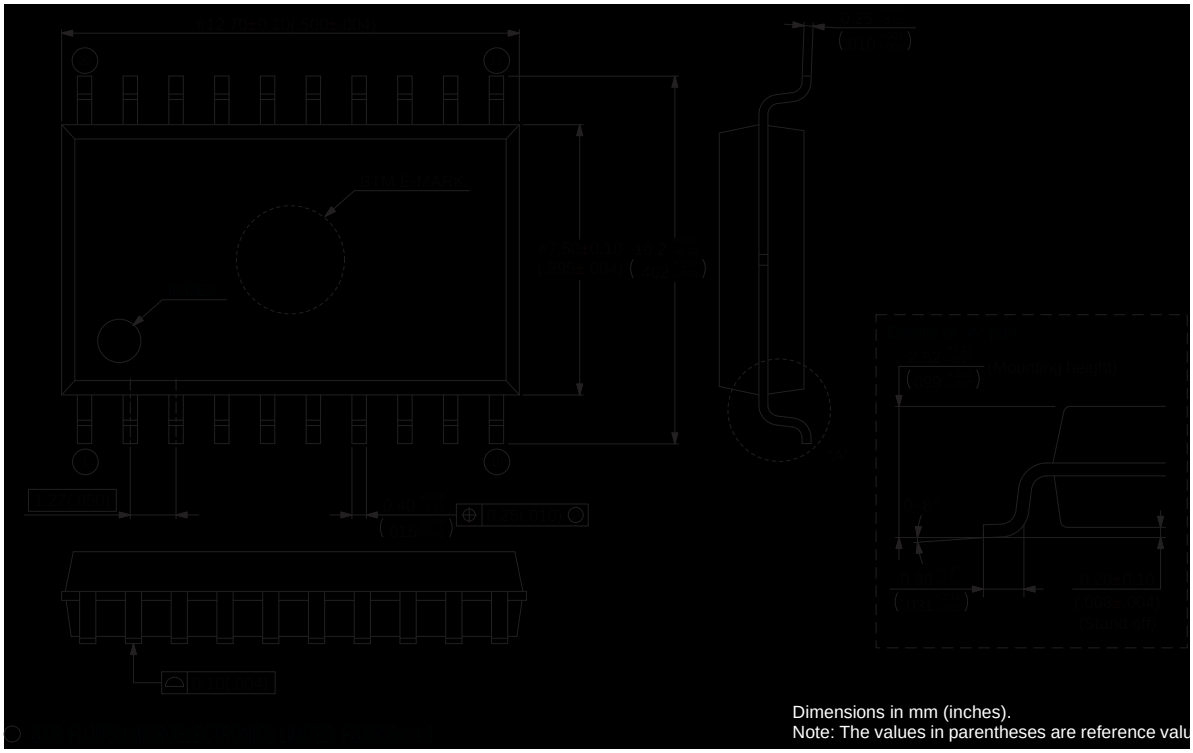


(FPT-20P-M09)



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Preliminary Data Sheet → Data Sheet
4	■ PRODUCT OVERVIEW	Corrected number of read/write cycles for FRAM. 10^{11} times → (Min)10^{10} times (Typ)10^{11} times
9	■ I/O CIRCUIT TYPE	Corrected the remarks of Type G. CMOS input → CMOS output
12	■ NOTES ON DEBUG	Corrected the address. $F555_H$ → $F554_H$
15	■ I/O MAP	Corrected the register abbreviation and the register name for address $000B_H$. WTCR → WPCR Watch timer control register → Watch prescaler control register
17		Changed the register name for address $0F89_H$, $0F8A_H$, and $0F8B_H$ to (disabled).
24	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Added “T_A = + 25 °C” to the condition for “Power supply current (I_{CCLS})”.
32	4. AC Characteristics (4) Power-on Reset	Corrected the voltage for “Hold Condition in stop mode”. 2.3 V → 2.6 V
45 to 50	■ EXAMPLE CHARACTERISTICS	Added the section.

The vertical lines marked in the left side of the page show the changes.

MEMO

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