10 G SFP+ 850 nm Limiting Transceiver, 10 Gigabit Ethernet Compatible

PLRXPL-Vx-S43-23-N Series

Key Features

- **Compatible with 10 G links**
- **Uses a highly reliable, 850 nm oxide VCSEL**
- **Lead-free and RoHS 6/6-compliant, with allowed exemptions**
- **Commercial case operating temperature of 0 – 70°C**
- **Single 3.3 V power supply**
- **Low power consumption (typically 450 mW)**
- **Bit error rate < 1 x 10^{-12}**
- **Hot pluggable**

Applications

- Intra data center connectivity
  - Switch and hub
  - Mass storage systems
  - Host bus adapters
- Enterprise access interconnect
- High-speed storage interconnect
- Disaster recovery/backup connectivity
- High-speed cluster/grid computing aggregation

Compliance

- SFF 8431 Revision 3.2
- SFF 8432 Revision 5.0
- SFF 8472 Revision 10.3
- CDRH and IEC60825-1 Class 1 Laser Eye Safety
- FCC Class B
- ESD Class 2 per MIL-STD 883
- UL 94, V0
- Reliability tested per Telcordia GR-468

The lead-free and RoHS-compliant small form factor pluggable (SFP+) transceiver from JDSU improves the performance for 10 Gigabit Ethernet (10 G) applications, and is ideal for high-speed campus and large data center applications. This transceiver features a highly reliable, 850 nm, oxide, vertical-cavity surface-emitting laser (VCSEL) coupled to an LC optical connector. The transceiver is fully compatible with 10GBASE-SR, 10GBASE-SW and 10 G Fibre Channel specifications at shorter link distances, with internal AC coupling on both transmit and receive data signals. The all-metal housing design provides low EMI emissions in demanding 10 G applications and conforms to IPF specifications. An enhanced digital diagnostic feature set allows for real-time monitoring of transceiver performance and system stability, and the serial ID allows for customer and vendor system specific information to be stored in the transceiver. Transmit disable, loss-of-signal, and transmitter fault functions are also provided. The small size of the transceiver allows for high-density board designs that, in turn, enable greater aggregate bandwidth.

Section 1 Functional Description

The PLRXPL-Vx-S43-23-N 10G SFP+ 850 nm optical transceiver is designed to transmit and receive 10 G serial optical data over 50/125 µm or 62.5/125 µm multimode optical fiber.

Transmitter

The transmitter converts serial PECL or CML electrical data into serial optical data compatible with the 10GBASE-SR, 10GBASE-SW or 10 G Fibre Channel standard. Transmit data lines (TD+ and TD-) are internally AC coupled, with 100 Ω differential termination.

Transmitter rate select (RS1) pin 9 is assigned to control the SFP+ module transmitter rate. It is connected internally to a 30 kΩ pull-down resistor. A data signal on this pin does not affect the operation of the transmitter.

An open collector-compatible transmit disable (Tx_Disable) is provided. This pin is internally terminated with a 10 kΩ resistor to $V_{cc,T}$. A logic "1," or no connection, on this pin will disable the laser from transmitting. A logic "0" on this pin provides normal operation.

The transmitter has an internal PIN monitor diode that ensures constant optical power output, independent of supply voltage. It is also used to control the laser output power over temperature to ensure reliability at high temperatures.

An open collector-compatible transmit fault (Tx_Fault) is provided. The Tx_Fault signal must be pulled high on the host board for proper operation. A logic "1" output from this pin indicates that a transmitter fault has occurred or that the part is not fully seated and the transmitter is disabled. A logic "0" on this pin indicates normal operation.

Receiver

The receiver converts serial optical data into serial PECL/CML electrical data. Receive data lines (RD+ and RD-) are internally AC coupled with 100 Ω differential source impedance, and must be terminated with a 100 Ω differential load.

Receiver Rate Select (RS0) pin 7 is assigned to control the SFP+ module receiver rate. It is connected internally to a 30 kΩ pull-down resistor. A data signal on this pin has no affect on the operation of the receiver.

An open collector compatible loss of signal (LOS) is provided. The LOS must be pulled high on the host board for proper operation. A logic "0" indicates that light has been detected at the input to the receiver (see Optical characteristics, Loss of Signal Assert/Deassert Time). A logic "1" output indicates that insufficient light has been detected for proper operation.

3

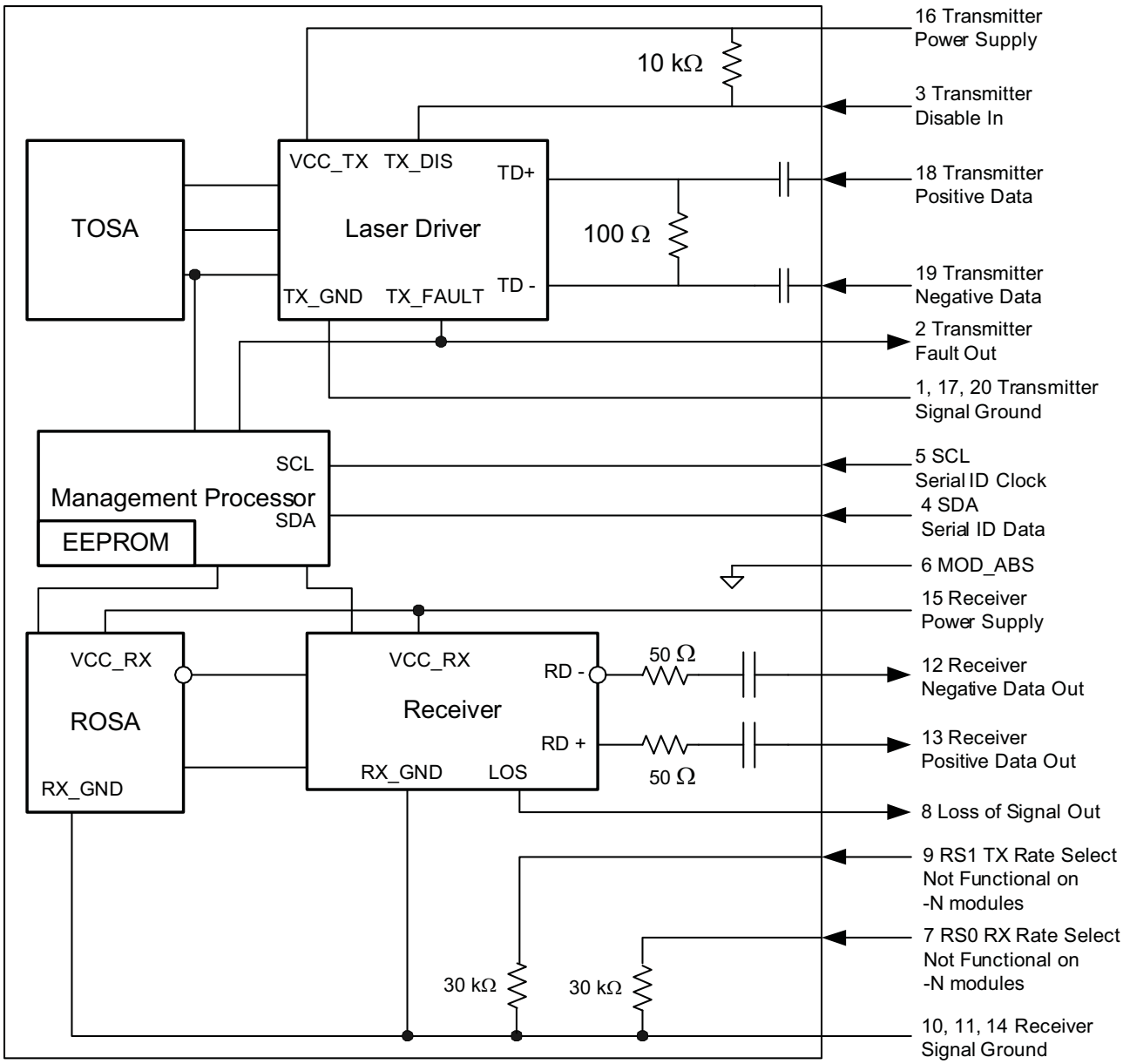


Figure 1 SFP+ optical transceiver functional block diagram

Section 2 Application Schematic

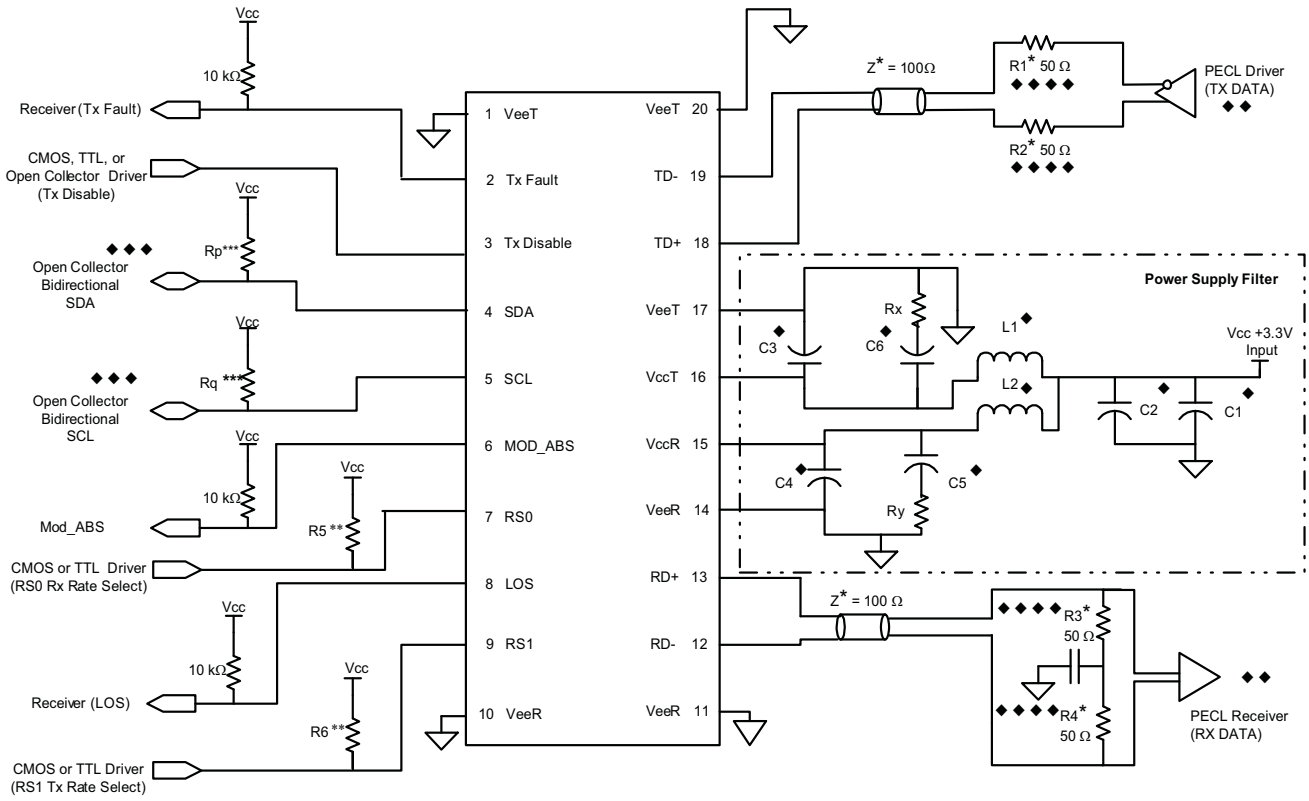


Figure 2 Recommended application schematic for the 10 G SFP+ optical transceiver

Notes

◆ Power supply filtering components should be placed as close to the V_{cc} pins of the host connector as possible for optimal performance.

◆◆ PECL driver and receiver components will require biasing networks. Please consult application notes from suppliers of these components. CML I/O on the PHY are supported. Good impedance matching for the driver and receiver is required.

◆◆◆ SDA and SCL should be bi-directional open collector connections in order to implement serial ID in JDSU SFP+ transceiver modules.

◆◆◆◆ R1/R2 and R3/R4 are normally included in the output and input of the PHY. Please check the application notes for the IC in use.

* Transmission lines should be 100 Ω differential traces. Vias and other transmission line discontinuities should be avoided. In order to meet the host TP1 output jitter and TP4 jitter tolerance requirements it is recommended that the PHY has both transmitter pre-emphasis to equalize the transmitter traces and receiver equalization to equalize the receiver traces. With appropriate transmitter pre-emphasis and receiver equalization, up to 8 dB of loss at 5 GHz can be tolerated.

** R5 and R6 are required when an Open Collector driver is used in place of CMOS or TTL drivers. 5 kΩ value is appropriate.

*** The value of R_p and R_q depend on the capacitive loading of these lines and the two wire interface clock frequency. See SFF-8431. A value of 10 kΩ is appropriate for 80 pF capacitive loading at 100 kHz clock frequency.

Power supply filtering is recommended for both the transmitter and receiver. Filtering should be placed on the host assembly as close to the Vcc pins as possible for optimal performance. $V_{cc,R}$ and $V_{cc,T}$ should have separate filters.

Power supply filter component values from Figure 2 are shown in the table below for two different implementations.

Power Supply Filter Component Values

Component	Option A	Option B	Units
L1, L2	1.0	4.7	µH
Rx, Ry	0.5*	0.5*	Ω
C1, C5	10	22	µF
C2, C3, C4	0.1	0.1	µF
C6	Not required	22	µF

Notes:
Option A is recommended for use in applications with space constraints. Power supply noise must be less than 100 mV_{p-p}.
Option B is used in the module compliance board in SFF-8431.
*If the total series resistance of L1+C6 and L2+C5 exceeds the values of Rx and Ry in the table, then Rx and Ry can be omitted.

Section 3 Specifications

Technical specifications related to the SFP+ optical transceiver include:

- Section 3.1 Pin Function Definitions
- Section 3.2 Absolute Maximum Ratings
- Section 3.3 Operating Conditions
- Section 3.4 Electrical Characteristics
- Section 3.5 Optical Characteristics
- Section 3.6 Link Length
- Section 3.7 Regulatory Compliance
- Section 3.8 PCB Layout
- Section 3.9 Front Panel Opening
- Section 3.10 Module Outline
- Section 3.11 Transceiver Belly-to-belly Mounting

3.1 Pin Function Definitions

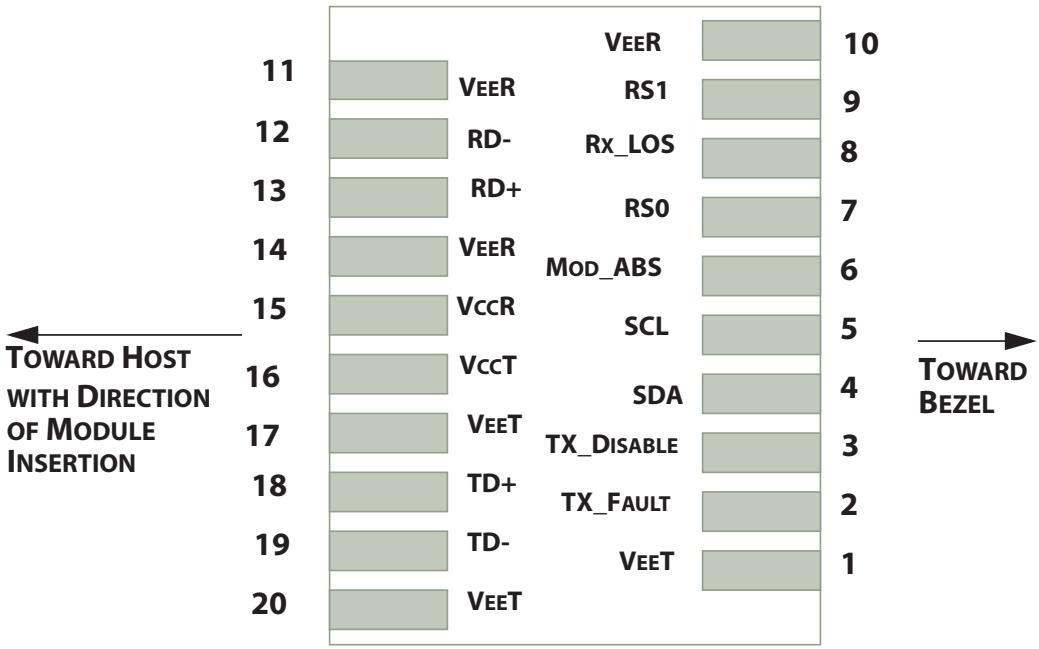


Figure 3 Host PCB SFP+ Pad assignment top view

7

SFP+ Optical Transceiver Pin Descriptions

Pin Number	Symbol	Name	Description
Receiver			
8	LOS	Loss of Signal Out (OC)	Sufficient optical signal for potential BER < $1x10^{-12}$ = Logic "0" Insufficient signal for potential BER < $1x10^{-12}$ = Logic "1" This pin is open collector compatible, and should be pulled up to Host V_{cc} with a 10 kΩ resistor.
10, 11, 14	V_{eeR}	Receiver Signal Ground	These pins should be connected to signal ground on the host board. The V_{eeR} and V_{eeT} signals are connected together within the module and are isolated from the module case.
12	RD-	Receiver Negative DATA Out (PECL)	Light on = Logic "0" Output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
13	RD+	Receiver Positive DATA Out (PECL)	Light on = Logic "1" Output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
15	V_{ccR}	Receiver Power Supply	This pin should be connected to a filtered +3.3 V power supply on the host board. See Application schematics on page 4 for filtering suggestions.
7	RS0	RX Rate Select (LVTTL)	This pin has an internal 30 kΩ pull-down to ground. A signal on this pin will not affect module performance.
Transmitter			
3	TX_Disable	Transmitter Disable In (LVTTL)	Logic "1" Input (or no connection) = Laser off Logic "0" Input = Laser on This pin is internally pulled up to V_{ccT} with a 10 kΩ resistor.
1, 17, 20	V_{eeT}	Transmitter Signal Ground	These pins should be connected to signal ground on the host board. The V_{eeR} and V_{eeT} signals are connected together within the module and are isolated from the module case.
2	TX_Fault	Transmitter Fault Out (OC)	Logic "1" Output = Laser Fault (Laser off before t_fault) This pin is open collector compatible, and should be pulled up to Host Vcc with a 10 kΩ resistor.
16	V_{ccT}	Transmitter Power Supply	This pin should be connected to a filtered +3.3 V power supply on the host board. See Application schematics on page 4 for filtering suggestions.
18	TD+	Transmitter Positive DATA In (PECL)	Logic "1" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
19	TD-	Transmitter Negative DATA In (PECL)	Logic "0" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
9	RS1	TX Rate Select (LVTTL)	This pin has an internal 30 kΩ pulldown to ground. A signal on this pin will not affect module performance.
Module Definition			
4	SDA	Two-wire Serial Data	Serial ID with SFF 8472 Diagnostics. Module definition pins should be pulled up to Host V_{cc} with appropriate resistors for the speed and capacitive loading of the bus. See SFF8431.
5	SCL	Two-wire Serial Clock	Serial ID with SFF 8472 Diagnostics. Module definition pins should be pulled up to Host V_{cc} with appropriate resistors for the speed and capacitive loading of the bus. See SFF8431.
6	MOD_ABS	Module Absent	Pin should be pulled up to Host V_{cc} with 10 kΩ resistor. MOD_ABS is asserted "high" when the SFP+ module is physically absent from the host slot.

3.2 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage temperature	T_{ST}	-40 to +95	˚C
Operating case temperature	T_C	-40 to +85	˚C
Relative humidity	RH	5 – 95 (noncondensing)	%
Transmitter differential input voltage	V_D	2.5	V
Power supply voltage	V_{CC}	0 to +4.0	V_{P-P}

Note:
Absolute maximum ratings represent the damage threshold of the device.
Damage may occur if the device is subjected to conditions beyond the limits stated here.

3.3 Operating Conditions

Part Number	Temperature Rating	Unit
PLRXPL-VC-S43-23-N	0 – 70	˚C

Note:
Performance is not guaranteed and reliability is not implied for operation at any condition outside these limits.

3.4 Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply voltage	V_{cc}	3.14	3.3	3.47	V	All electrical and optical specifications valid within this range
Power consumption	P_{diss}		480	1000	mW	
Data rate			10.3125	10.52	Gbps	BER < $1x10^{-12}$
Transmitter						
Supply current	I_{ccT}			100	mA	
Common mode voltage tolerance	ΔV	15			mV_{rms}	
Data dependent input jitter	DDJ			0.10	UI	2^9-1 pattern, TP1, at 10.3 Gbps (Note 1)
Data input uncorrelated jitter	Uj			0.023	UI (rms)	
Data input total jitter	TJ			0.28	UI	2^{31}-1 pattern, TP1, BER < $1x10^{-12}$, at 10.3 Gbps (Notes 1, 8)
Input data dependent pulse width shrinkage	DDPWS			0.055	UI	Reference SFF-8431 Revision 3.2
Eye mask	X1			0.12	UI	Reference SFF-8431 Revision 3.2,
	X2			0.33	UI	Figure 22. 5 x 10^{-5} hit ratio
	Y1	95			mV	
	Y2			800	mV	
Transmit disable voltage levels	V_{IH}	2.0		V_{cc} + 0.3	V	Laser output disabled after T_{TD} if
	V_{IL}	-0.3		0.8	V	input level is V_{IH}; Laser output enabled after T_{TEN} if input level is V_{IL}
Transmit disable/enable assert time	T_{TD}			10	µs	Laser output disabled after T_{TD} if
	T_{TEN}			2	ms	input level is V_{IH}; Laser output enabled after T_{TEN} if input level is V_{IL}
Transmit fault output levels	I_{OH}	-50		+37.5	µA	Fault level is I_{OH} and Laser output
	V_{OL}	-0.3		0.4	V	disabled T_{Fault} after laser fault. I_{OH} is measured with a 4.7 kΩ load to V_{cc} host. V_{OL} is measured at 0.7 mA.
Transmit fault assert and reset times	T_{Fault}			100	µs	Fault is V_{OL} and Laser output restored
	T_{Reset}	10			µs	T_{INI} after disable is asserted for T_{Reset}, then disabled.
Initialization time	T_{INI}			300	ms	After hot plug or $V_{cc} \geq 2.97$ V
Receiver						
Supply current	I_{ccR}			120	mA	
Data output rise/fall time	tr/tf	28			ps	20% – 80%, differential
Output common mode voltage				7.5	mV_{rms}	R_{LOAD} = 25 Ω, common mode
99% jitter				0.42	UI	2^{31}-1 pattern, TP4, at 10.3 Gbps (Notes 1, 4, 9)
Total jitter	TJ			0.70	UI	2^{31}-1 pattern, TP4 , BER < $1x10^{-12}$, at 10.3 Gbps (Notes 1, 4, 8)
Eye mask	X1			0.35	UI	Reference SFF-8431 Revision 3.2,
	Y1	200			mV	Figure 23. 5 x 10^{-5} hit ratio
	Y2			425	mV	
Loss of signal levels	I_{OH}	-50		+37.5	µA	LOS output level I_{OL} T_{LOSD} after light input > LOSD (Note 2)
	V_{OL}	-0.3		0.4	V	LOS output level V_{OH} T_{LOSA} after light input < LOSA (Note 2)
Loss of signal assert/deassert time	T_{LOSA}			100	µs	LOS output level V_{OL} T_{LOSD} after light input > LOSD (Note 2)
	T_{LOSD}			100	µs	LOS output level V_{OH} T_{LOSA} after light input < LOSA (Note 2)

Note: All high frequency measurements are made with the module compliance board as described in SFF8431

3.5 Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Wavelength	λ_p	840	850	860	nm	
RMS spectral width				0.45	nm	
Average optical power	P_{AVG}	-8		Note 6	dBm	
Optical modulation amplitude	OMA	*			µW	
Transmitter dispersion penalty	TDP			3.9	dB	(Note 3)
Relative intensity noise	$RIN_{12}OMA$			-128	dB/Hz	12 dB reflection
Receiver						
Wavelength	λ	840	850	860	nm	
Maximum input power	P_{max}	+1			dBm	Exceeds IEEE 802.3 Clause 52
Sensitivity (OMA)	S			-10.7	dBm	(Note 7)
Stressed sensitivity (OMA)	ISI = 2.8 dB			-7.8	dBm	
Loss of signal assert/deassert level	LOSD			-11	dBm	Chatter-free operation; LOSD is
	LOSA	-30			dBm	OMA, LOSA is average power
Low frequency cutoff	F_C			0.3	MHz	-3 dB, P<-16 dBm

Note:
* Tradeoffs between center wavelength, spectral width, and minimum OMA are used. Refer to the table on Minimum Optical Modulation Amplitude in dBm for details.

Minimum Optical Modulation Amplitude in dBm

Wavelength (nm)	Spectral Width (nm)							
	<0.1	0.1 – 0.15	0.15 – 0.2	0.2 – 0.25	0.25 – 0.30	0.3 – 0.35	0.35 – 0.4	0.4 – 0.45
840 – 845	-4.3	-4.2	-4.2	-4.1	-4.1	-4.0	-3.9	-3.7
845 – 850	-4.3	-4.2	-4.2	-4.2	-4.1	-4.0	-3.9	-3.8
850 – 855	-4.3	-4.3	-4.2	-4.2	-4.1	-4.0	-3.9	-3.8
855 – 860	-4.3	-4.3	-4.2	-4.2	-4.1	-4.1	-4.0	-3.9

Note:
* Tradeoffs between center wavelength, spectral width, and minimum OMA are used.

3.6 Link Length

Data Rate / Standard	Fiber Type	Modal Bandwidth at 850 nm (MHz*km)	Distance Range (m)	Notes
10.3 GBd	62.5/125 µm MMF	200	0.5 – 20	5
	50/125 µm MMF	500	0.5 – 50	5
	50/125 µm MMF	900	0.5 – 90	5
	50/125 µm MMF	1500	0.5 – 160	5
	50/125 µm MMF	2000	0.5 – 200	5

Specification Notes

1. UI (unit interval): one UI is equal to one bit period. For example, 10.3125 Gbps corresponds to a UI of 96.97 ps.
2. For LOSA and LOSD definitions, see Loss of Signal Assert/Deassert Level in Optical Characteristics.
3. Transmitter dispersion penalty is measured using the methods specified in the IEEE standard 802.3-2005 Clause 52 except that the transversal filter differential delay is 33 ps.
4. Measured with stressed eye pattern as per IEEE standard 802.3-2005, Clause 52 except that the vertical eye opening penalty is as specified in Optical Characteristics.
5. Distances, shown in the “Link Length” table, are calculated for worst-case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques specified in IEEE 802.3. In the nominal case, longer distances are achievable.
6. The maximum transmitter output power is the lesser of the Class 1 laser eye safety limit and -1 dBm (the maximum receiver input power limit per the IEEE 802.3 Clause 52 specification).
7. Sensitivity is for informational purposes only.
8. The data pattern for the total jitter measurement is one of IEEE 802.3 Clause 52.9 Pattern 1, Pattern 3, or valid 64/66B data traffic.
9. 99% jitter is as defined in SFF-8431 Revision 3.2. 99% jitter has the same definition as “all but 1% for jitter” as used in IEEE 802.3 Clause 52.9.9 and is defined as the time from the 0.5th to the 99.5th percentile of the jitter histogram.

3.7 Regulatory Compliance

The PLRXPL-Vx-S43-23-N optical transceiver complies with international Electromagnetic Compatibility (EMC) and international safety requirements and standards. EMC performance is dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

The PLRXPL-Vx-S43-23-N optical transceiver is lead-free and RoHS-compliant per Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Regulatory Compliance

Feature	Test Method	Performance
Component safety	UL 60950 UL 94, V0 IEC 60950	UL File E209897 TUV Report/Certificate (CB scheme)
RoHS-compliant	Directive 2002/95/EC	Compliant per the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
Laser eye safety[1]	EN 60825 U. S. 21CFR 1040.10	TUV Certificate CDRH compliant and Class 1 laser eye safe
Electromagnetic Compatibility		
Electromagnetic emissions	EMC Directive 89/336/EEC FCC CFR47 Part 15 IEC/CISPR 22 AS/NZS CISPR22 EN 55022 ICES-003, Issue 4 VCCI-03	Noise frequency range: 30 MHz to 40 GHz. Good system EMI design practice required to achieve Class B margins.
Electromagnetic immunity	EMC Directive 89/336/EEC IEC/CISPR/24 EN 55024	
ESD immunity	EN 61000-4-2	Exceeds requirements. Withstand discharges of 4 kV contact and 8 kV air discharge to Criterion A, and 8 kV contact and 25 kV air discharge to Criterion B.
Radiated immunity	EN 61000-4-3	Exceeds requirements. Field strength of 10 V/m RMS, from 10 MHz to 1 GHz. No effect on transmitter/receiver performance is detectable between these limits.

1. For further details, see Eye Safety

3.8 PCB Layout

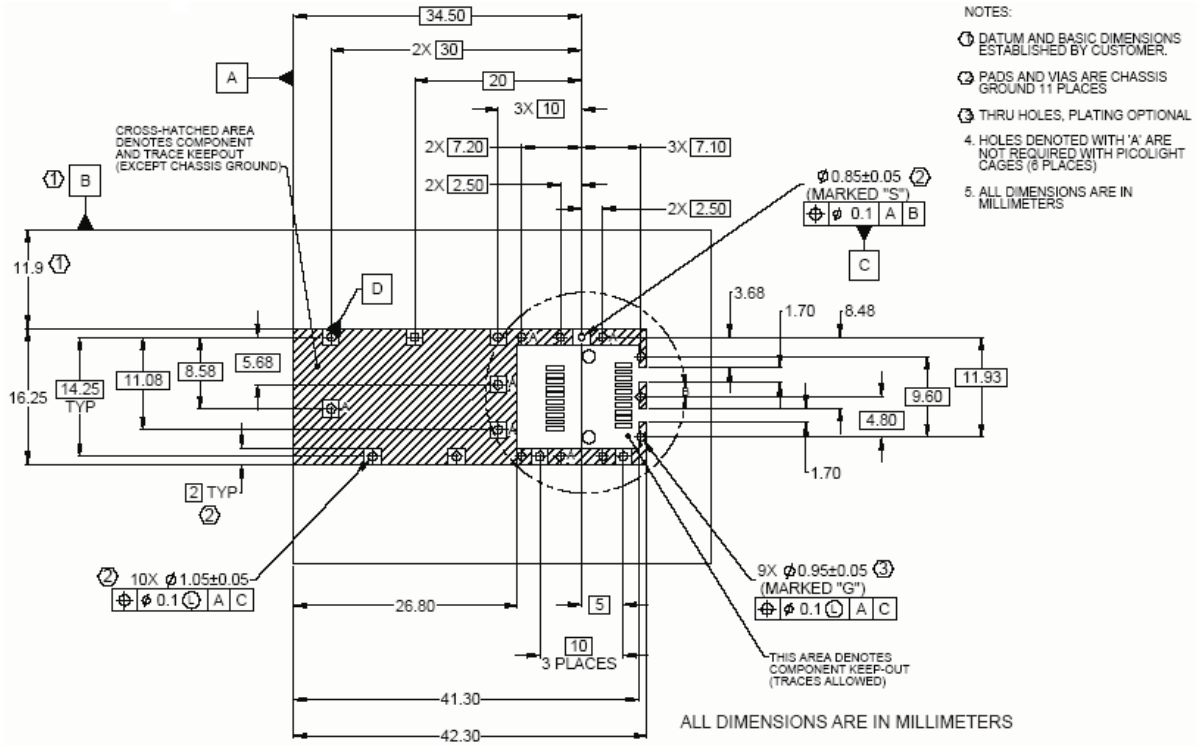


Figure 4 Board layout

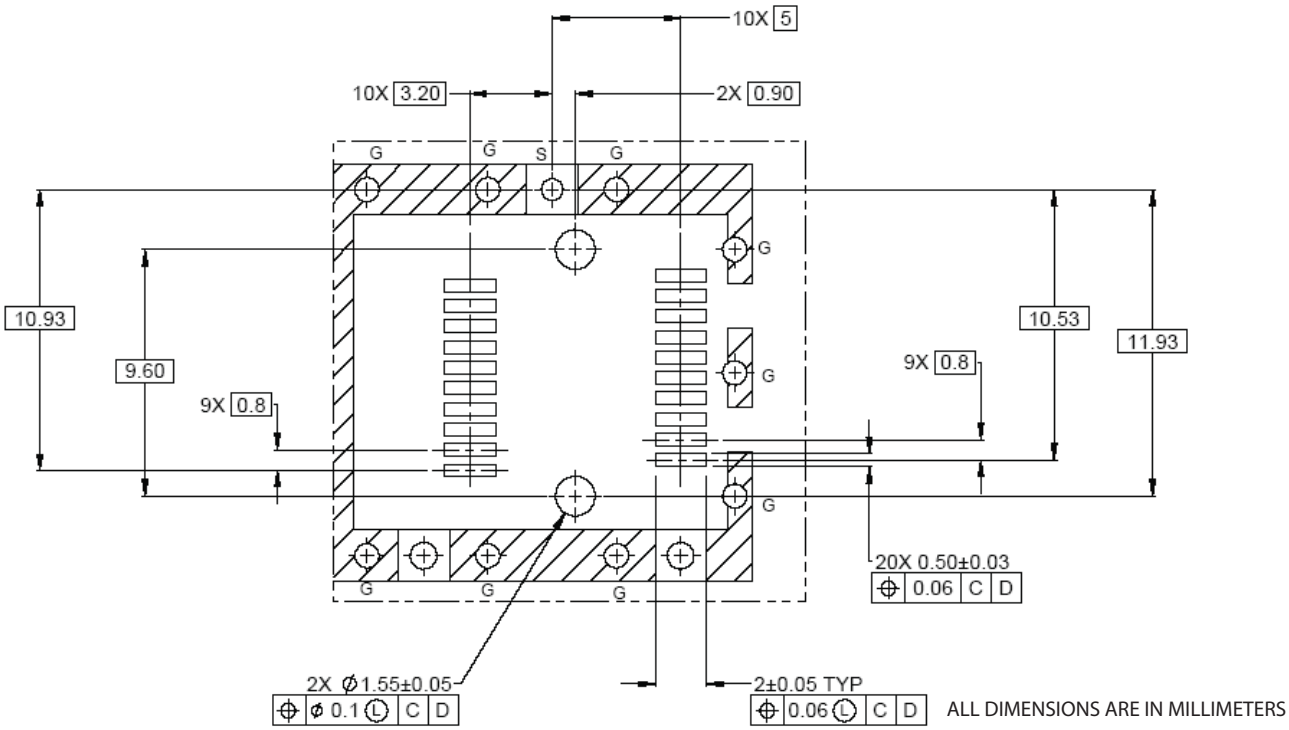


Figure 5 Detail layout

3.9 Front Panel Opening

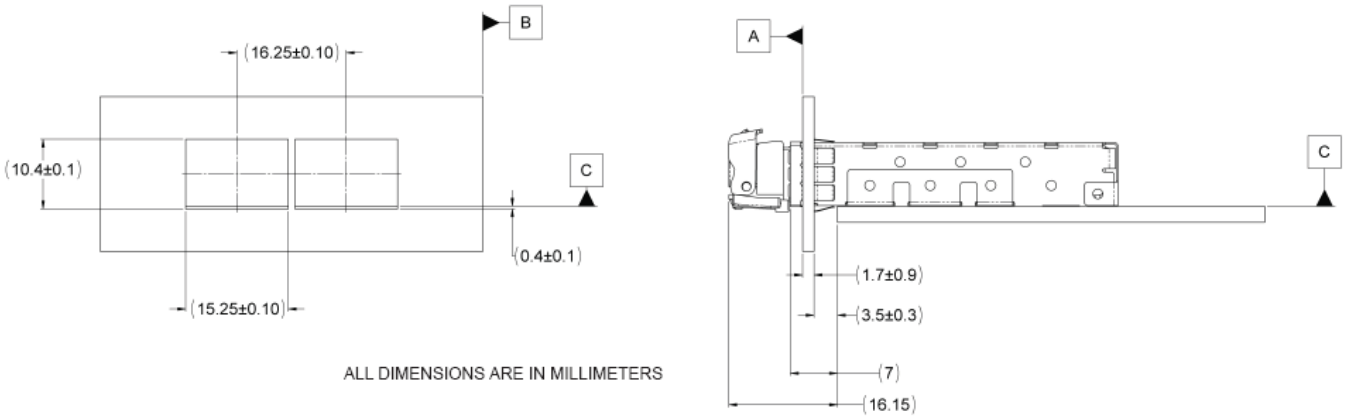


Figure 6

3.10 Module Outline

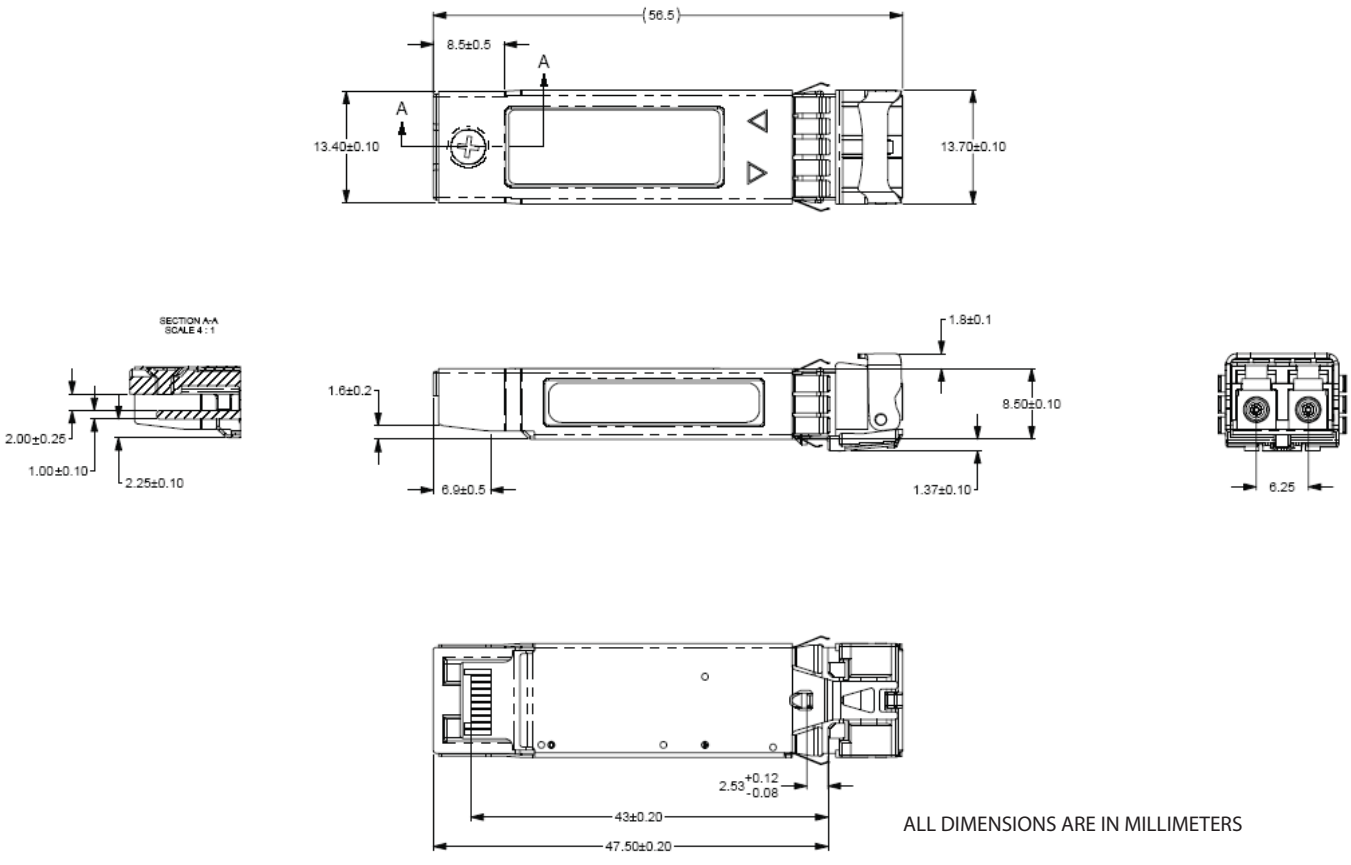


Figure 7

3.11 Transceiver Belly-to-belly Mounting

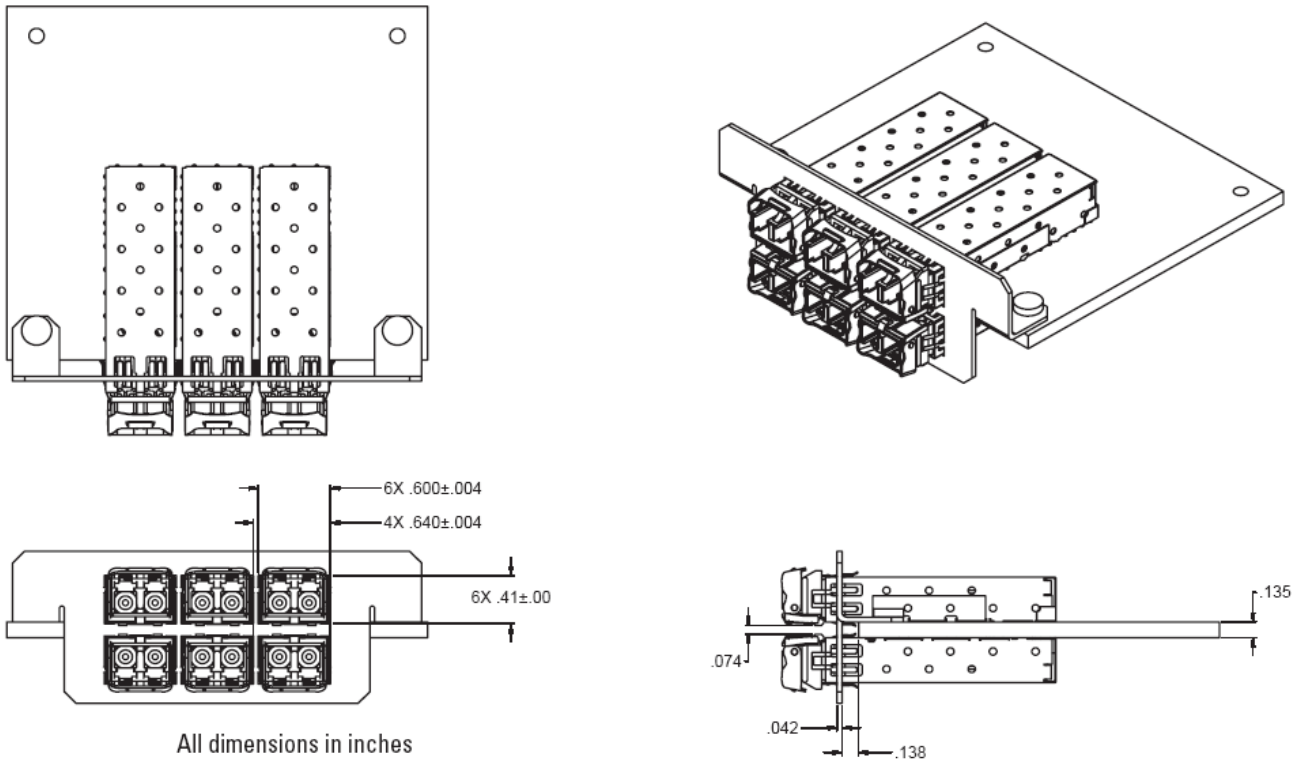


Figure 8

Section 4 Related Information

Other information related to the SFP+ optical transceiver includes:

- Section 4.1 Digital diagnostic monitoring and serial ID operation
- Section 4.2 Package and handling instructions
- Section 4.3 ESD discharge (ESD)
- Section 4.4 Eye safety

4.1 Digital Diagnostic Monitoring and Serial ID Operation

The PLRXPL-Vx-S43-23-N optical transceiver is equipped with a two-wire serial EEPROM that is used to store specific information about the type and identification of the transceiver as well as real-time digitized information relating to the transceiver's performance. See the Small Form Factor Committee document number SFF-8472 Revision 10.3, dated December 1, 2007 for memory/address organization of the identification data and digital diagnostic data. The enhanced digital diagnostics feature monitors five key transceiver parameters which are internally calibrated and should be read as absolute values and interpreted as follows:

Transceiver Temperature in degrees Celsius: Internally measured. Represented as a 16-bit signed two's complement value in increments of 1/256°C from -40 to +70°C with LSB equal to 1/256°C. Accuracy is ± 3°C over the specified operating temperature and voltage range.

Vcc/Supply Voltage in Volts: Internally measured. Represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value(0 – 65535) with LSB equal to 100 uV with a measurement range of 0 to +6.55 V. Accuracy is ± three percent of nominal value over the specified operating temperature and voltage ranges.

TX Bias Current in mA: Represented as a 16-bit unsigned integer with current defined as the full 16-bit value (0 – 65535) with LSB equal to 2 uA with a measurement range of 0 – 131 mA. Accuracy is ± 10 percent of nominal value over the specified operating temperature and voltage ranges.

TX Output Power in mW: Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 – 65535) with LSB equal to 0.1 uW. Accuracy is ± 2 dB over the specified temperature and voltage ranges over the range of -8.2 dBm to 0.5 dBm. Data is not valid when transmitter is disabled.

RX Received Optical Power in mW: Represented as average power as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to 0.1 uW. Accuracy is ± 3 dB over the specified temperature and voltage ranges over the power range of -12 dBm to 0.5 dBm.

Reading the data

The information is accessed through the SCL and SDA connector pins of the module. The SFF-8431 Revision 3.2 specification contains all the timing and addressing information required for accessing the data in the EEPROM.

The device address used to read the Serial ID data is 1010000X(A0h), and the address to read the diagnostic data is 1010001X(A2h). Any other device addresses will be ignored.

MOD_ABS, pin 6 on the transceiver, is connected to Logic 0 (Ground) on the transceiver.

SCL, pin 5 on the transceiver, is connected to the SCL pin of the EEPROM.

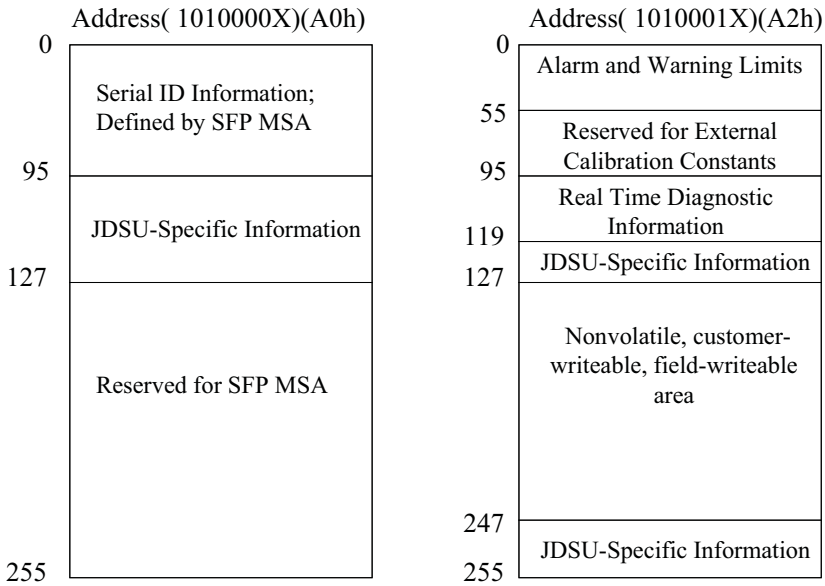
SDA, pin 4 on the transceiver, is connected to the SDA pin of the EEPROM.

The EEPROM Write Protect pin is internally tied to ground with no external access, allowing write access to the customer-writable field (bytes 128 – 247 of address 1010001X). Note: address bytes 0 – 127 are not write protected and may cause diagnostic malfunctions if written over.

Decoding the data

The information stored in the EEPROM, including the organization and the digital diagnostic information, is defined in the Small Form Factor Committee document SFF-8472 Revision 10.3, dated December 1, 2007.

Data Field Descriptions



Serial ID Data and Map

Memory Address	Value	Comments
0	03	SFP Transceiver
1	04	SFP with Serial ID
2	07	LC Connector
3-10	0000000000000000	
11	06	64B/66B
12	67	Nominal Bit rate of 10.3 Gbps
13	00	Rate Identifier (for Rate-selectable modules)
14	00	Single-mode fiber not supported
15	00	Single-mode fiber not supported
16	05	50 meters of OM2 50/125 µm multimode fiber
17	02	20 meters of OM1 62.5/125 µm multimode fiber
18	00	Copper not supported
19	14	200 meters of OM3 50/125 µm multimode fiber
20-35	JDSU	Vendor Name (ASCII)
36	00	Reserved
37-39	00019C	IEEE Company ID (ASCII)
40-55	PLRXPLVxS43xxN	Part Number (ASCII), x = part number variable
56-59		Revision of part number (ASCII)
60-61	0352	Wavelength of laser in nm; 850
62		Unallocated
63	CC_BASE	Check Code; Lower 8 bits of sum from byte 0 through 62
64	00	Conventional uncooled laser, Class 1 power level, Conventional limiting receiver output
65	1A	Tx_Disable, Tx Fault, Loss of Signal implemented
66	00	
67	00	
68-83		Serial Number (ASCII)
84-91		Date Code (ASCII)
92	68	Diagnostic monitoring implemented, internally calibrated, Receiver Power Measurement type is Average Power
93	F0	Alarms and Warnings, TX_Fault and Rx_LOS monitoring implemented, TX_Disable Control and Monitoring.
94	03	SFF-8472 Revision 10.3 compliant
95	CC_EXT	Check Code; Lower 8 bits of sum from byte 64 through 94
96-127		JDSU-specific EEPROM
128-255		Reserved for SFF-8079

Diagnostics Data Map

Memory Address	Value	Comments
00-01	Temp High Alarm	MSB at low address
02-03	Temp Low Alarm	MSB at low address
04-05	Temp High Warning	MSB at low address
06-07	Temp Low Warning	MSB at low address
08-09	Voltage High Alarm	MSB at low address
10-11	Voltage Low Alarm	MSB at low address
12-13	Voltage High Warning	MSB at low address
14-15	Voltage Low Warning	MSB at low address
16-17	Bias High Alarm	MSB at low address
18-19	Bias Low Alarm	MSB at low address
20-21	Bias High Warning	MSB at low address
22-23	Bias Low Warning	MSB at low address
24-25	TX Power High Alarm	MSB at low address
26-27	TX Power Low Alarm	MSB at low address
28-29	TX Power High Warning	MSB at low address
30-31	TX Power Low Warning	MSB at low address
32-33	RX Power High Alarm	MSB at low address
34-35	RX Power Low Alarm	MSB at low address
36-37	RX Power High Warning	MSB at low address
38-39	RX Power Low Warning	MSB at low address
40-55	Reserved	For future monitoring quantities
56-59	RP4	External Calibration Constant
60-63	RP3	External Calibration Constant
64-67	RP2	External Calibration Constant
68-71	RP1	External Calibration Constant
72-75	RP0	External Calibration Constant
76-77	Islope	External Calibration Constant
78-79	Ioffset	External Calibration Constant
80-81	TPslope	External Calibration Constant
82-83	TPoffset	External Calibration Constant
84-85	Tslope	External Calibration Constant
86-87	Toffset	External Calibration Constant
88-89	Vslope	External Calibration Constant
90-91	Voffset	External Calibration Constant
92-94	Reserved	Reserved
95	Checksum	Low order 8 bits of sum from 0 – 94
96	Temperature MSB	Internal temperature AD values
97	Temperature LSB	
98	Vcc MSB	Internally measured supply voltage AD values
99	Vcc LSB	
100	TX Bias MSB (Note 1)	TX Bias Current AD values

Diagnostics Data Map (continued)

Memory Address	Value	Comments
101	TX Bias LSB (Note 1)	
102	TX Power MSB (Note 1)	Measured TX output power AD values
103	TX Power LSB (Note 1)	
104	RX Power MSB	Measured RX input power AD values
105	RX Power LSB	
106	Reserved MSB	For 1st future definition of digitized analog input
107	Reserved LSB	
108	Reserved MSB	For 2nd future definition of digitized analog input
109	Reserved LSB	
110-7	Tx Disable State	Digital State of Tx Disable Pin
110-6	Soft Tx Disable Control	Writing "1" OR pulling the Tx_Disable pin will disable the laser
110-5	Reserved	
110-4	Rate Select State	Digital State of Rate Select Pin
110-3	Soft Rate Select Control	Writing to this bit has no effect
110-2	Tx Fault State	Digital State
110-1	LOS State	Digital State
110-0	Data Ready State	Digital State; "1" until transceiver is ready
111	Reserved	Reserved
112-119	Optional alarm & warning flag bits (Note 2)	Refer to SFF-8472 Revision 10.3
120-127	Vendor specific	JDSU specific
128-247	User/Customer EEPROM	Field writeable EEPROM
248-255	Vendor specific	Vendor-specific control

Note :
1. During Tx disable, Tx bias and Tx power will not be monitored.
2. Alarm and warning are latched. The flag registers are cleared when the system Reads AND the alarm/warning condition no longer exists.

4.2 Package and Handling Instructions

This product is not compatible with any aqueous wash process.

Process plug
The PLRXPL-Vx-S43-23-N optical transceiver is supplied with a process plug. This plug protects the transceiver optics during standard manufacturing processes by preventing contamination from air borne particles.

Note: It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.

Recommended cleaning and degreasing chemicals
JDSU recommends the use of methyl, isopropyl and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

Flammability
The housing is made of cast zinc and sheet metal.

4.3 Electrostatic Discharge (ESD)

Handling
Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and operation
In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event may require the application to reacquire synchronization at the higher layers (serializer/deserializer chip).

4.4 Eye Safety

The PLRXPL-Vx-S43-23-N Optical Transceiver is a CLASS 1 LASER PRODUCT as defined by the international standard IEC 60825-1 Second Edition 2007-03 and by U.S.A. regulations for Class 1 products per CDRH 21 CFR 1040.10 and 1040.11. Laser emissions from Class 1 laser products are not considered hazardous when operated according to product specifications. Operating the product with a power supply voltage exceeding 4.0 volts may compromise the reliability of the product, and could result in laser emissions exceeding Class 1 limits.

Caution

Tampering with this laser based product or operating this product outside the limits of this specification may be considered an act of "manufacturing," and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (21 CFR 1040).

The use of optical instruments with this product will increase eye hazard.

Ordering Information

For more information on this or other products and their availability, please contact your local JDSU account manager or JDSU directly at 1-800-498-JDSU (5378) in North America and +800-5378-JDSU worldwide, or via e-mail at customer.service@jdsu.com.

Sample: PLRXPL-VC-S43-23-N

Part Number	Product Description
PLRXPL-VC-S43-23-N	10 G SFP+ SR compatible, limiting electrical interface, 0 – 70°C, ± 5% Vcc, no rate select, generic