

DATA SHEET

PEMD9; PUMD9
NPN/PNP resistor-equipped
transistors;
R1 = 10 k Ω , R2 = 47 k Ω

Product data sheet
Supersedes data of 2003 Nov 04

2004 Apr 15

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PEMD9; PUMD9

FEATURES

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
TR1	NPN	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	10	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

NPN/PNP resistor-equipped transistors in a SOT666 plastic package.

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD9	SOT666	–	D9	PEMB9	PEMH9
PUMD9	SOT363	SC-88	D*9 ⁽¹⁾	PUMB9	PUMH9

Note

- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD9; PUMD9	<p>Top view MAM448</p>	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD9	–	plastic surface mounted package; 6 leads	SOT666
PUMD9	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage TR1 positive negative		–	+40	V
			–	–6	V
V _I	input voltage TR2 positive negative		–	+6	V
			–	–40	V
I _o	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation SOT363 SOT666	T _{amb} ≤ 25 °C;	–	–	
		note 1	–	200	mW
		notes 1 and 2	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation SOT363 SOT666	T _{amb} ≤ 25 °C;	–	–	
		note 1	–	300	mW
		notes 1 and 2	–	300	mW

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
R _{th(j-a)}	thermal resistance from junction to ambient			
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
R _{th(j-a)}	thermal resistance from junction to ambient			
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	–	–	150	μ A
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	100	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 5 mA; I _B = 0.25 mA	–	–	100	mV
V _{i(off)}	input-off voltage	V _{CE} = 5 V; I _C = 100 μ A	–	0.7	0.5	V
V _{i(on)}	input-on voltage	V _{CE} = 0.3 V; I _C = 1 mA	1.4	0.8	–	V
R1	input resistor		7	10	13	k Ω
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
C _c	collector capacitance					
	TR1 (NPN)	V _{CB} = 10 V; I _E = i _e = 0 A; f = 1 MHz	–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

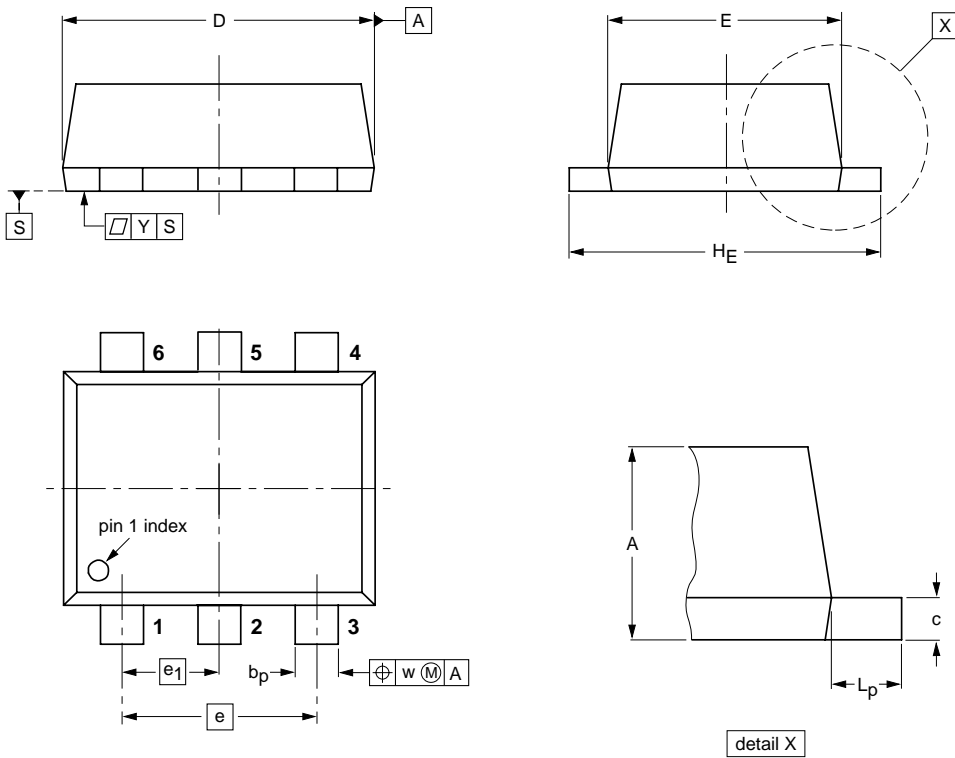
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PACKAGE OUTLINES

Plastic surface-mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

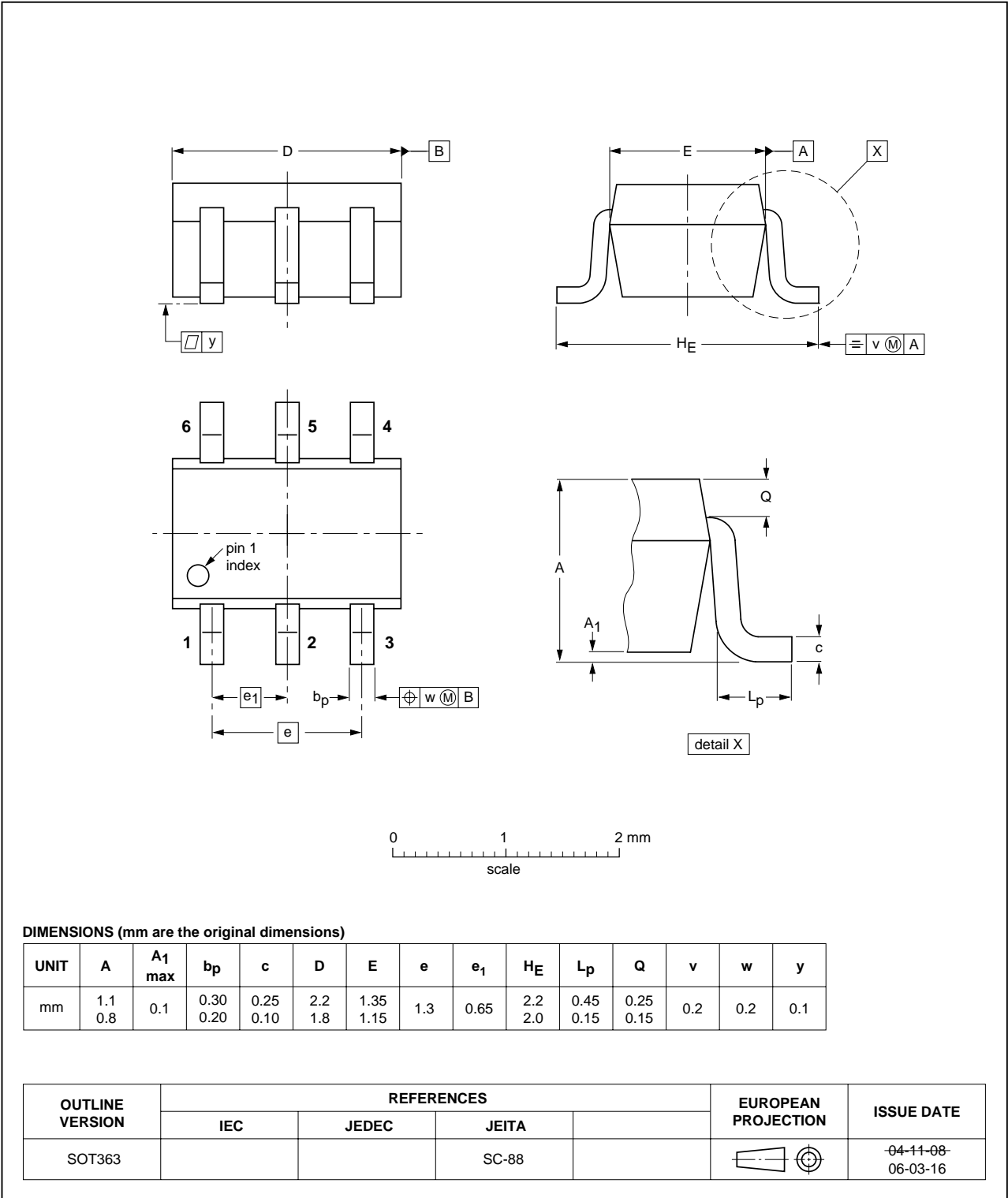
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT666					04-11-08 06-03-16

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DATA SHEET STATUS

DOCUMENT STATUS⁽¹⁾	PRODUCT STATUS⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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