19-4442; Rev 0; 2/09

EVALUATION KIT AVAILABLE

Low-Jitter Frequency Synthesizer with Selectable Input Reference

MAX3673

General Description

The MAX3673 is a low-jitter frequency synthesizer that accepts two reference clock inputs and generates nine phase-aligned outputs. The device features 40kHz jitter transfer bandwidth, 0.3ps$_{RMS}$ (12kHz to 20MHz) integrated phase jitter, and best-in-class power-supply noise rejection (PSNR), making it ideal for jitter clean-up, frequency translation, and clock distribution in wireless base-station applications.

The MAX3673 operates from a single +3.3V supply and typically consumes 400mW. The IC is available in an 8mm x 8mm, 56-pin TQFN package, and operates from -40°C to +85°C.

Applications

3G Wireless Base Stations

Frequency Translation

Jitter Cleanup

Clock Distribution

Pin Configuration and Typical Application Circuits appear at end of data sheet.

Features

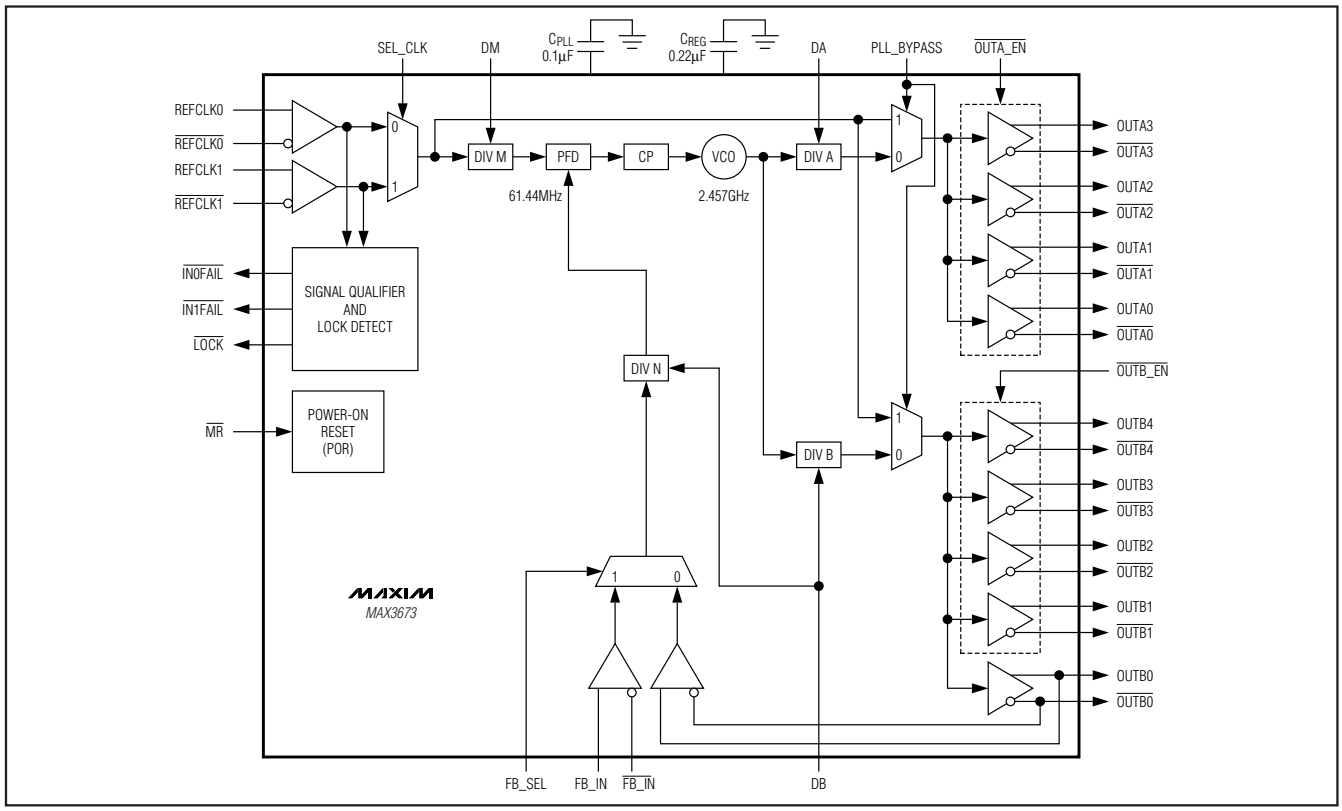
- **Two Reference Clock Inputs: LVPECL**
- **Nine Phase-Aligned Clock Outputs: LVPECL**
- **Input Frequencies: 61.44MHz,122.88MHz, 245.76MHz, 307.2MHz**
- **Output Frequencies: 61.44MHz, 122.88MHz, 153.6MHz, 245.76MHz, 307.2MHz**
- **Low-Jitter Generation: 0.3ps$_{RMS}$ (12kHz to 20MHz)**
- **Clock Failure Indicator for Both Reference Clocks**
- **External Feedback Provides Zero-Delay Capability**
- **Low Output Skew: 20ps Typical**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3673ETN+	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Functional Diagram



Low-Jitter Frequency Synthesizer with Selectable Input Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}, VCC_VCO).....-0.3V to +4.0V
LVPECL Output Current (OUTA[3:0], $\overline{OUTA[3:0]}$, OUTB[4:0], $\overline{OUTB[4:0]}$) .....-56mA
All Other Pins.....-0.3V to (V_{CC} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above 70°C).....3808mW
Operating Junction Temperature (T_J).....-55°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	LVPECL outputs unterminated		120	175	mA
POWER-ON RESET						
V_{CC} Rising		(Note 1)		2.55		V
V_{CC} Falling		(Note 1)		2.45		V
LVCMOS/LVTTL INPUTS ($\overline{MR}$, SEL_CLK, PLL_BYPASS, FB_SEL)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC}			75	µA
Input Low Current	I_{IL}	V_{IN} = GND	-75			µA
LVCMOS/LVTTL OUTPUTS ($\overline{IN0FAIL}$, $\overline{IN1FAIL}$, $\overline{LOCK}$)						
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +8mA			0.4	V
LVPECL INPUTS (REFCLK0, $\overline{REFCLK0}$, REFCLK1, $\overline{REFCLK1}$, FB_IN, $\overline{FB\_IN}$) (Note 2)						
Input High Voltage	V_{IH}				V_{CC} - 0.7	V
Input Low Voltage	V_{IL}		V_{CC} - 2.0			V
Input Bias Voltage	V_{CMI}		V_{CC} - 1.8	V_{CC} - 1.34		V
Differential-Input Swing			0.15		1.9	V_{P-P}
Differential-Input Impedance				> 40		kΩ
Common-Mode Input Impedance				> 14		kΩ
Input Capacitance				1.5		pF
Input Current		V_{IH} = V_{CC} - 0.7V, V_{IL} = V_{CC} - 2.0V	-100		+100	µA
Input Inrush Current When Power is Off (Steady State)	I_{DC}	(Notes 3, 4)		8		mA
Input Inrush Current Overshoot When Power is Off	$I_{OVERSHOOT}$	(Notes 3, 4)		6		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE CLOCK INPUTS (REFCLK0, $\overline{\text{REFCLK0}}$, REFCLK1, $\overline{\text{REFCLK1}}$)						
Reference Clock Frequency	f_{REF}			Table 1		MHz
Reference Clock Frequency Tolerance			-200		+200	ppm
Reference Clock Duty Cycle			40		60	%
Reference Clock Amplitude Detection Assert Threshold	V_{DT}	Differential swing (Notes 5, 6)		200		mV_{P-P}
LVPECL OUTPUTS (OUTA[3:0], $\overline{\text{OUTA[3:0]}}$, OUTB[4:0], $\overline{\text{OUTB[4:0]}}$) (Note 7)						
Output High Voltage	V_{OH}		V_{CC} - 1.13	V_{CC} - 0.98	V_{CC} - 0.83	V
Output Low Voltage	V_{OL}		V_{CC} - 1.85	V_{CC} - 1.70	V_{CC} - 1.55	V
Differential-Output Swing			1.1	1.45	1.8	V_{P-P}
Output Current When Disabled		V_O = V_{CC} - 2.0V to V_{CC} - 0.7V			130	µA
Output Frequency	f_{OUT}			Tables 2, 3		MHz
Output Rise/Fall Time	t_R, t_F	20% to 80% (Note 8)	150		500	ps
Output Duty Cycle		PLL_BYPASS = 0	48		52	%
		PLL_BYPASS = 1 (Note 9)	45		55	
Output-to-Output Skew	t_{SKEW}	Within output bank		20		ps
		All outputs		40		
OTHER AC ELECTRICAL SPECIFICATIONS						
PLL Jitter Transfer Bandwidth				40		kHz
Jitter Peaking				0.1		dB
PFD Compare Frequency				61.44		MHz
VCO Center Frequency				2.457		GHz
Random Jitter Generation		Integrated 12kHz to 20MHz (Notes 5, 8)		0.3	1.0	ps_{RMS}
Determinisitic Jitter Caused by Power-Supply Noise		(Note 10)		5		ps_{P-P}
Frequency Difference Between Reference Clock and VCO Within Which the PLL is Considered in Lock				500		ppm
Frequency Difference Between Reference Clock and VCO at Which the PLL is Considered Out-of-Lock				800		ppm
PLL Lock Time	t_{LOCK}	Figure 2		600		µs

Low-Jitter Frequency Synthesizer with Selectable Input Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, C_{PLL} = 0.1µF, C_{REG} = 0.22µF. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Master Reset ($\overline{MR}$) Minimum Pulse Width				100		ns
Propagation Delay from Input to FB_IN		FB_SEL = 1 (Notes 8, 11)	-120		+120	ps
Propagation Delay from Input to Any Output		PLL_BYPASS = 1		1.0		ns

Note 1: During the power-on-reset time, the LVPECL outputs are held to logic-low (OUTxx = low, $\overline{OUTxx}$ = high). See the *Power-On-Reset (POR)* section for more information.
Note 2: LVPECL inputs can be AC- or DC-coupled.
Note 3: For hot-pluggable purposes, the device can receive LVPECL inputs when no supply voltage is applied. Measured with V_{CC} pins connected to GND. See Figure 1.
Note 4: Measured with LVPECL input (V_{IH}, V_{IL}) as specified.
Note 5: Measured using reference clock input with 550ps rise/fall time (20% to 80%).
Note 6: When input differential swing is below the specified threshold, a clock failure is declared. See Figure 4.
Note 7: LVPECL outputs terminated 50Ω to V_{TT} = V_{CC} - 2V.
Note 8: Guaranteed by design and characterization.
Note 9: Measured with 50% duty cycle at reference clock input.
Note 10: Measured with 50mV_{P-P} sinusoidal noise on the power supply, f_{NOISE} = 100kHz.
Note 11: Measured with $f_{REFCLKx}$ = f_{FB_IN} and matched slew rates.

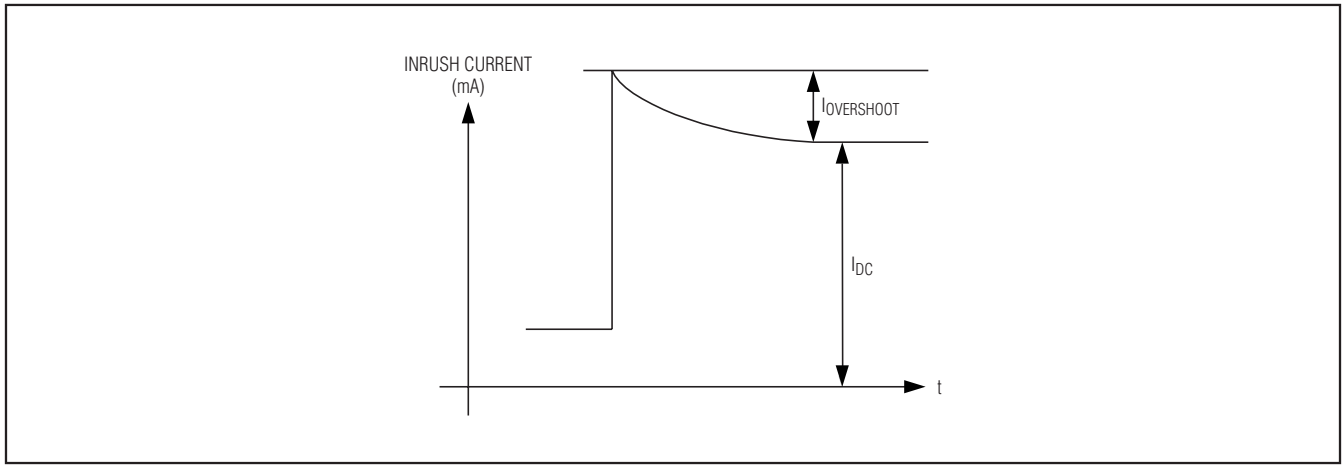


Figure 1. LVPECL Input Inrush Current

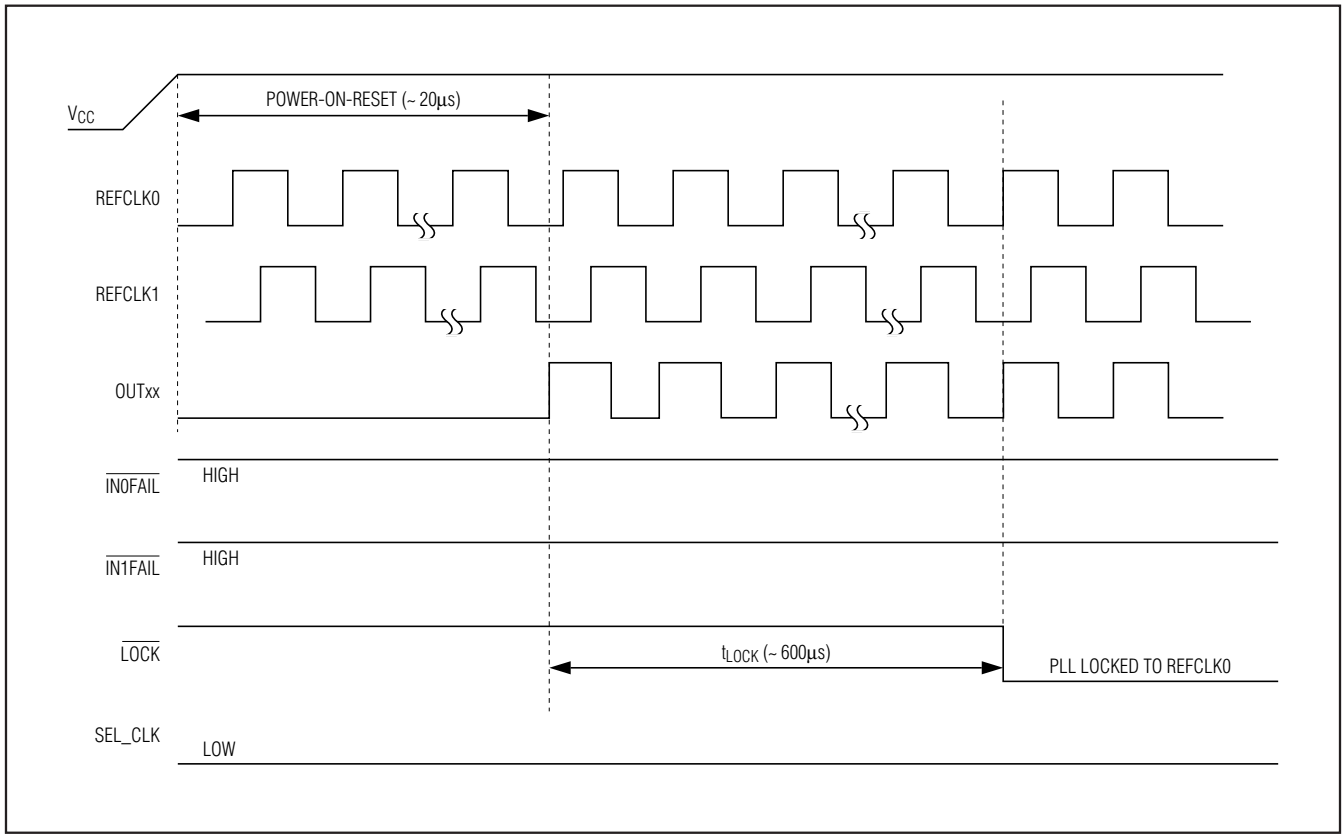


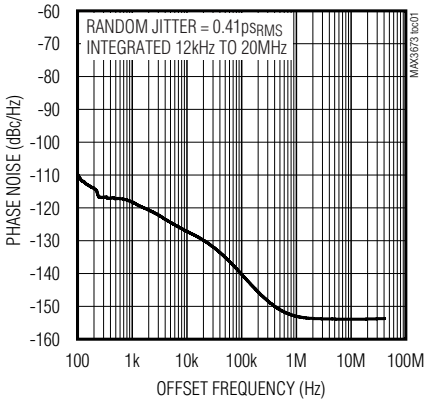
Figure 2. Power-Up, PLL Locks to REFCLK0

Low-Jitter Frequency Synthesizer with Selectable Input Reference

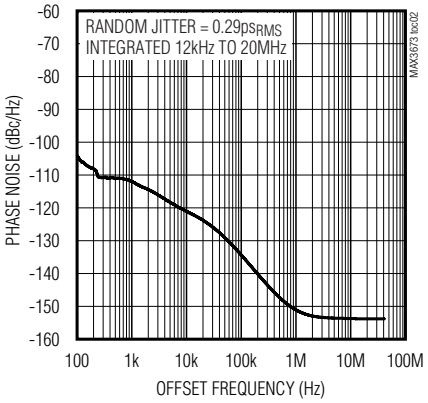
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

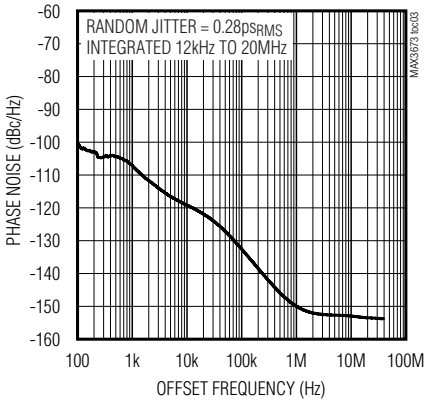
PHASE NOISE AT 61.44MHz



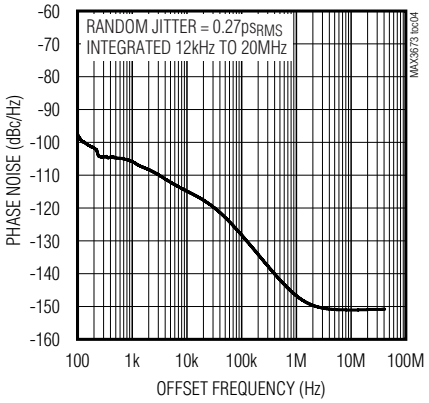
PHASE NOISE AT 122.88MHz



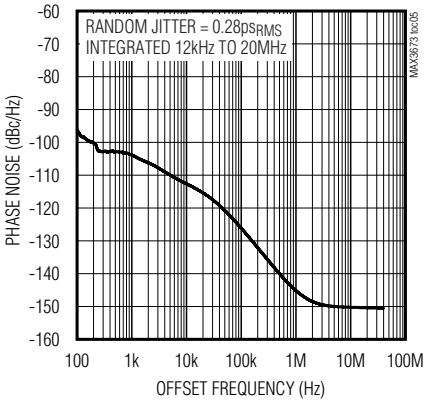
PHASE NOISE AT 153.6MHz



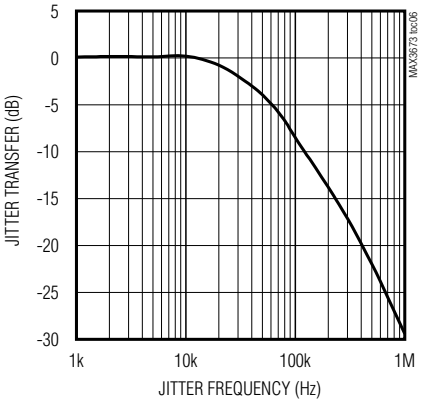
PHASE NOISE AT 245.76MHz



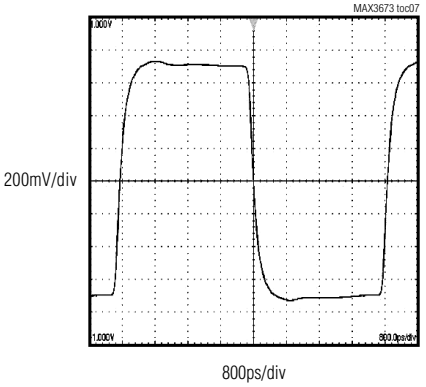
PHASE NOISE AT 307.2MHz



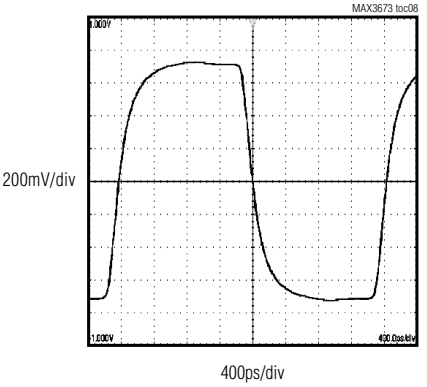
JITTER TRANSFER



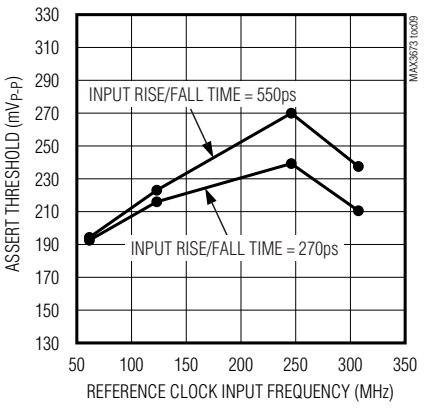
DIFFERENTIAL OUTPUT WAVEFORM AT 153.6MHz



DIFFERENTIAL OUTPUT WAVEFORM AT 307.2MHz



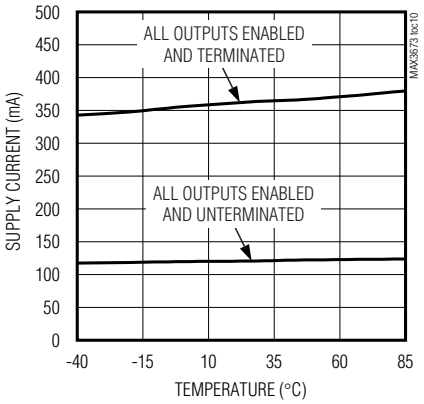
REFERENCE CLOCK AMPLITUDE DETECTION ASSERT THRESHOLD vs. INPUT FREQUENCY



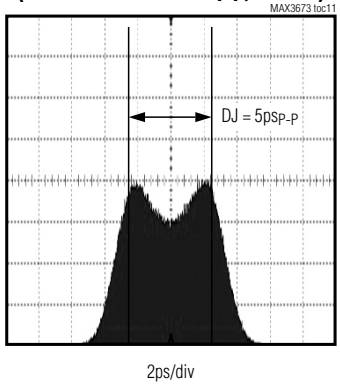
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

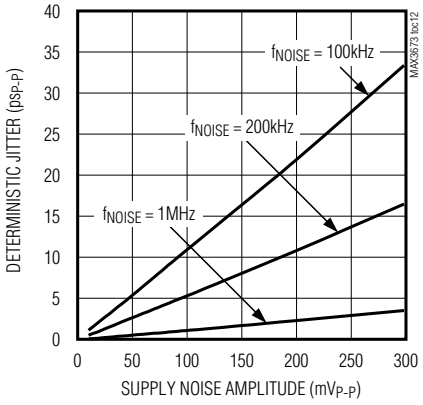
SUPPLY CURRENT vs. TEMPERATURE



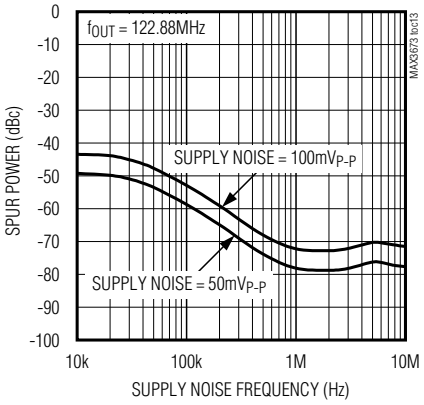
JITTER HISTOGRAM WITH SUPPLY NOISE (SUPPLY NOISE = 50mVP-P, 100kHz)



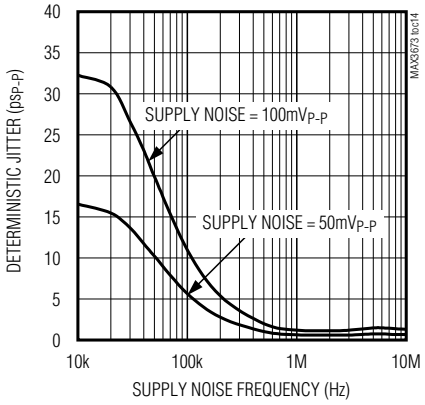
DETERMINISTIC JITTER vs. POWER-SUPPLY NOISE AMPLITUDE



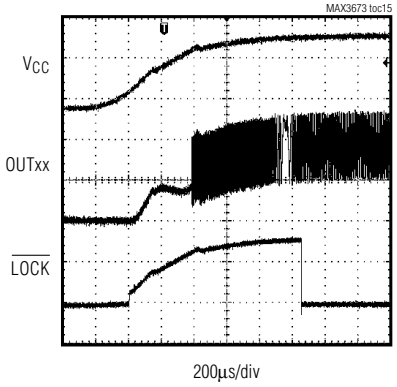
SPURS CAUSED BY POWER-SUPPLY NOISE vs. SUPPLY NOISE FREQUENCY



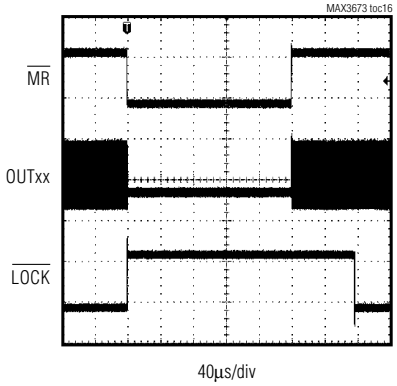
DETERMINISTIC JITTER vs. POWER-SUPPLY NOISE FREQUENCY



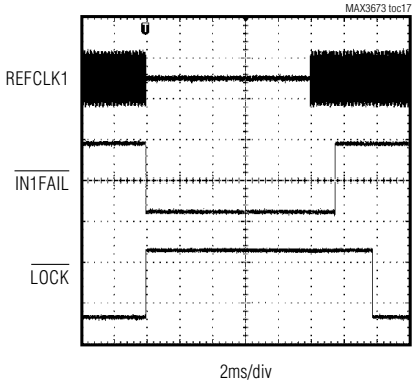
POWER-ON-RESET



MASTER RESET



REFERENCE CLOCK FAILURE DETECTION



Low-Jitter Frequency Synthesizer with Selectable Input Reference

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{IN0FAIL}}$	REFCLK0 Failure Indicator, LVCMOS/LVTTL Output. Low indicates REFCLK0 fails the clock qualification. Once a failed clock is detected, the indicator status is latched and updated every 128 PFD cycles (~ 2µs).
2	RSVD1	Reserved. Leave pin open.
3	RSVD2	Reserved. Connect to GND.
4	REFCLK0	Reference Clock Input 0, Differential LVPECL
5	$\overline{\text{REFCLK0}}$	
6	DM	Four-Level Control Input for Reference Clock Input Divider. See Table 1.
7, 22, 30, 41, 49, 52	V_{CC}	Power Supply. Connect to +3.3V.
8, 14, 23, 29, 42, 48, 53	GND	Supply Ground
9	$\overline{\text{MR}}$	Master Reset, LVCMOS/LVTTL Input. Connect this pin high or leave open for normal operation. Has internal 90kΩ pullup to V_{CC}. Connect low to reset the device. A reset is not required at power-up. If the output divider settings are changed on the fly, a reset is required to phase align the outputs. This input has a 100ns minimum pulse width and is asynchronous to the reference clock. While in reset, all clock outputs are held to logic-low. See Table 6.
10	REFCLK1	Reference Clock Input 1, Differential LVPECL
11	$\overline{\text{REFCLK1}}$	
12	SEL_CLK	Reference Clock Select, LVCMOS/LVTTL Input. Connect low or leave open to select REFCLK0 as the reference clock. Has internal 90kΩ pulldown to GND. Connect high to select REFCLK1 as the reference clock.
13	VCC_VCO	Power Supply for VCO. Connect to +3.3V.
15	CPLL	Connection for PLL Filter Capacitor. Connect a 0.1µF capacitor between this pin and GND.
16	CREG	Connection for VCO Regulator Capacitor. Connect a 0.22µF capacitor between this pin and GND.
17	FB_SEL	External Feedback Select, LVCMOS/LVTTL Input. Connect high to select external feedback for zero-delay buffer configuration. Connect low or leave open for internal feedback. Has internal 90kΩ pulldown to GND.
18	FB_IN	External Feedback Clock Input, Differential LVPECL. Used for zero-delay buffer configuration.
19	$\overline{\text{FB\_IN}}$	
20	$\overline{\text{OUTB0}}$	Clock Output B0, Differential LVPECL
21	OUTB0	
24	$\overline{\text{OUTB1}}$	Clock Output B1, Differential LVPECL
25	OUTB1	
26	$\overline{\text{OUTB2}}$	Clock Output B2, Differential LVPECL
27	OUTB2	
28	DB	Four-Level Control Input for B-Group Output Divider. See Table 3.
31	$\overline{\text{OUTB3}}$	Clock Output B3, Differential LVPECL
32	OUTB3	
33	$\overline{\text{OUTB4}}$	Clock Output B4, Differential LVPECL
34	OUTB4	
35	$\overline{\text{OUTB\_EN}}$	Three-Level Control Input for B-Group Output Enable. See Table 5.
36	$\overline{\text{OUTA\_EN}}$	Three-Level Control Input for A-Group Output Enable. See Table 4.

Pin Description (continued)

PIN	NAME	FUNCTION
37	$\overline{OUTA3}$	Clock Output A3, Differential LVPECL
38	OUTA3	
39	$\overline{OUTA2}$	Clock Output A2, Differential LVPECL
40	OUTA2	
43	DA	Four-Level Control Input for A-Group Output Divider. See Table 2.
44	$\overline{OUTA1}$	Clock Output A1, Differential LVPECL
45	OUTA1	
46	$\overline{OUTA0}$	Clock Output A0, Differential LVPECL
47	OUTA0	
50	PLL_BYPASS	PLL Bypass Control, LVCMOS/LVTTL Input. Connect low or open for normal operation. Has internal 90kΩ pulldown to GND. Connect high to bypass the PLL, connecting the selected reference clock directly to the clock outputs. In this mode, the clock qualification function is not valid. To reduce spurious jitter in bypass mode, the internal VCO should be disabled by shorting the CREG pin to GND.
51	RSVD3	Reserved. Connect to V_{CC}.
54	RSVD4	Reserved. Leave pin open.
55	$\overline{LOCK}$	PLL Lock Indicator, LVCMOS/LVTTL Output. Low indicates PLL is locked.
56	$\overline{IN1FAIL}$	REFCLK1 Failure Indicator, LVCMOS/LVTTL Output. Low indicates REFCLK1 fails the clock qualification. Once a failed clock is detected, the indicator status is latched and updated every 128 PFD cycles (~ 2µs).
—	EP	Exposed Pad. Connect to supply ground for proper electrical and thermal performance.

Detailed Description

The MAX3673 integrates two differential LVPECL reference inputs with a 2:1 mux, a PLL with configurable dividers, nine differential LVPECL clock outputs, and a selectable external feedback input for zero-delay buffer applications (see the *Functional Diagram*).

The two reference clock inputs are continuously monitored for clock failure by the internal PLL and associated logic. If the primary clock fails, the user can switch over to the secondary clock using the 2:1 mux.

The PLL accepts reference input frequencies of 61.44, 122.88, 245.76, or 307.2MHz and generates output frequencies of 61.44, 122.88, 153.6, 245.76, or 307.2MHz. The nine clock outputs are organized into two groups (A and B). Each group has a configurable frequency divider and output-enable control.

Phase-Locked Loop (PLL)

The PLL contains a phase-frequency detector (PFD), charge pump (CP) with a lowpass filter, and voltage-controlled oscillator (VCO). The PFD compares the divided reference frequency to the divided VCO output at 61.44MHz, and generates a control signal to keep the VCO phase and frequency locked to the selected reference clock. Using a high-frequency VCO (2.457GHz) and low-loop bandwidth (40kHz), the MAX3673 attenuates reference clock jitter while maintaining lock and generates low-jitter clock outputs at multiple frequencies. Typical jitter generation is $0.3ps_{RMS}$ (integrated 12kHz to 20MHz).

To minimize supply noise-induced jitter, the VCO supply (VCC_VCO) is isolated from the core logic and output buffer supplies. Additionally, the MAX3673 uses an internal low-dropout (LDO) regulator to attenuate noise from the power supply. This allows the device to achieve excellent power-supply noise rejection, significantly reducing the impact on jitter generation.

Clock Failure Conditions

The MAX3673 clock failure detection is performed using the combination of amplitude qualification and PLL frequency and phase-error qualification. The failure status is indicated for REFCLK0 and REFCLK1 at

Low-Jitter Frequency Synthesizer with Selectable Input Reference

$\overline{\text{IN0FAIL}}$ and $\overline{\text{IN1FAIL}}$, respectively. Once an indicator is asserted low, it is latched and updated every 128 PFD cycles (~ 2µs).

It should be noted that when the PLL is locked to a reference clock, the clock failure indicator for the other reference clock is only valid for amplitude qualification and frequency qualification.

Amplitude Qualification

A reference clock input fails amplitude qualification if any of the following conditions occur:

- Either one or both inputs (REFCLKx, $\overline{\text{REFCLKx}}$) are shorted to V_{CC} or GND.
- Both inputs (REFCLKx, $\overline{\text{REFCLKx}}$) are disconnected from the source and have 130Ω to V_{CC} and 82Ω to GND at each input. See Figure 3.
- Input reference clock differential swing is below the clock failure assert threshold as specified in the *Electrical Characteristics*. See Figure 4.

The response time for these conditions is typically between 50ns and 300ns.

Phase Qualification

A reference clock input fails phase qualification when the phase error at the PFD output exceeds the error window (0.75ns typical) for more than five of eight PFD cycles. A reference clock input is qualified when phase error at the PFD output is within the phase-error window for eight consecutive PFD cycles. Note that phase qualification only applies to the reference input currently being used by the PLL.

Frequency Qualification

A reference clock input becomes frequency qualified if the input frequency is within ±2.4% of the nominal frequency. The reference input becomes frequency disqualified if the input frequency moves away from the nominal frequency by more than ±8%.

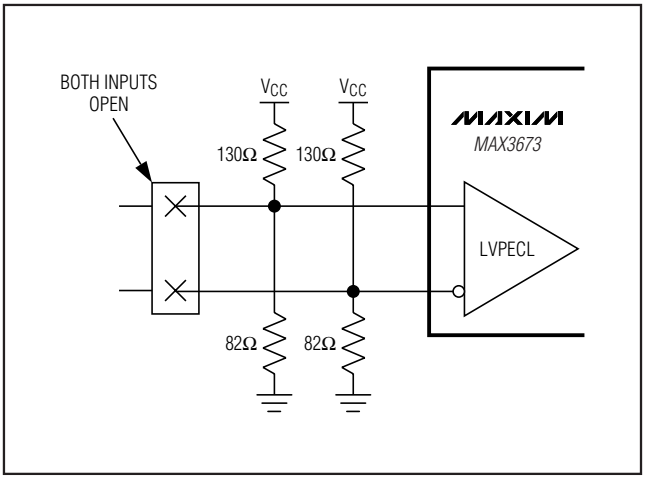


Figure 3. Positions for Open-Circuit Detection

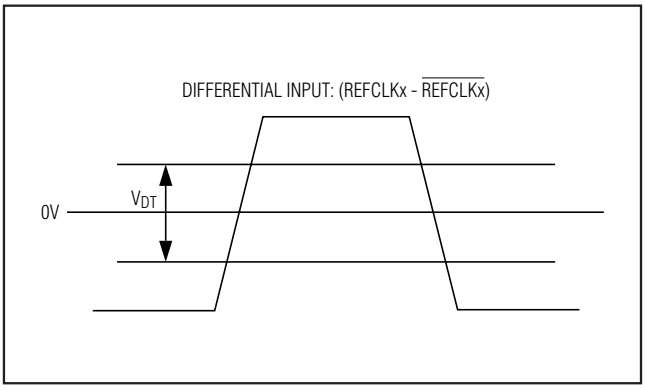


Figure 4. Input Amplitude Detection Threshold

Table 1. Divider M Configuration for Input Frequencies

CONNECTION FROM DM PIN	INPUT FREQUENCY (MHz)
GND	61.44
V_{CC}	122.88
Open	245.76
10kΩ to GND	307.2

Table 2. Divider A Configuration for A-Group Output Frequencies

CONNECTION FROM DA PIN	OUTPUT FREQUENCY AT OUTA[3:0] (MHz)
GND	61.44
V_{CC}	122.88
Open	153.6
10kΩ to GND	307.2

Table 3. Divider B Configuration for B-Group Output Frequencies

CONNECTION FROM DB PIN	OUTPUT FREQUENCY AT OUTB[4:0] (MHz)
GND	61.44
V_{CC}	122.88
Open	245.76
10kΩ to GND	307.2

PLL Out-of-Lock Condition

If the frequency difference between the reference clock input and the VCO at the PFD input becomes within 500ppm, the PLL is considered to be in lock ($\overline{LOCK}$ = 0). When the frequency difference between the reference clock input and the VCO at the PFD input becomes greater than 800ppm, the PLL is considered out-of-lock. It should be noted that the LOCK indicator is not part of the frequency qualification used for the $\overline{INxFAIL}$ indicators.

Input and Output Frequencies

The MAX3673 input and output dividers are configured using four-level control inputs DM, DA, and DB. Each divider is independent and can have a unique setting. The input connection and associated frequencies are listed in Tables 1, 2, and 3.

Output-Enable Controls

Each output group (A and B) has a three-level control input $\overline{OUTA\_EN}$ and $\overline{OUTB\_EN}$. See Tables 4 and 5 for configuration settings. When clock outputs are disabled, they are high impedance. Unused enabled outputs should be left open.

Power-On-Reset (POR)

At power-on, an internal signal is generated to hold the MAX3673 in a reset state. This internal reset time is about 20µs after V_{CC} reaches 3.0V (Figure 2). During the POR time, the outputs are held to logic-low (OUTxx = low and $\overline{OUTxx}$ = high). See Table 6 for output signal status during POR. After this internal reset time, the PLL starts to lock to the reference clock selected by SEL_CLK.

Table 4. OUTA[3:0] Enable Control

CONNECTION FROM $\overline{OUTA\_EN}$ PIN	A-GROUP OUTPUT ENABLED	A-GROUP OUTPUT DISABLED TO HIGH IMPEDANCE
GND	OUTA0, OUTA1, OUTA2, OUTA3	—
V_{CC}*	—	OUTA0, OUTA1, OUTA2, OUTA3
Open	OUTA0, OUTA1	OUTA2, OUTA3

**Connecting both $\overline{OUTA\_EN}$ and $\overline{OUTB\_EN}$ to V_{CC} enables a factory test mode and forces all indicators to GND. This is not a valid mode of operation.*

Table 5. OUTB[4:0] Enable Control

CONNECTION FROM $\overline{OUTB\_EN}$ PIN	B-GROUP OUTPUT ENABLED	B-GROUP OUTPUT DISABLED TO HIGH IMPEDANCE
GND	OUTB0, OUTB1, OUTB2, OUTB3, OUTB4	—
V_{CC}*	OUTB0	OUTB1, OUTB2, OUTB3, OUTB4
Open	OUTB0, OUTB1, OUTB2	OUTB3, OUTB4

**Connecting both $\overline{OUTA\_EN}$ and $\overline{OUTB\_EN}$ to V_{CC} enables a factory test mode and forces all indicators to GND. This is not a valid mode of operation.*

Low-Jitter Frequency Synthesizer with Selectable Input Reference

Master Reset

After power-up, an external master reset ($\overline{MR}$) can be provided to reset the internal dividers. This input requires a minimum reset pulse width of 100ns (active low) and is asynchronous to the reference clock. While $\overline{MR}$ is low, all clock outputs are held to logic-low (OUTxx = low, $\overline{OUTxx}$ = high). See Table 6 for the output signal status during master reset. When the master reset input is deasserted ($\overline{MR}$ = 1), the PLL starts to lock to the reference clock selected by SEL_CLK.

Master reset is only needed for applications where divider configurations are changed on the fly and the clock outputs need to maintain phase alignment. A master reset is not required at power-up.

External Feedback for Zero-Delay Buffer

The MAX3673 can be operated with either internal or external PLL feedback path, controlled by the FB_SEL input. Connecting FB_SEL to GND selects internal feedback. For applications where a known phase relationship between the reference clock input and the external feedback input (FB_IN, $\overline{FB\_IN}$) are needed for phase synchronization, connect FB_SEL to V_{CC} for zero-delay buffer configuration and provide external feedback to the FB_IN input.

PLL Bypass Mode

PLL bypass mode is provided for test purposes. In PLL bypass mode (PLL_BYPASS = 1), the selected reference clock is connected to the LVPECL clock outputs directly. The output clock frequency is the same as the input clock frequency and the clock qualification function is not valid. To reduce spurious jitter in bypass mode, the internal VCO should be disabled by shorting the CREG pin to GND.

Applications Information

Interfacing with LVPECL Inputs

Figure 5 shows the equivalent LVPECL input circuit for REFCLK0, REFCLK1, and FB_IN. These inputs are internally biased to allow AC- or DC-coupling and have > 40kΩ differential input impedance. When AC-coupled, these inputs can accept LVDS, CML, and LVPECL signals. Unused reference clock inputs should be left open.

Interfacing with LVPECL Outputs

Figure 6 shows the equivalent LVPECL output circuit. These outputs are designed to drive a pair of 50Ω transmission lines terminated with 50Ω to V_{TT} = V_{CC} - 2V. If a separate termination voltage (V_{TT}) is not available, other termination methods can be used such as those shown in Figures 7 and 8. Unused outputs, enabled or disabled, can be left open or properly terminated. For more information on LVPECL terminations and how to interface with other logic families, refer to Application Note 291: *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

Layout Considerations

The clock inputs and outputs are critical paths for the MAX3673, and care should be taken to minimize discontinuities on the transmission lines. Maintain 100Ω differential (or 50Ω single-ended) impedance in and out of the MAX3673. Avoid using vias and sharp corners. Termination networks should be placed as close as possible to receiving clock inputs. Provide space between differential output pairs to reduce crosstalk, especially if the A and B group outputs are operating at different frequencies.

Table 6. Output Signal Status During Power-On-Reset or Master Reset

OUTPUT	DURING POWER-ON-RESET (FOR ~ 20µs AFTER V_{CC} > 3.0V)	DURING MASTER RESET ($\overline{MR}$ = 0)	NOTES
$\overline{IN0FAIL}$	1		Forced high regardless of reference input qualification.
$\overline{IN1FAIL}$	1		Forced high regardless of reference input qualification.
$\overline{LOCK}$	1		PLL out-of-lock.
OUTA[3:0]	Logic-Low		—
OUTB[4:0]	Logic-Low		—

Power Supply and Ground Connections

The MAX3673 has seven supply connection pins; installation of a bypass capacitor at each supply pin is recommended. All seven supply connections should be driven from the same source to eliminate the possibility of independent power-supply sequencing. Excessive supply noise can result in increased jitter.

The 56-pin TQFN package features an exposed pad (EP), which provides a low-resistance thermal path for heat removal from the IC and must be connected to the circuit board ground plane for proper operation.

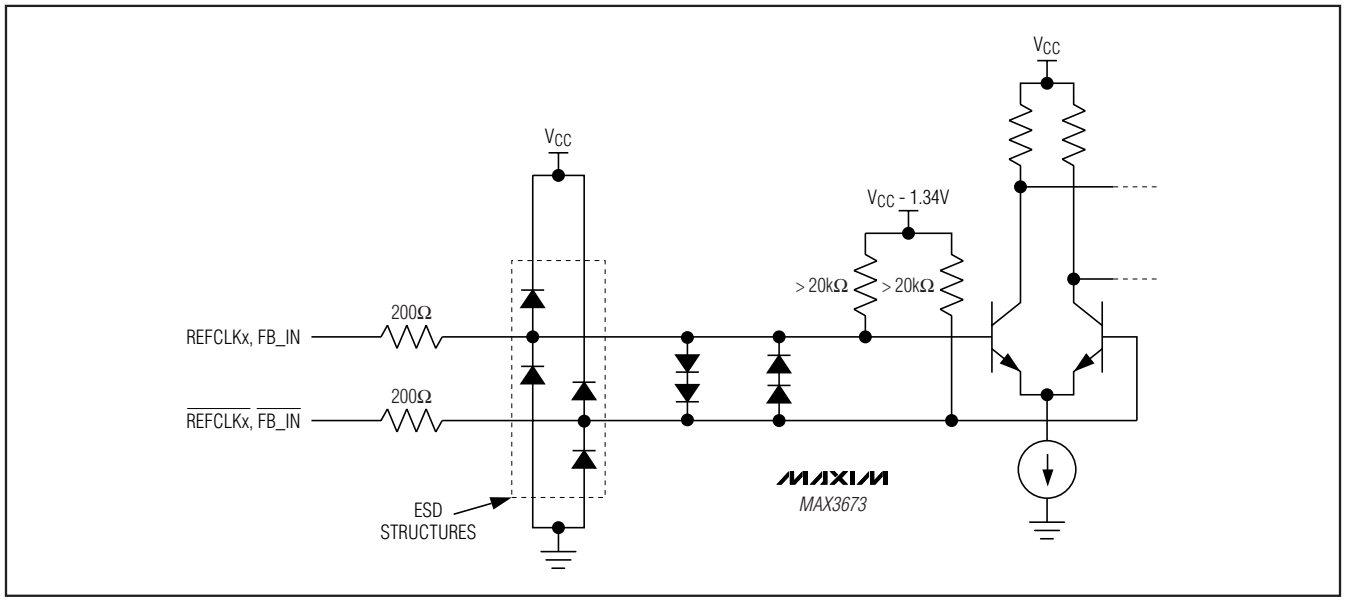


Figure 5. Equivalent LVPECL Input Circuit

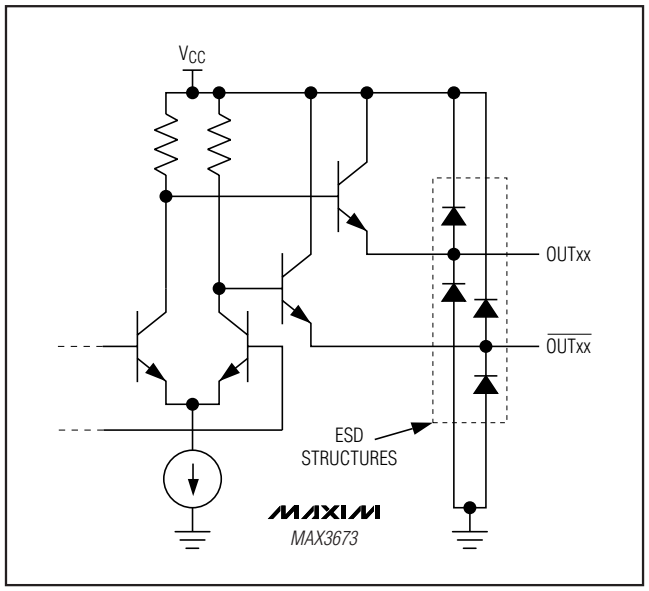


Figure 6. Equivalent LVPECL Output Circuit

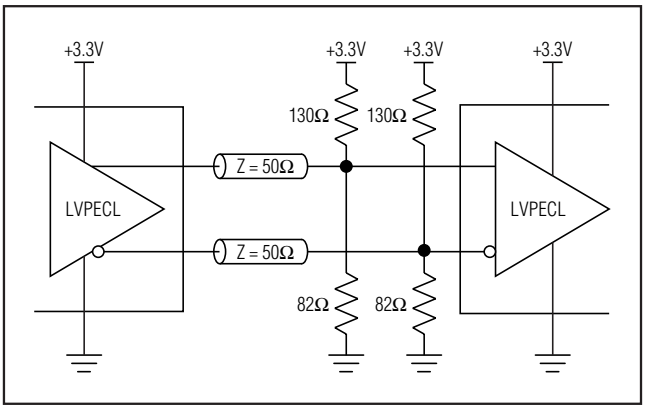


Figure 7. Thevenin Equivalent LVPECL Termination

Low-Jitter Frequency Synthesizer with Selectable Input Reference

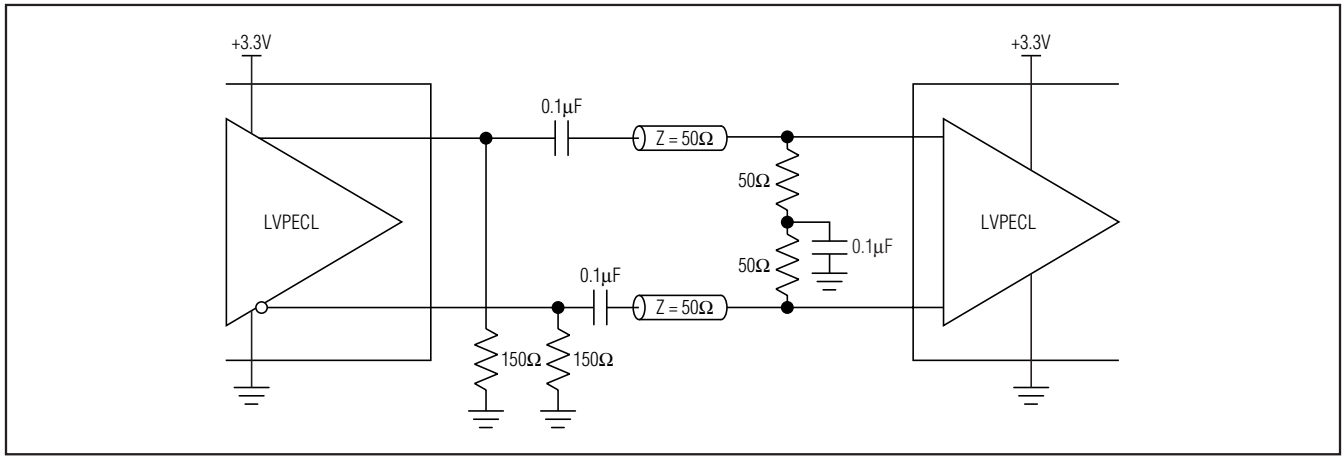
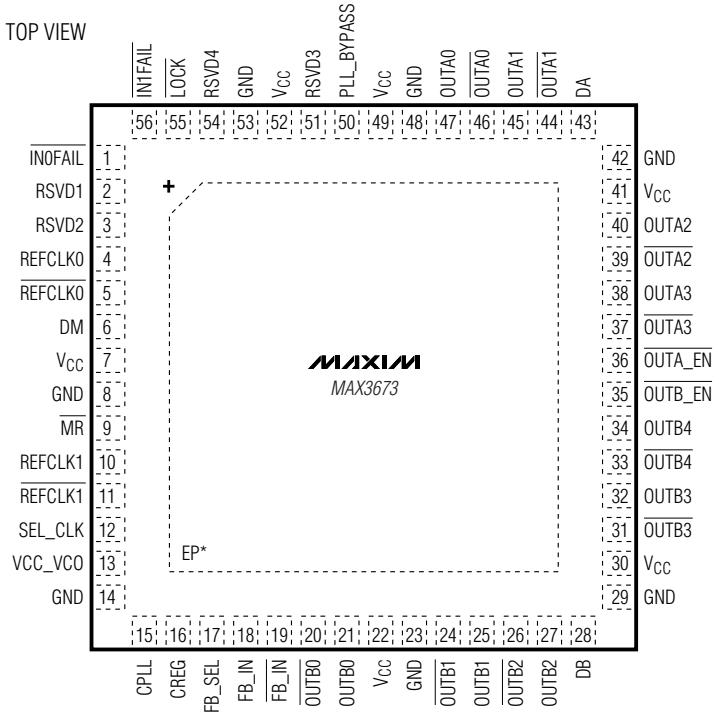


Figure 8. AC-Coupled LVPECL Termination

Pin Configuration

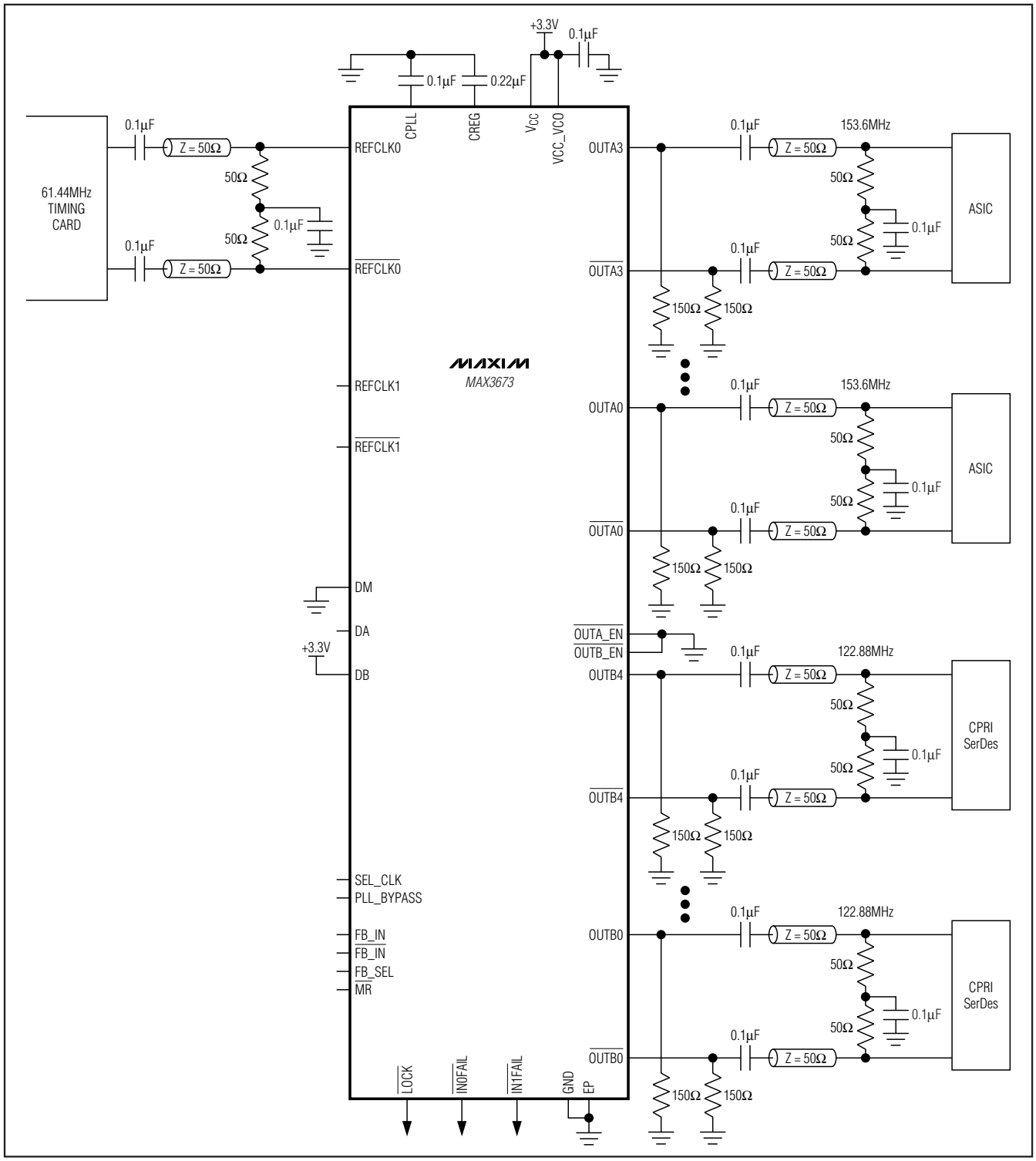


THIN QFN
(8mm × 8mm × 0.8mm)

*THE EXPOSED PAD OF THE TQFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

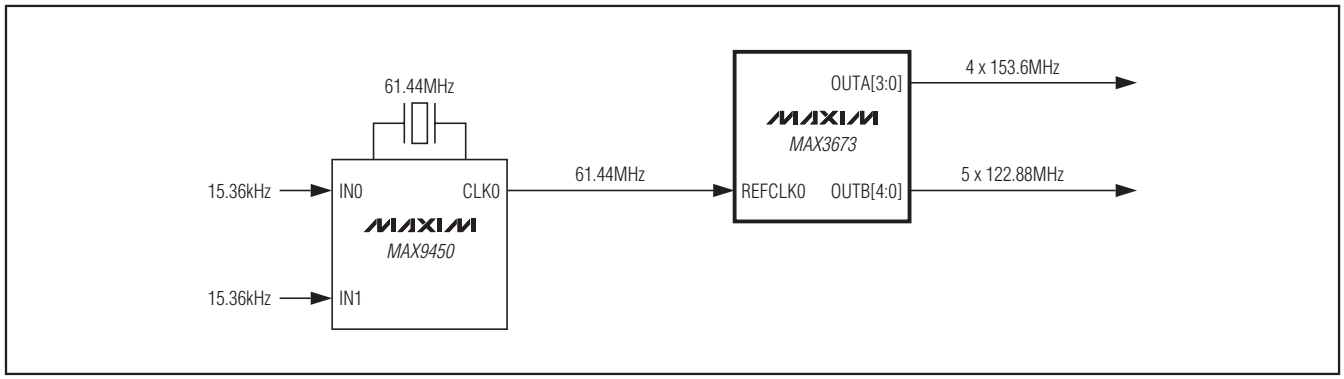
Low-Jitter Frequency Synthesizer with Selectable Input Reference

Typical Application Circuits



Low-Jitter Frequency Synthesizer with Selectable Input Reference

Typical Application Circuits (continued)



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5688+3	**21-0135**