19-4421; Rev 0; 4/09

EVALUATION KIT AVAILABLE

Adaptive Step-Up Converters with 1.5A Flash Driver

General Description

The MAX8834Y/MAX8834Z flash drivers integrate a 1.5A PWM DC-DC step-up converter and three programmable low-side, low-dropout LED current regulators. The step-up converter features an internal switching MOSFET and synchronous rectifier to improve efficiency and minimize external component count. An I²C interface provides flexible control of step-up converter output voltage setting, movie/flash mode selection, flash timer duration settings, and current regulator settings. The MAX8834Y/MAX8834Z operate down to 2.5V, making them future proof for new battery technologies.

The MAX8834Y/MAX8834Z consist of two current regulators for the flash/movie mode. Each current regulator can sink 750mA in flash mode and 125mA in movie mode. The MAX8834Y/MAX8834Z also integrate a 16mA low-current regulator that can be used to indicate camera status. The indicator current regulator includes programmable ramp and blink timer settings. A programmable input current limit, invoked using the GSMB control, reduces the total current drawn from the battery during PA transmit events. This ensures the flash current is set to the maximum possible for any given operating condition. Additionally, the MAX8834Y/MAX8834Z include a MAXFLASH* function that adaptively reduces flash current during low battery conditions to help prevent system undervoltage lockup.

Other features include an optional NTC input for finger-burn protection and open/short LED detection. The MAX8834Y switches at 2MHz, providing best overall efficiency. The MAX8834Z switches at 4MHz, providing smallest overall solution size. The MAX8834Y/MAX8834Z are available in a 20-bump, 0.5mm pitch WLP package (2.5mm x 2.0mm).

*Patent pending.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SWITCHING FREQUENCY (MHz)
MAX8834YEWP+T	-40°C to +85°C	20 WLP (2.5mm x 2.0mm)	2
MAX8834ZEWP+T	-40°C to +85°C	20 WLP (2.5mm x 2.0mm)	4

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Pin Configuration appears at end of data sheet.

Features

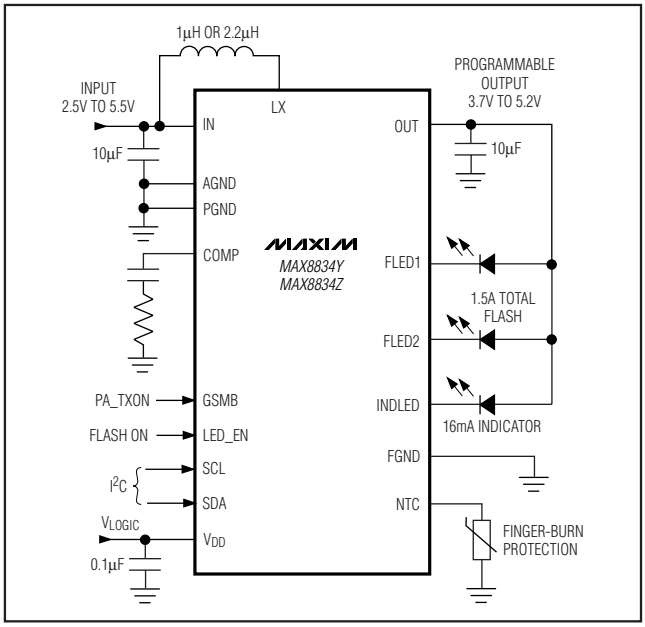
- **2.5V to 5.5V Operation Range**
- **Step-Up DC-DC Converter**
  - **1.5A Guaranteed Output Current**
  - **Adaptive or I²C Programmable Output Voltage**
  - **2MHz and 4MHz Switching Frequency Options**
- **Two Flash/Movie LED Current Regulators**
  - **I²C Programmable Flash and Movie Current**
  - **Low-Dropout Voltage (110mV max) at 500mA**
- **LED Indicator Current Regulator**
  - **I²C Programmable Output Current**
  - **Ramp and Blink Timers for Indicator Mode**
  - **Low-Dropout Voltage (130mV max) at 16mA**
- **I²C Programmable Safety and Watchdog Timers**
- **GSM Blank Logic Input**
- **MAXFLASH System Lockup Protection**
- **Remote Temperature Sensor Input**
- **Open/Short LED Detection**
- **Thermal Shutdown Protection**
- **< 1µA Shutdown Current**
- **20-Bump, 0.5mm Pitch, 2.5mm x 2.0mm WLP**

Applications

Cell Phones and Smart Phones

PDAs, Digital Cameras, and Camcorders

Typical Operating Circuit



Adaptive Step-Up Converters with 1.5A Flash Driver

ABSOLUTE MAXIMUM RATINGS

IN, OUT, NTC to AGND .....-0.3V to +6.0V
V_{DD} to AGND.....-0.3V to +4.0V
SCL, SDA, LED_EN, GSMB to AGND .....-0.3V to (V_{DD} + 0.3V)
FLED1, FLED2, INDLED to FGND .....-0.3V to (V_{OUT} + 0.3V)
COMP to AGND.....-0.3V to (V_{IN} + 0.3V)
PGND, FGND to AGND .....-0.3V to +0.3V
I_{LX} Current (rms) 3A

Continuous Power Dissipation (T_A = +70°C)
(derate 17.5mW/°C above +70°C).....1410mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature* (soldering) .....+260°C

**This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, V_{AGND} = V_{PGND} = V_{FGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Operating Voltage			2.5		5.5	V
V_{DD} Operating Range			1.62		3.6	V
V_{DD} Undervoltage Lockout (UVLO) Threshold	V_{DD} falling		1.25	1.4	1.55	V
V_{DD} UVLO Hysteresis				50		mV
IN UVLO Threshold	V_{IN} falling		2.15	2.3	2.45	V
IN UVLO Hysteresis				50		mV
IN Standby Supply Current	V_{SCL} = V_{SDA} = V_{DD}, V_{IN} = 5.5V, I^2C ready				1	µA
V_{DD} Standby Supply Current (All Outputs Off, I^2C Enabled)	V_{SCL} = V_{SDA} = V_{DD} = 3.6V, I^2C ready			4	7	µA
LOGIC INTERFACE						
Logic Input-High Voltage	V_{DD} = 1.62V to 3.6V	LED_EN, GSMB	1.4			V
		SCL, SDA	0.7 x V_{DD}			
Logic Input-Low Voltage	V_{DD} = 1.62V to 3.6V	LED_EN, GSMB			0.4	V
		SCL, SDA			0.3 x V_{DD}	
LED_EN Minimum High Time (LED_EN is Internally Sampled by a 1MHz Clock)				1		µs
LED_EN Propagation Delay	From LED_EN going high to rising edge on current regulator			3		µs
LED_EN and GSMB Pulldown Resistor			400	800	1600	kΩ
Logic Input Current (SCL, SDA)	V_{IL} = 0V or V_{IH} = 3.6V	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{AGND} = V_{PGND} = V_{FGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Leakage Current	IN and V_{DD} in UVLO, V_{LED_EN} = V_{GSMB} = 0V	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		
I²C INTERFACE						
SDA Output Low Voltage	I_{SDA} = 3mA			0.03	0.4	V
I²C Clock Frequency					400	kHz
Bus-Free Time Between STOP and START	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}		0.6	0.1		µs
SCL Low Period	t_{LOW}		1.3	0.2		µs
SCL High Period	t_{HIGH}		0.6	0.2		µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6	0.1		µs
SDA Hold Time	t_{HD_DAT}		0	-0.01		µs
SDA Setup Time	t_{SU_DAT}		100	50		ns
Setup Time for STOP Condition	t_{SU_STO}		0.6	0.1		µs
STEP-UP DC-DC CONVERTER						
OUT Voltage Range	100mV steps		3.7		5.2	V
OUT Voltage Accuracy	No load, V_{OUT} = 5V		-2.75	±0.5	+2.75	%
OUT Overvoltage Protection	When running in adaptive mode		5.2	5.35	5.5	V
Adaptive Output Voltage Regulation Threshold	I_{FLED1} = I_{FLED2} = 492.24mA setting, I_{INDLED} = 16mA			150		mV
PGOOD Window Comparator	V_{OUT} = 5V, in programmable mode		-15	-12.5	-10	%
Line Regulation	V_{IN} = 2.5V to 4.2V			0.1		%/V
Load Regulation	I_{OUT} = 0mA to 1500mA			0.5		%/A
nFET Current Limit				3.6		A
LX nFET On-Resistance	LX to PGND, I_{LX} = 200mA			0.055	0.130	Ω
LX pFET On-Resistance	LX to OUT, I_{LX} = 200mA			0.12	0.200	Ω
LX Leakage	V_{LX} = 5.5V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.1		
Input Current Limit Range During GSMB Trigger			50		800	mA
Input Current Limit Step Size During GSMB Trigger				50		mA
Input Current Limit Accuracy	I_{ILIM} = 100mA, in dropout mode		-15		+15	%
Operating Frequency, No Load	MAX8834Y	T_A = +25°C	1.8	2	2.2	MHz
		T_A = -40°C to +85°C	1.6		2.4	
	MAX8834Z	T_A = +25°C	3.6	4	4.4	
		T_A = -40°C to +85°C	3.2		4.8	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{AGND} = V_{PGND} = V_{FGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle	V_{OUT} = 4.5V		69	75		%
Minimum Duty Cycle	V_{OUT} = 4.5V			7.5		%
COMP Transconductance	V_{COMP} = 1.5V			55		µS
COMP Discharge Resistance	During shutdown or UVLO, from COMP to AGND			120		Ω
OUT Discharge Resistance	During shutdown or UVLO, from OUT to LX			10		kΩ
FLED1/FLED2 CURRENT REGULATOR						
IN Supply Current	Step-up off, FLED1/FLED2 on, supply current for each current source			0.6		mA
Maximum Current Setting	Flash			750		mA
	Movie			125		
Current Accuracy	23.44mA setting	T_A = +25°C	-5		+20	%
	492.24mA setting	T_A = +25°C	-2.5	±0.5	+2.5	%
		T_A = -40°C to +85°C	-4		+4	
	750mA setting	T_A = -40°C to +85°C	-10		+5	%
Current Regulator Dropout (Note 2)	492.24mA setting				110	mV
	93.75mA setting			50	100	
FLED1/FLED2 Leakage in Shutdown	V_{FLED1} = V_{FLED2} = 5.5V	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		
INDLED CURRENT REGULATOR						
IN Supply Current	Step-up converter off, INDLED on			0.6		mA
Maximum Current Setting				16		mA
Current Accuracy	0.5mA setting	T_A = +25°C	-10		+10	%
	16mA setting	T_A = +25°C	-3	±0.5	+3	%
		T_A = -40°C to +85°C	-5		+5	%
Current Regulator Dropout	16mA setting (Note 2)			55	130	mV
INDLED Leakage in Shutdown	V_{INDLED} = 5.5V	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		
PROTECTION CIRCUITS						
NTC BIAS Current			19.4	20	20.6	µA
NTC Overtemperature Detection Threshold	V_{NTC} falling, 100mV hysteresis, NTC_CNTL[2:0] = 100		388	400	412	mV
NTC Short Detection Threshold	V_{NTC} falling			100		mV
Flash Duration Timer Range	In 50ms steps (Note 3)		50		800	ms
Flash Duration Timer Accuracy (400ms Setting)	T_A = +25°C		360	400	440	ms
	T_A = -40°C to +85°C		320		480	
Minimum Flash Duration	FLASH_EN[2:0] = 1XX			2		ms
Flash Safety Timer Reset Inhibit Period	From falling edge of LED_EN until flash safety timer is reset			30		ms
Watchdog Timer Range	In 4s steps		4		16	s

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, V_{AGND} = V_{PGND} = V_{FGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Watchdog Timer Accuracy (4s setting)	T_A = +25°C	3.6	4	4.4	s
	T_A = -40°C to +85°C	3.2		4.8	
Open LED Detection Threshold	FLED1, FLED2, INDLED enabled			100	mV
Shorted LED Detection Threshold	FLED1, FLED2, INDLED enabled		V_{OUT} - 1V		V
Open and Short Debounce Timer	From LED open or short detected until LED current regulator is disabled		30		ms
Thermal-Shutdown Hysteresis			20		°C
Thermal Shutdown			+160		°C
MAXFLASH					
Low-Battery Detect Threshold Range	33mV steps	2.5		3.4	V
Low-Battery Voltage Threshold Accuracy			±2.5		%
Low-Battery Voltage Hysteresis Programmable Range		100		200	mV
Low-Battery Voltage Hysteresis Step Size			100		mV
Low-Battery Reset Time	LB_TMR[1:0] = 00	200	250	300	µs
	LB_TMR[1:0] = 01	400	500	600	

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: LED current regulator dropout voltage is defined as the voltage when current drops 10% from the current level measured at 0.6V.

Note 3: Flash duration is from rising edge of LED_EN until I_{FLED} = 0A (safety time in one-shot mode).

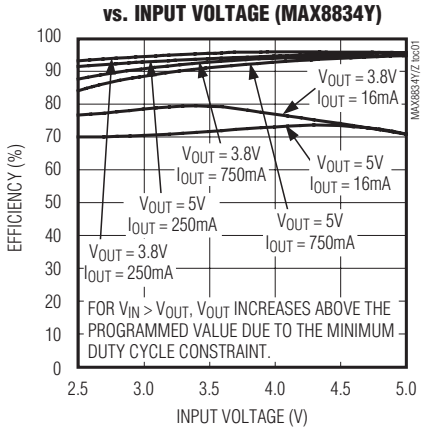
Note 4: The adaptive output voltage regulation threshold is individually set on each device to 75mV above the dropout voltage of the LED current regulators. This ensures minimum power dissipation on the IC during a flash event. The dropout voltage chosen is the highest measured dropout voltage of FLED1, FLED2, and INDLED.

Adaptive Step-Up Converters with 1.5A Flash Driver

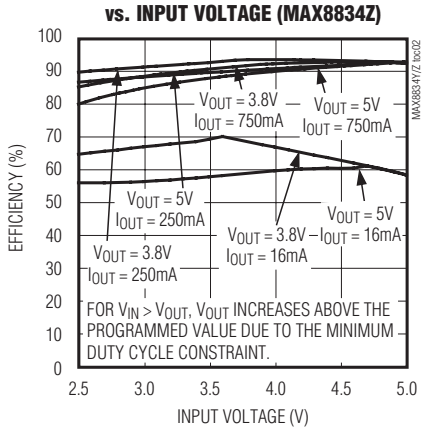
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

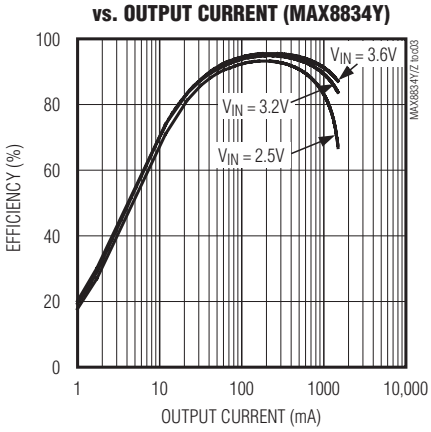
STEP-UP CONVERTER EFFICIENCY vs. INPUT VOLTAGE (MAX8834Y)



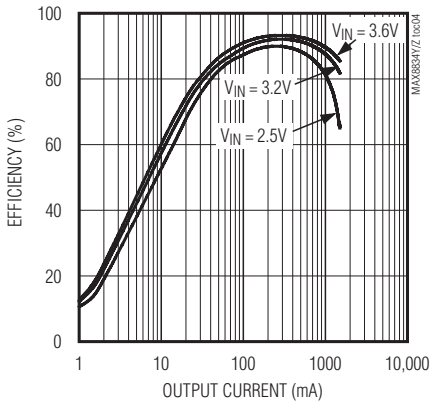
STEP-UP CONVERTER EFFICIENCY vs. INPUT VOLTAGE (MAX8834Z)



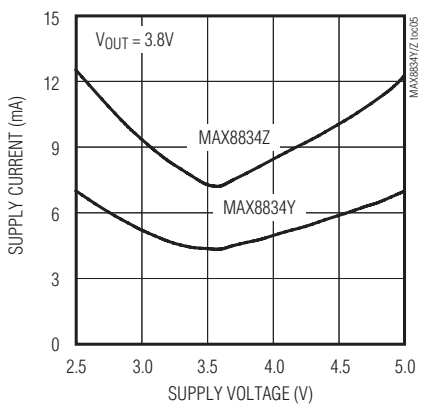
STEP-UP CONVERTER EFFICIENCY vs. OUTPUT CURRENT (MAX8834Y)



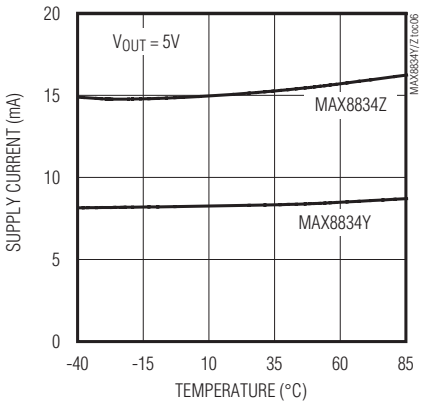
STEP-UP CONVERTER EFFICIENCY vs. OUTPUT CURRENT (MAX8834Z)



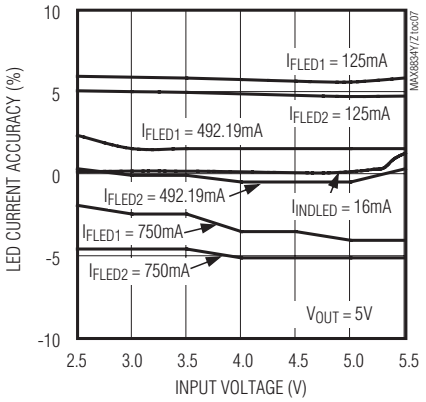
STEP-UP CONVERTER SUPPLY CURRENT vs. SUPPLY VOLTAGE



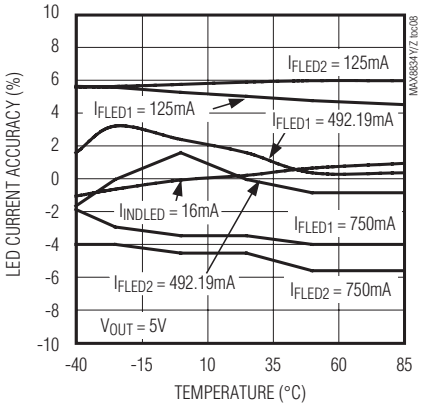
STEP-UP CONVERTER SUPPLY CURRENT vs. TEMPERATURE



LED CURRENT ACCURACY vs. INPUT VOLTAGE



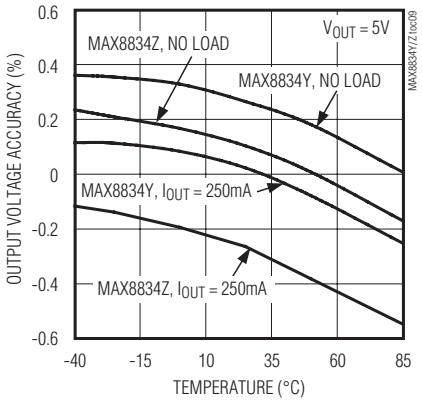
LED CURRENT ACCURACY vs. TEMPERATURE



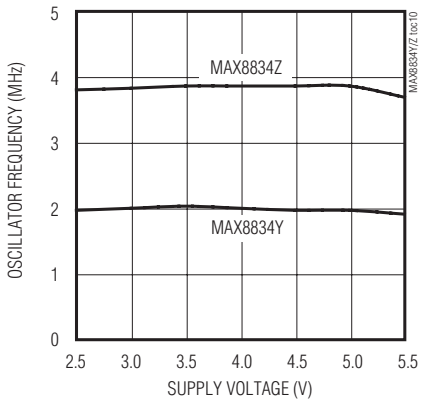
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

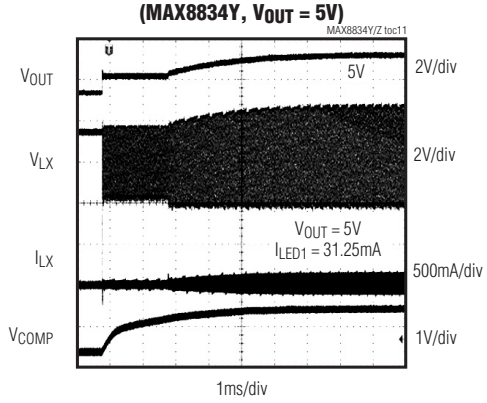
OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE



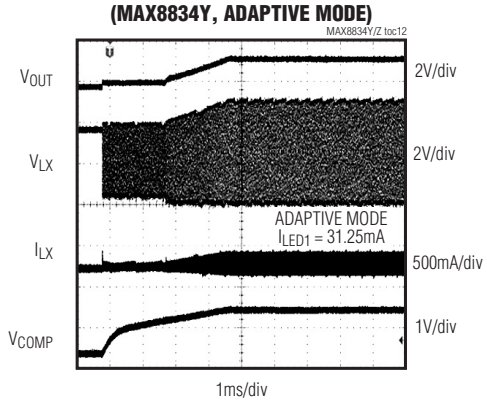
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



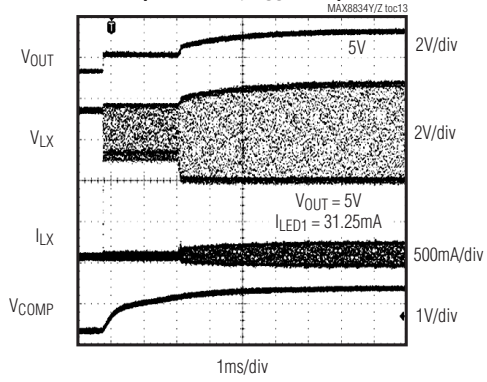
STARTUP WAVEFORM (MAX8834Y, V_{OUT} = 5V)



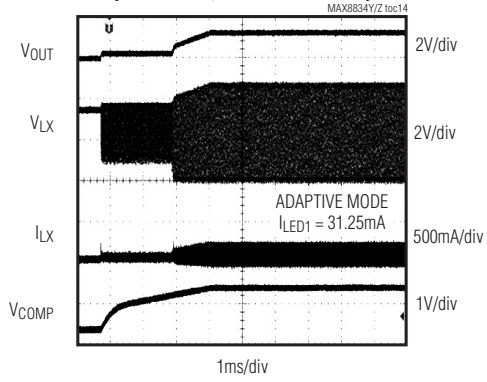
STARTUP WAVEFORM (MAX8834Y, ADAPTIVE MODE)



STARTUP WAVEFORM (MAX8834Z, V_{OUT} = 5V)



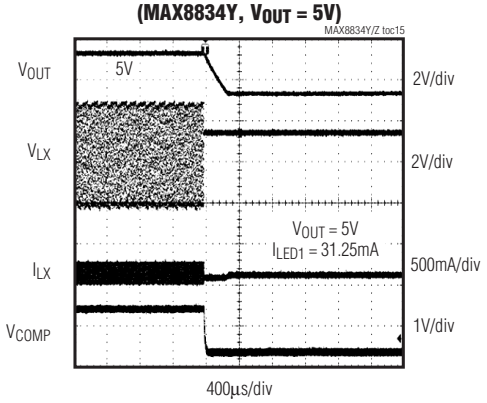
STARTUP WAVEFORM (MAX8834Z, ADAPTIVE MODE)



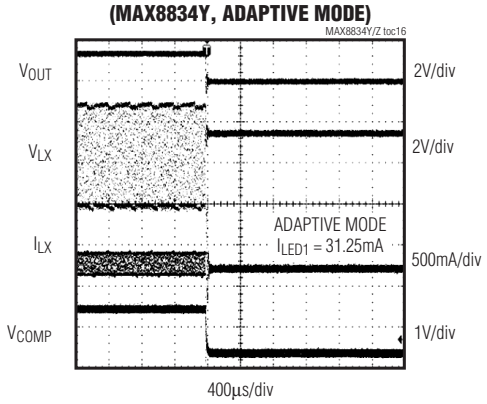
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

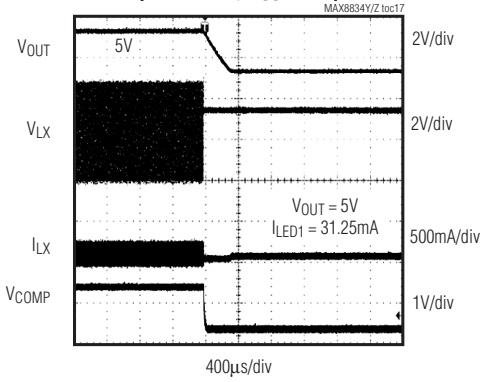
SHUTDOWN WAVEFORM (MAX8834Y, V_{OUT} = 5V)



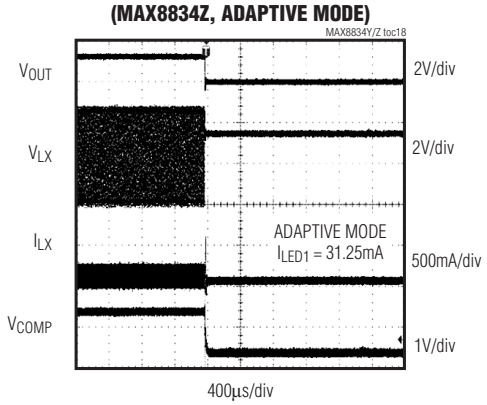
SHUTDOWN WAVEFORM (MAX8834Y, ADAPTIVE MODE)



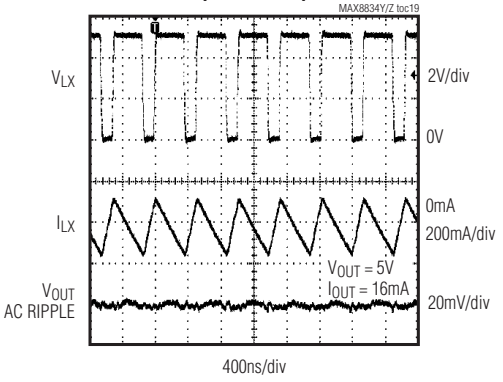
SHUTDOWN WAVEFORM (MAX8834Z, V_{OUT} = 5V)



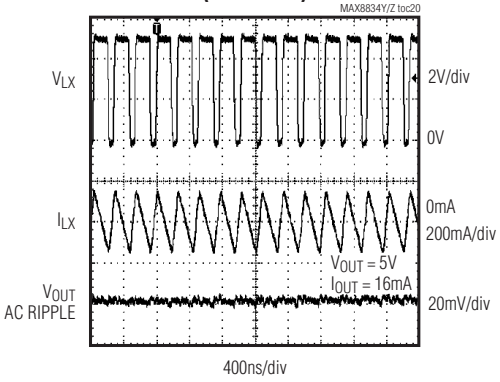
SHUTDOWN WAVEFORM (MAX8834Z, ADAPTIVE MODE)



LIGHT-LOAD SWITCHING WAVEFORMS (MAX8834Y)



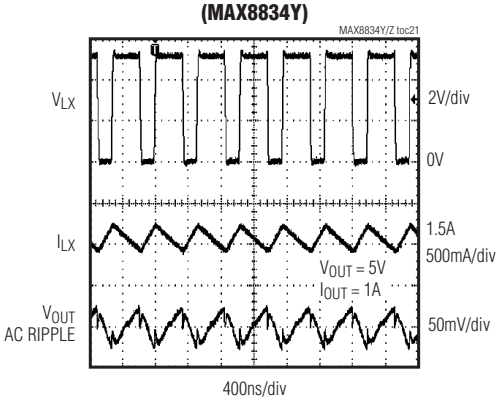
LIGHT-LOAD SWITCHING WAVEFORMS (MAX8834Z)



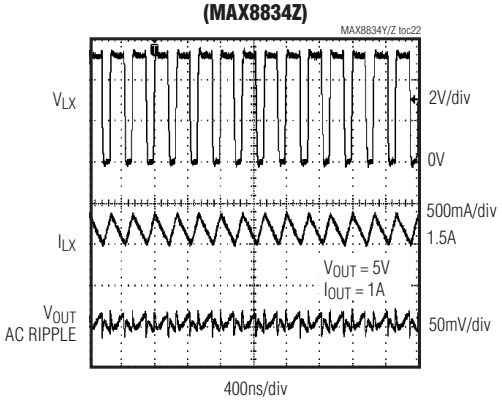
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

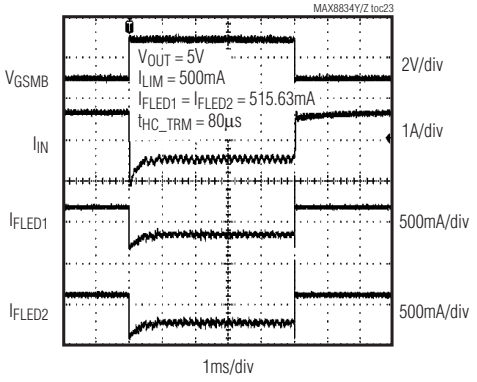
HEAVY-LOAD SWITCHING WAVEFORMS (MAX8834Y)



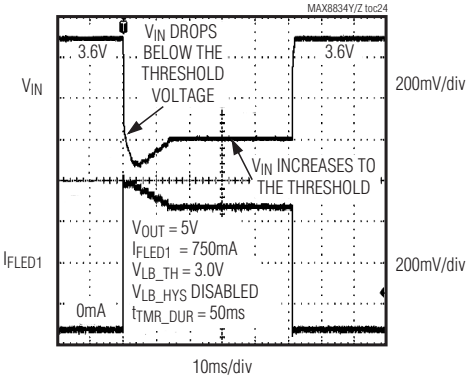
HEAVY-LOAD SWITCHING WAVEFORMS (MAX8834Z)



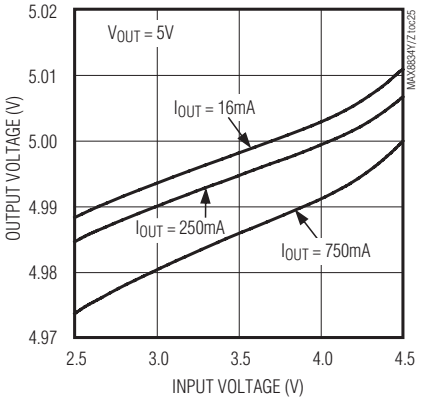
GSMB WAVEFORM



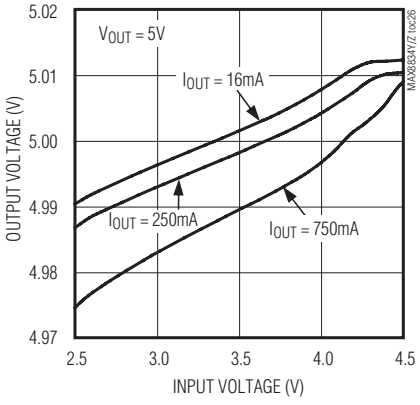
MAXFLASH FUNCTION



OUTPUT VOLTAGE LINE REGULATION (MAX8834Y)



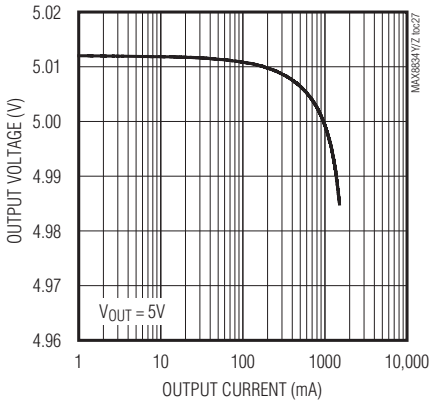
OUTPUT VOLTAGE LINE REGULATION (MAX8834Z)



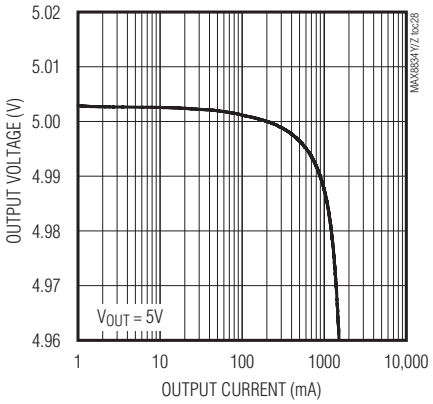
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V, T_A = +25°C, unless otherwise noted.)

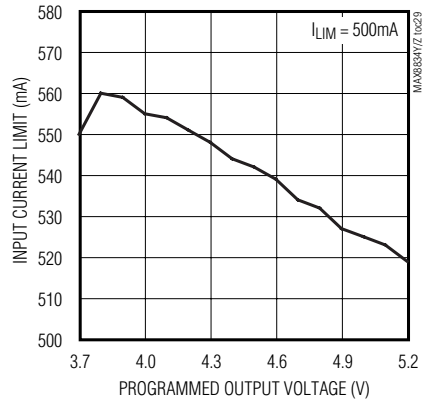
OUTPUT VOLTAGE LOAD REGULATION (MAX8834Y)



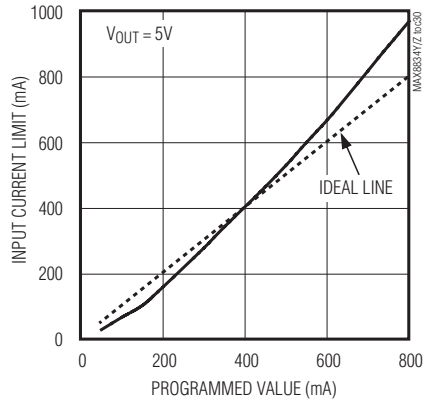
OUTPUT VOLTAGE LOAD REGULATION (MAX8834Z)



INPUT CURRENT LIMIT vs. PROGRAMMED OUTPUT VOLTAGE



INPUT CURRENT LIMIT vs. PROGRAMMED VALUE



Pin Description

PIN	NAME	FUNCTION
A1, B1	OUT	Regulator Output. Connect OUT to the anodes of the external LEDs. Bypass OUT to PGND with a 10µF ceramic capacitor. OUT is connected to LX through an internal 10kΩ resistor during shutdown.
A2, B2	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drains of the internal MOSFETs. LX is connected to OUT through an internal 10kΩ resistor during shutdown.
A3, B3	PGND	Power Ground. Connect PGND to AGND and to the input capacitor ground. Connect PGND to the PCB ground plane.
A4	IN	Analog Supply Voltage Input. The input voltage range is 2.5V to 5.5V. Bypass IN to AGND and PGND with a 10µF ceramic capacitor as close as possible to the IC. IN is high impedance during shutdown.
A5	V_{DD}	Logic Input Supply Voltage. Connect V_{DD} to the logic supply driving SCL, SDA, LED_EN, and GSMB. Bypass V_{DD} to AGND with a 0.1µF ceramic capacitor. When V_{DD} is below the UVLO, the I^2C registers reset and the step-up converter turns off.
B4	SCL	I^2C Clock Input. Data is read on the rising edge of SCL.
B5	AGND	Analog Ground. Connect AGND to PGND and to the input capacitor ground. Connect AGND to the PCB ground plane.
C1	COMP	Compensation Input. See the *Compensation Network Selection* section for details. COMP is internally pulled to AGND through a 180Ω resistor in shutdown.
C2, D2	FGND	FLED1/FLED2 and INDLED Power Ground. Connect FGND to PGND.
C3	LED_EN	LED Enable Logic Input. LED_EN controls FLED1, FLED2, and INDLED, depending on control bits written into the LED_CNTL register. See the LED_EN Control register description for an explanation of this input function. LED_EN has an internal 800kΩ pulldown resistor to AGND.
C4	GSMB	GSM Blank Signal. Assert GSMB to reduce the current regulator settings according to the values programmed into the GSMB_CUR register. The status of the flash safety timer and the flash/movie mode values in the current regulator registers are not affected by the GSMB state. Connect GSMB to the PA module enable signal or other suitable logic signal that indicates a GSM transmit is in process. Polarity of this signal is set by a bit in the GSMB_CUR register (default is active-high). GSMB has an internal 800kΩ pulldown resistor to AGND.
C5	SDA	I^2C Data Input. Data is read on the rising edge of SCL and data is clocked out on the falling edge of SCL.
D1	FLED2	FLED2 Current Regulator. Current flowing into FLED2 is based on the internal I^2C registers FLASH2_CUR and MOVIE_CUR. Connect FLED2 to the cathode of an external flash LED or LED module. FLED2 is high impedance during shutdown. If unused, connect FLED2 to ground.
D3	FLED1	FLED1 Current Regulator. Current flowing into FLED1 is based on the internal I^2C registers FLASH1_CUR and MOVIE_CUR. Connect FLED1 to the cathode of an external flash LED or LED module. FLED1 is high impedance during shutdown. If unused, connect FLED1 to ground.
D4	INDLED	INDLED Current Regulator. Current flowing into INDLED is based on the internal I^2C registers IND_CUR. Connect INDLED to the cathode of an external indicator LED. INDLED is high impedance during shutdown. If unused, connect INDLED to ground.
D5	NTC	NTC Bias Output. NTC provides 20µA to bias the NTC thermistor. The NTC voltage is compared to the trip threshold programmed by the NTC_CNTL register. NTC is high impedance during shutdown. Connect NTC to IN if not used. See the *Finger-Burn Protection (NTC)* section for details.

Adaptive Step-Up Converters with 1.5A Flash Driver

Detailed Description

The MAX8834Y/MAX8834Z flash drivers integrate an adaptive 1.5A PWM step-up DC-DC converter, two 750mA white LED camera flash/movie current regulators, and a 16mA indicator LED current regulator. An I^2C interface controls individual output on/off, the step-up output voltage setting, the movie/flash current, and the flash timer duration settings.

Step-Up Converter (LX, OUT, COMP, PGND)

The MAX8834Y/MAX8834Z include a fixed-frequency, PWM step-up converter that supplies power to the flash LEDs. The output voltage is programmable from 3.7V to 5.2V (in 100mV steps) through the I^2C interface. The output voltage can also be set adaptively based on the LED forward voltage. The step-up converter switches an internal power MOSFET and synchronous rectifier at a constant 2MHz or 4MHz frequency, with varying duty cycle up to 75%, to maintain constant output voltage as the input voltage and load vary. Internal circuitry prevents any unwanted subharmonic switching by forcing a minimum 7% (typ) duty cycle.

When the step-up converter is set to dropout mode, the internal synchronous rectifier is driven fully on, keeping the voltage at OUT equal to the LX input. This mode provides the lowest current consumption when driving LEDs with low forward voltage.

The output voltage is internally monitored for a fault condition. If the output voltage drops below 8% (typ) of the nominal programmed value, a POK fault is indicated in STATUS1 register bit 5. This feature is disabled if the step-up converter is set to operate in adaptive mode.

Overvoltage Protection

The MAX8834Y/MAX8834Z include a comparator to monitor the output voltage (V_{OUT}) during adaptive mode operation of the step-up converter. If at anytime the output voltage exceeds a maximum threshold of 5.5V, the COMP capacitor is discharged until the output voltage is reduced by the 200mV (typ) hysteresis. Once the output voltage drops below this threshold, normal charging of the COMP capacitor is resumed.

Flash Current Regulator (FLED1 and FLED2)

A low-dropout linear current regulator from FLED1/FLED2 to FGND sinks current from the cathode terminal of the flash LED(s). The FLED1/FLED2 current is regulated to I^2C programmable levels for movie mode (up to 125mA, see Table 5) and flash mode (up to 750mA, see Tables 3 and 4). The movie mode provides continuous lighting when enabled through I^2C or LED_EN. When the flash mode is enabled, a flash safety timer, programmable from 50ms to 800ms through I^2C, limits the duration of the flash mode. Once the flash safety timer expires, the current regulators return to movie mode if movie mode was active when a flash event was triggered. The flash mode has priority over the movie mode.

Flash Safety Timer

The flash safety timer is activated any time flash mode is selected, either with LED_EN or through the I^2C interface.

The flash safety timer, programmable from 50ms to 800ms through I^2C, limits the duration of the flash mode in case LED_EN is stuck high or the I^2C command to turn off has not been sent within the programmed flash safety timer duration. This timer can be configured to operate either in one-shot mode or maximum flash duration mode (see Table 9). In one-shot mode, the flash function is initiated on the rising edge of LED_EN (or I^2C bit) and terminated based on the programmed value of the safety timer (see Figure 1). In the maximum flash timer mode, flash function remains enabled as long as LED_EN (or I^2C bit) is high, unless the preprogrammed safety timer times out (see Figure 2).

Once the flash mode is disabled, by either LED_EN, I^2C, or flash safety timer, the flash has to be off for a minimum time (flash safety timer reset inhibit period), before it can be reinitiated (see Figure 3). This prevents spurious events from re-enabling the flash mode.

Indicator Current Regulator (INDLED)

A low-dropout linear current regulator from INDLED to FGND sinks current from the cathode terminal of the indicator LED. The INDLED current is regulated to I^2C programmable levels up to 16mA. Programmable control is provided for ramp-up (OFF to ON) and ramp-down (ON to OFF) times, as well as blink rate and duty cycle. The user can choose to enable or disable the ramp time and blink rate features. See Tables 6, 7, and 8 for more information.

INDLED Blink Function

INDLED current regulator is able to generate a blink function. The OFF and ON time for INDLED are set using the I^2C interface. See Figure 4.

INDLED Ramp Function

The INDLED current regulator output provides ramp-up/down for smooth transition between different brightness settings. The ramp-up/down times are controlled by the

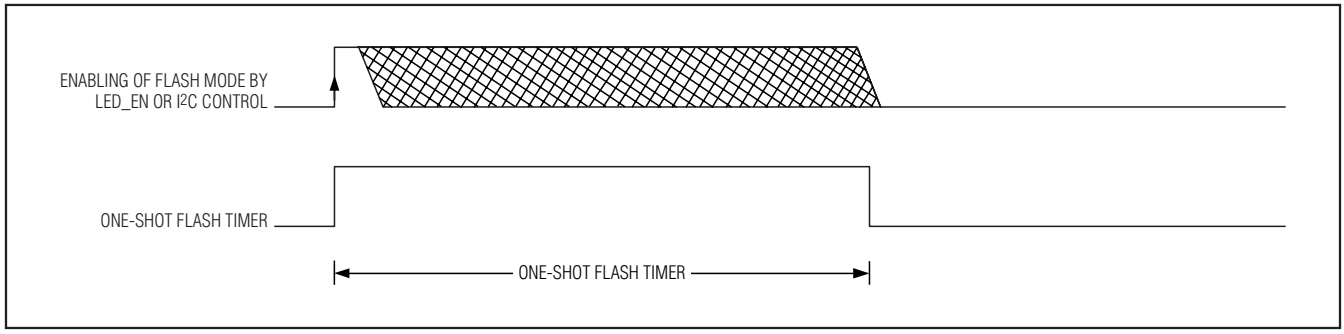


Figure 1. One-Shot Flash-Timer Mode

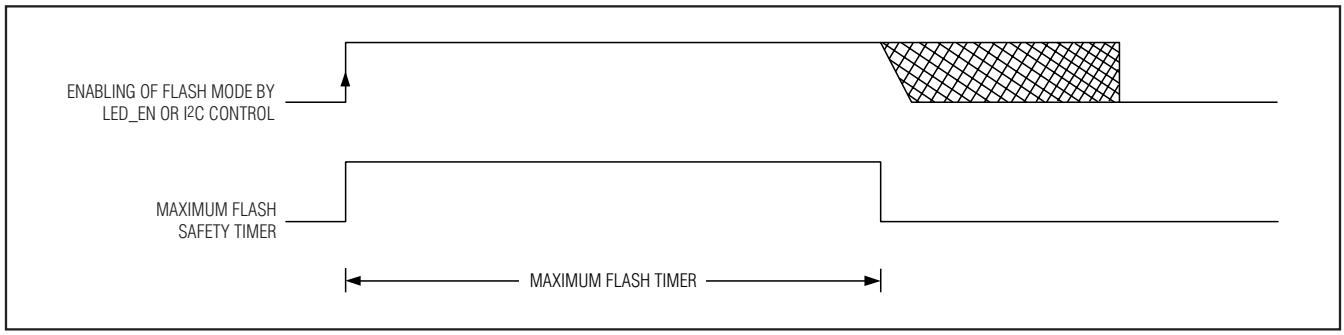


Figure 2. Maximum Flash-Timer Mode

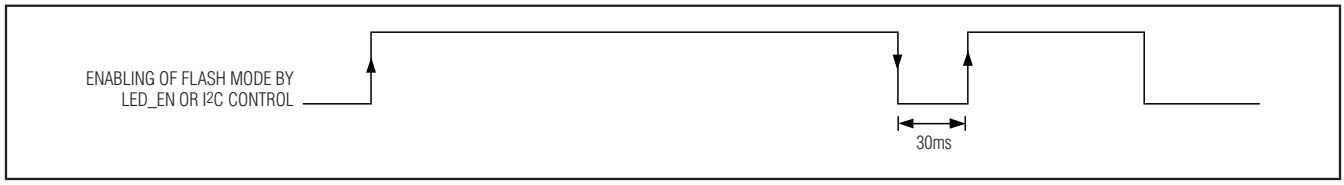


Figure 3. Flash Safety Timer Reset Inhibit Period

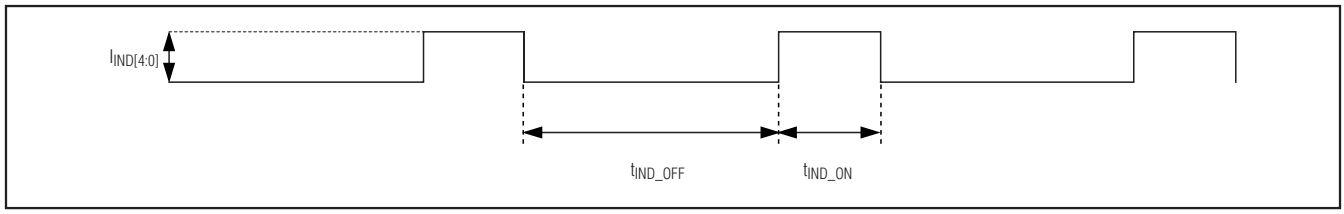


Figure 4. Blink Function Timing

IND_RU and IND_RD control bits, and the ramp function is enabled/disabled by the IND_RP_EN bit. The current regulator increases/decreases the current one-step every $t_{RAMP}/32$ until 0mA or IND[4:0] current is reached. See Figures 5 and 6.

Combining BLINK Timer and Ramp Function

When using the ramp function for INDLED together with the blink timer, keep the ramp-up timer shorter than the ON blink timer and the ramp-down timer shorter than the OFF timer. Failing to comply with this results in the

Adaptive Step-Up Converters with 1.5A Flash Driver

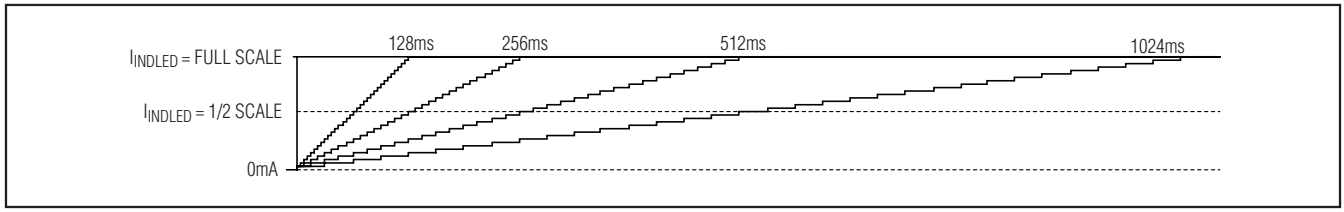


Figure 5. Ramp-Up Behavior

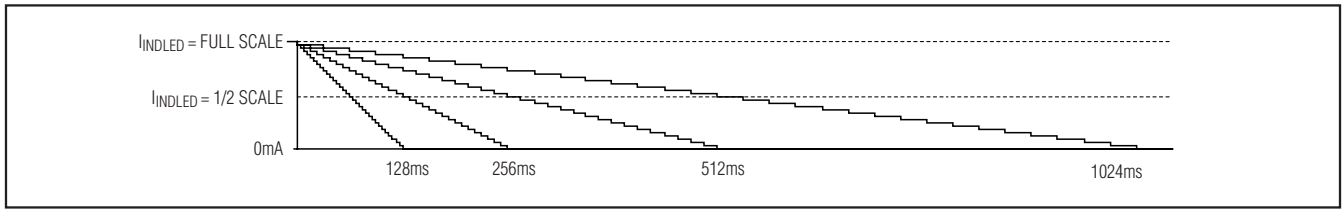


Figure 6. Ramp-Down Behavior

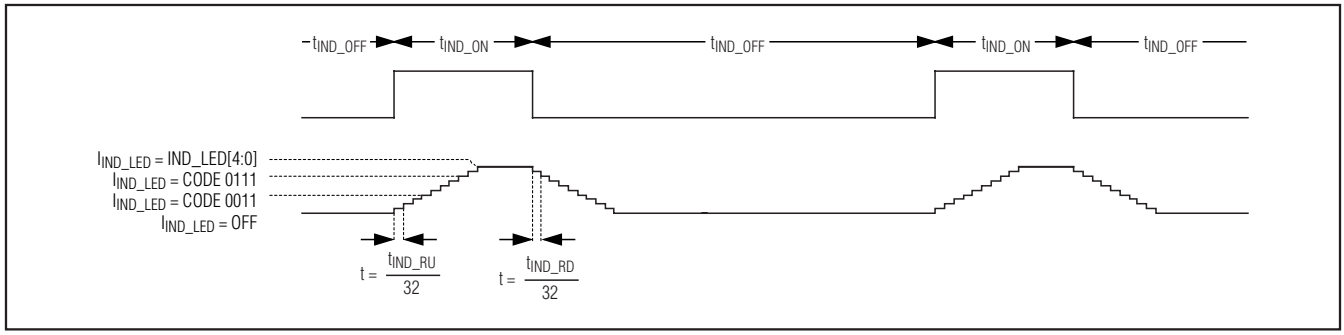


Figure 7. Combining RAMP Function and Blink Timer

programmed current not being reached during the ON time, or the INDLED current not returning to 0mA during the OFF time. See Figure 7.

$$t_{IND\_ON} \geq \frac{t_{IND\_RU}}{32}(IND\_LED + 1)$$

$$t_{IND\_OFF} \geq \frac{t_{IND\_RD}}{32}(IND\_LED + 1)$$

where IND_LED is the code from 0 to 31 specified in the IND_LED[4:0].

LED Enable Input (LED_EN)

The LED_EN logic input can enable/disable the FLED1, FLED2, and INDLED current regulators. It can be programmed to control movie mode, flash mode, and indicator mode by using the IND_EN, MOVIE_EN, and FLASH_EN bits, respectively. See Table 8 for more information.

If FLED1/FLED2 is enabled for both movie and flash modes at the same time, flash mode has priority. Once the safety timer expires, the current regulator then returns to the movie mode.

Watchdog Timer

The MAX8834Y/MAX8834Z include a watchdog timer function that can be programmed using the I^2C interface from 4 seconds to 16 seconds with a 4-second step. If the watchdog timer expires, the MAX8834Y/MAX8834Z interpret it as an indication that the system is no longer responding and enters safe mode. In safe mode, the MAX8834Y/MAX8834Z disable all current regulators and the step-up DC-DC converter to prevent potential damage to the system. The I^2C setting for the respective registers does not change, therefore, resetting the watchdog timer reverts the MAX8834Y/MAX8834Z back to the state present before entering safe mode.

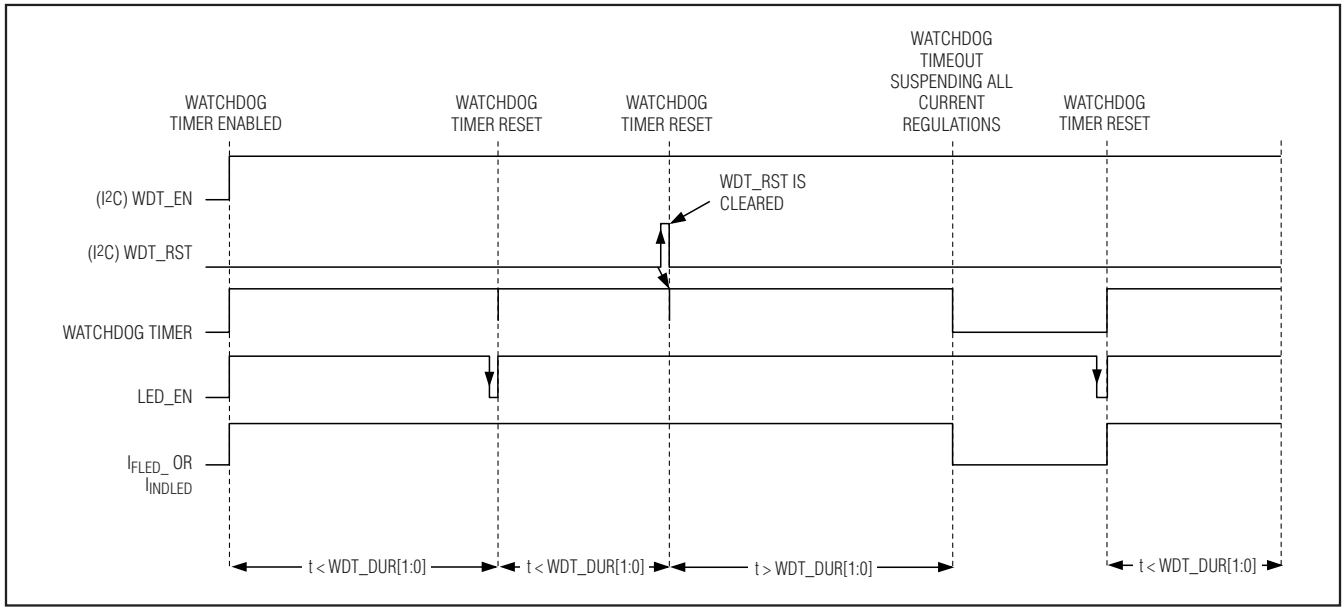


Figure 8. Watchdog Timer Timing Diagram 1

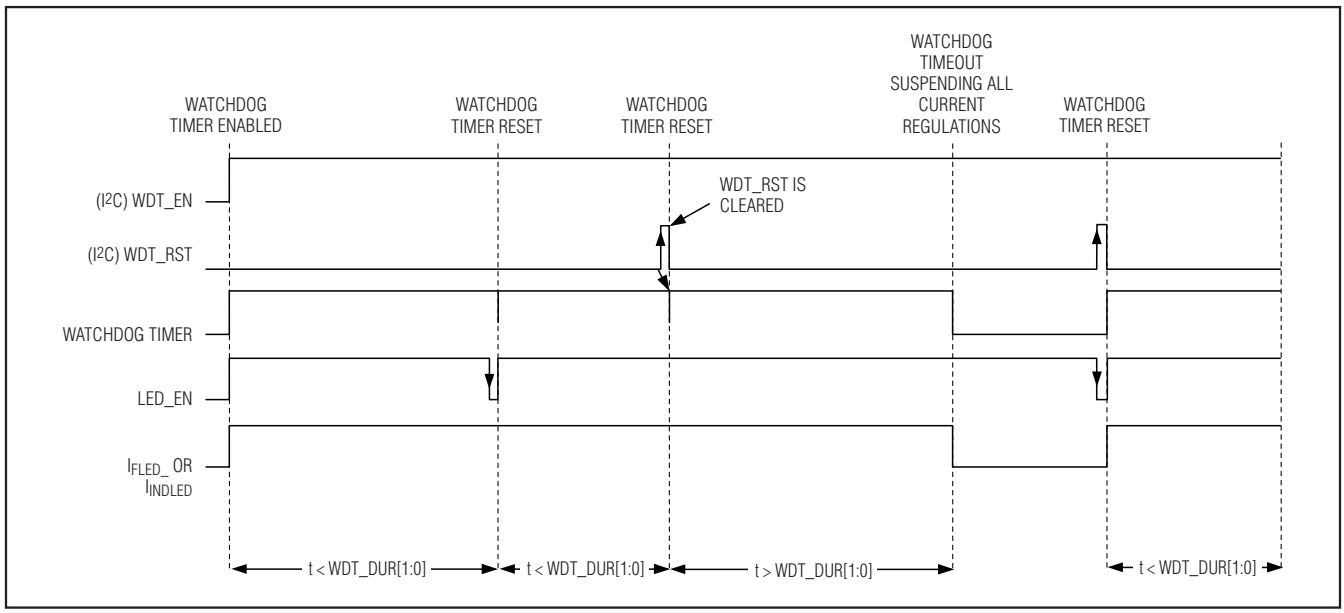


Figure 9. Watchdog Timer Timing Diagram 2

Setting the WDT_EN bit to 1 in the TMR_DUR register (Table 9) enables the watchdog timer. Resetting the watchdog timer is achieved by the rising or falling edge of LED_EN or by setting bit 0 in the WDT_RST register (Table 14). See Figures 8 and 9 for two examples of watchdog timer timing diagrams.

Adaptive Step-Up Converters with 1.5A Flash Driver

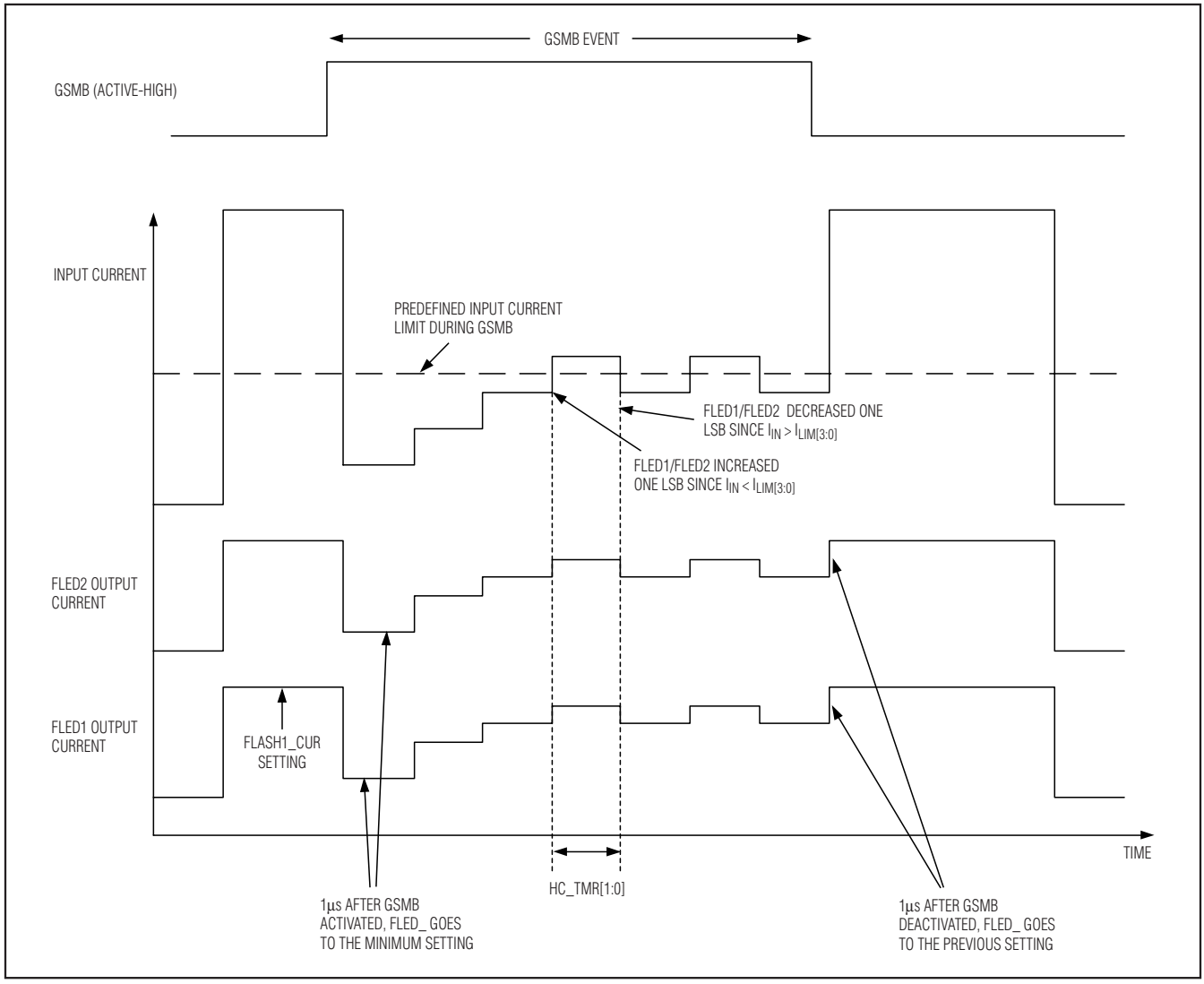


Figure 10. Input Current Limit During GSMB Event

GSM Blank Function (GSMB)

The GSMB input is provided to allow the flash current to be momentarily reduced during a GSM transmit to reduce the peak current drawn from the battery. The input current limit ensures that the maximum possible output current is always provided, regardless of the input voltage and the LED forward voltages.

When a GSMB event is triggered, the FLED1 and FLED2 current regulators go to the lowest setting to ensure the current drawn from the battery is quickly reduced to a safe level. The MAX8834Y/MAX8834Z then start increasing the FLED1 and FLED2 current by one LSB steps, at a time interval set by HC_TMR[1:0] (see Table 11). The increasing continues until either the predefined FLED1/FLED2 current setting is reached or the input current exceeds the maximum predefined input current limit during a GSMB event. When the input current exceeds the predefined input current limit, the FLED1/FLED2 current is reduced by one LSB. The MAX8834Y/MAX8834Z continue to adjust the FLED1 and FLED2 up and down depending on the input current limit as long as the GSMB event is present. See Figure 10 for more detailed information.

To use this feature, connect the logic signal used to enable the PA, or equivalent, to the GSMB input. Assertion of this signal does not change the current status of the flash safety timer or the flash current values stored in the I^2C registers. Once the signal is deasserted, the current regulators change back to their previously programmed values. Polarity of this signal is controlled through bit 6 in the GSMB_CUR register (Table 11). The default is active-high.

Finger-Burn Protection (NTC)

An NTC input is provided for the (optional) finger-burn protection feature. To use this feature, connect a 100kΩ NTC with B = 4550 between NTC and AGND. NTC sources 20µA current and the voltage established by this current and the NTC resistance is compared internally to a voltage threshold in the range of 200mV to 550mV, programmed through bits [2:0] of the NTC Control register (see Table 10).

If the voltage on the NTC pin falls below the programmed threshold during a flash event, the flash cycle is immediately terminated, and an indication is latched through bit 3 in the STATUS1 register (see Table 15).

To disable this function, clear bit 3 (enable bit) in the NTC Control register.

MAXFLASH Function

During high load currents, the battery voltage momentarily drops due to its internal ESR, together with the serial impedance from the battery to the load. For equipment requiring a minimum voltage for stable operation, the battery ESR needs to be calculated to estimate the maximum battery current that maintains the battery voltage above the critical threshold. Due to the complicated measurement of the battery ESR, the MAX8834Y/MAX8834Z feature the MAXFLASH function to prevent the battery voltage from dropping below the threshold voltage. See Figure 11 for details.

The MAX8834Y/MAX8834Z input voltage is monitored during a FLASH/MOVIE event. If the input voltage drops below a predefined threshold (V_{LB_TH}), it indicates that the FLASH/MOVIE event is drawing more current than the battery can support. As a result, the FLED1/FLED2 current regulators start decreasing their output currents by one step. Therefore, the input current is reduced and the input voltage starts to rise due to the internal battery ESR. The input voltage is then sampled again after t_{LB_TMR} and compared to V_{LB_TH} plus a predefined hysteresis (V_{LB_HYS}). If it is still below V_{LB_TH} + V_{LB_HYS}, the FLED1/FLED2 current regulators reduce their output current again to ensure that minimum input voltage is available for the system. If the input voltage is above V_{LB_TH} + V_{LB_HYS}, the current regulator increases the output current by one step (if it is less than the user-defined output current). To disable the hysteresis, set LB_HYS[1:0] to 11. In this case, after the FLED1/FLED2 current is reduced, it stays at the current setting. Figures 12, 13, and 14 show examples of MAXFLASH function operation. See Tables 12 and 13 for control register details.

The MAXFLASH function continues for the entire duration of the FLASH/MOVIE event to ensure that the FLASH/MOVIE output current is always maximized for the specific operating conditions.

Undervoltage Lockout

The MAX8834Y/MAX8834Z contain undervoltage lockout (UVLO) circuitry that disables the IC until V_{IN} is greater than 2.3V (typ). Once V_{IN} rises above 2.3V (typ), the UVLO circuitry does not disable the IC until V_{IN} falls below the UVLO threshold minus the hysteresis voltage. The MAX8834Y/MAX8834Z also contain a V_{DD} UVLO circuitry that monitors the V_{DD} voltage. When the V_{DD} voltage falls below 1.4V (typ), the contents of all the logic registers are reset to their default states. The logic registers are only reset in a V_{DD} UVLO condition and not an IN UVLO condition.

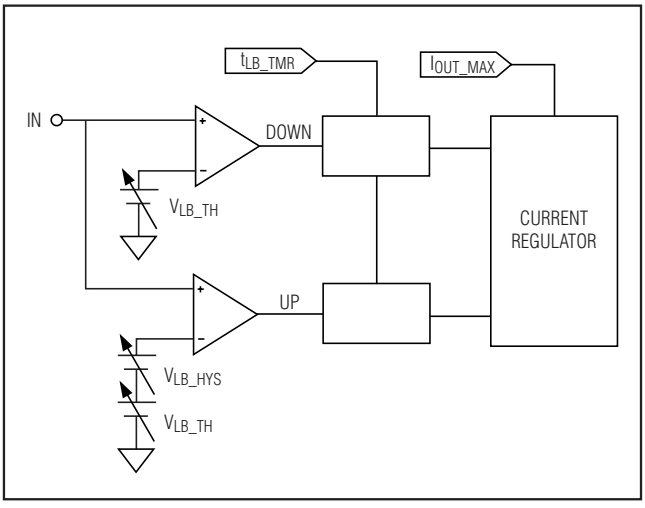


Figure 11. Block Diagram of MAXFLASH Function

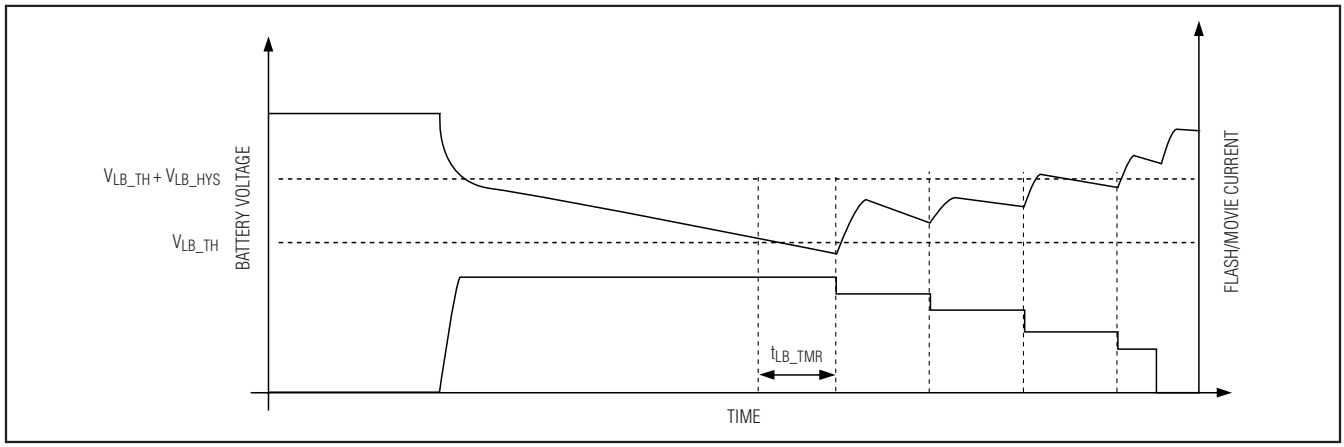


Figure 12. Example 1 of MAXFLASH Function Operation

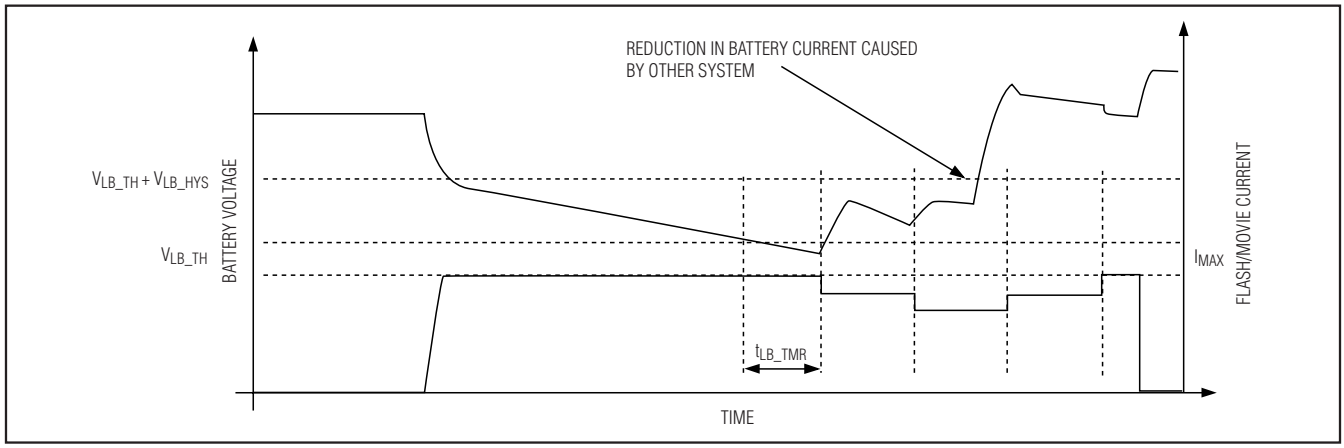


Figure 13. Example 2 of MAXFLASH Function Operation

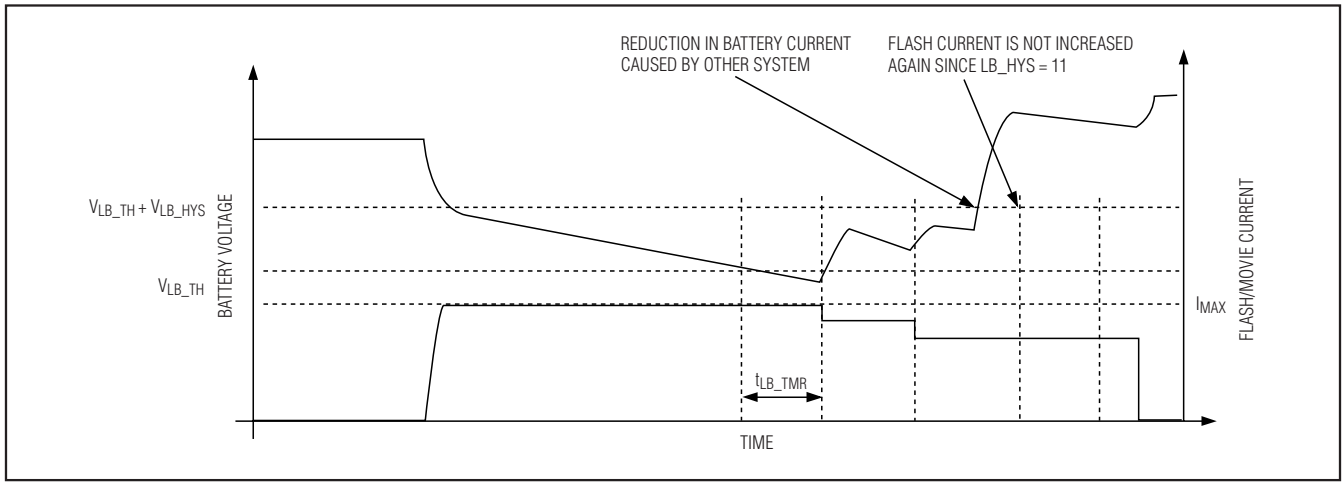


Figure 14. Example 3 of MAXFLASH Function Operation with Hysteresis Disabled

Soft-Start

The step-up converter implements a soft-start to control inrush current when it turns on. It soft-starts by charging C_{COMP} with a 100µA current source. During this time, the internal MOSFET is switching at the minimum duty cycle. Once V_{COMP} rises above 1V, the duty cycle increases until the output voltage reaches the desired regulation level. COMP is pulled to AGND with a 180Ω (typ) internal resistor during IN, UVLO, dropout mode, or shutdown. See the *Typical Operating Characteristics* for an example of soft-start operation. Soft-start is reinitiated after UVLO or if the step-up converter is re-enabled after shutdown or dropout mode.

Shutdown and Standby

The MAX8834Y/MAX8834Z are in shutdown when either V_{IN} or V_{DD} are in UVLO. In shutdown, supply current is reduced to 0.1µA (typ). When V_{IN} is above its UVLO threshold, but V_{DD} is below its UVLO threshold, the IC disables its internal reference, keeps all registers reset, turns the step-up converter off, and turns the FLED1/FLED2 current regulators off (high impedance). Once a logic-level voltage is supplied to V_{DD}, the IC enters standby condition and is ready to accept I^2C commands. The internal MOSFET, synchronous rectifier, and FLED1/FLED2 are also high impedance in standby.

Typical shutdown timing characteristics are shown in the *Typical Operating Characteristics*.

Parallel Connection of Current Regulators

The FLED1/FLED2 current regulators can be connected in parallel as long as the system software properly sets the current levels for each regulator. Unused current regulators may be connected to ground. The FLED1/FLED2 regulators must be disabled through I^2C to avoid a fault detection from an open or short.

Open/Short Detection

The MAX8834Y/MAX8834Z monitor the FLED1, FLED2, and INDLED voltage to detect any open or short LEDs. A short fault is detected when the voltage rises above V_{OUT} - 1V (typ), and an open fault is detected when the voltage falls below 100mV. The fault detection circuitry is only activated when the corresponding current regulator is enabled and provides a continuous monitor of the current regulator condition. Once a fault is detected, the corresponding current regulator is disabled and the status is latched into the corresponding fault register bit (see Table 15). This allows the processor to determine the MAX8834Y/MAX8834Z operating condition.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX8834Y/MAX8834Z. When the junction temperature exceeds +160°C (typ), the IC turns off, allowing itself to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal overload conditions.

I^2C Serial Interface

An I^2C-compatible, 2-wire serial interface controls the step-up converter output voltage, flash, movie, and indicator current settings, flash duration, and other parameters. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The MAX8834Y/MAX8834Z are slave-only devices, relying upon a master to generate a clock signal. The master initiates data transfer to and from the MAX8834Y/

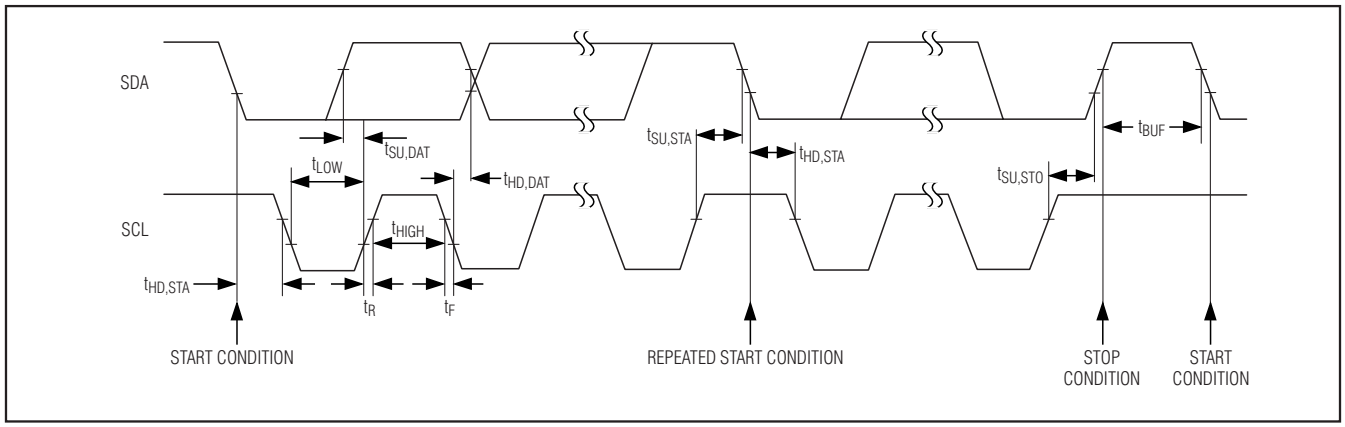


Figure 15. 2-Wire Serial Interface Timing Detail

Adaptive Step-Up Converters with 1.5A Flash Driver

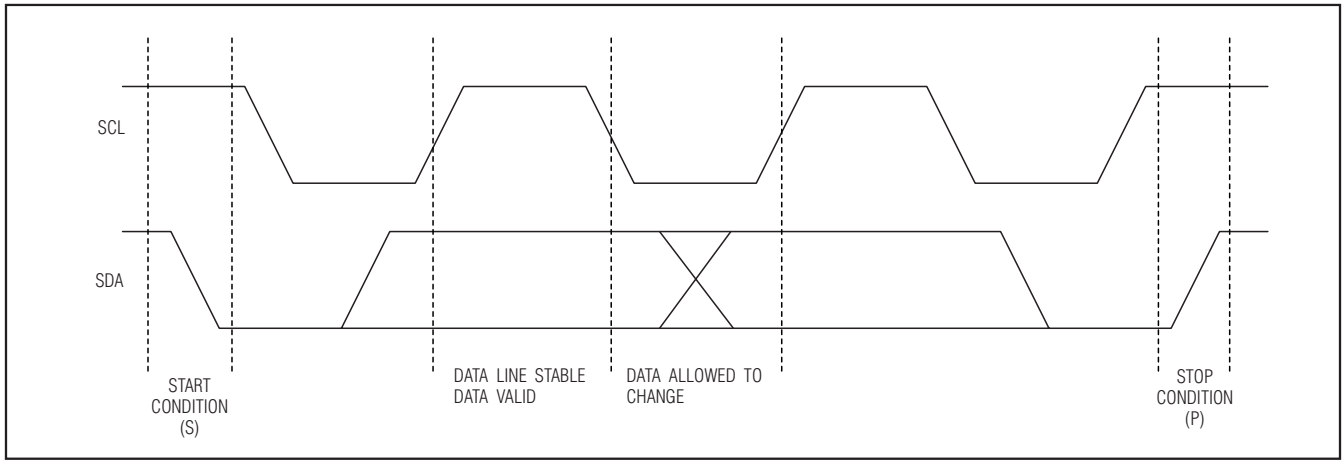


Figure 16. Bit Transfer

MAX8834Z and generates SCL to synchronize the data transfer (Figure 15).

I^2C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to assure proper device operation.

A bus master initiates communication with the MAX8834Y/MAX8834Z as a slave device by issuing a START (S) condition followed by the MAX8834Y/MAX8834Z address. The MAX8834Y/MAX8834Z address byte consists of 7 address bits and a read/write bit (R/$\overline{W}$). After receiving the proper address, the MAX8834Y/MAX8834Z issue an acknowledge bit by pulling SDA low during the ninth clock cycle.

Slave Address

The MAX8834Y/MAX8834Z act as a slave transmitter/receiver. Its slave address is 0x94 for write operations and 0x95 for read operations.

Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock (Figure 16).

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the MAX8834Y/MAX8834Z, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 17). Both START and STOP conditions are generated by the bus master.

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data (Figure 18). After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse so the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the MAX8834Y/MAX8834Z, it releases the SDA line and the MAX8834Y/MAX8834Z take control of the SDA line and generate the acknowledge bit. When SDA remains high during this 9th clock pulse, this is defined as the not acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

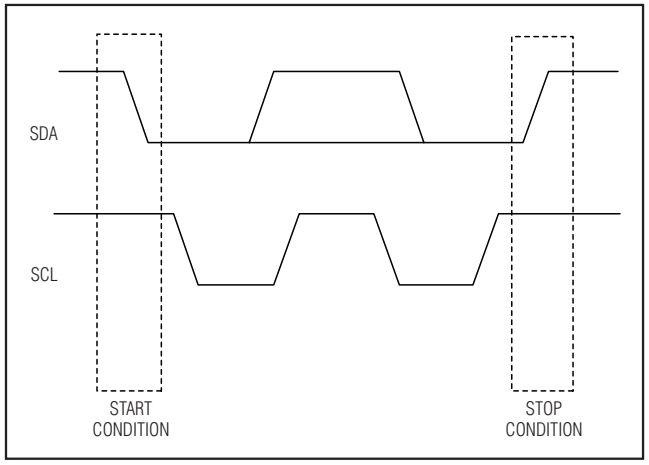


Figure 17. START and STOP Conditions

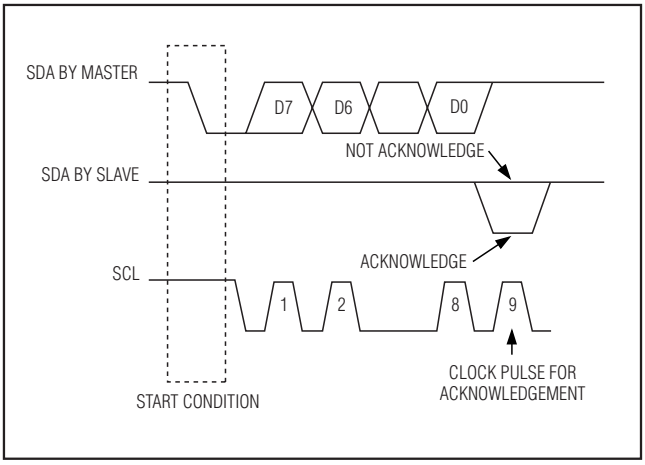


Figure 18. Acknowledge

Write Operations

The MAX8834Y/MAX8834Z recognize the write byte protocol as defined in the SMBus™ specification and shown in section A of Figure 19. The write byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write-byte protocol requires a register pointer address for the subsequent write. The MAX8834Y/MAX8834Z acknowledge any register pointer even though only a subset of those registers actually exists in the device. The write byte protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) The master sends a STOP (P) condition.

In addition to the write-byte protocol, the MAX8834Y/MAX8834Z can write to multiple registers as shown in section B of Figure 19. This protocol allows the I²C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

Read Operations

The method for reading a single register (byte) is shown in section A of Figure 20. To read a single register:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.

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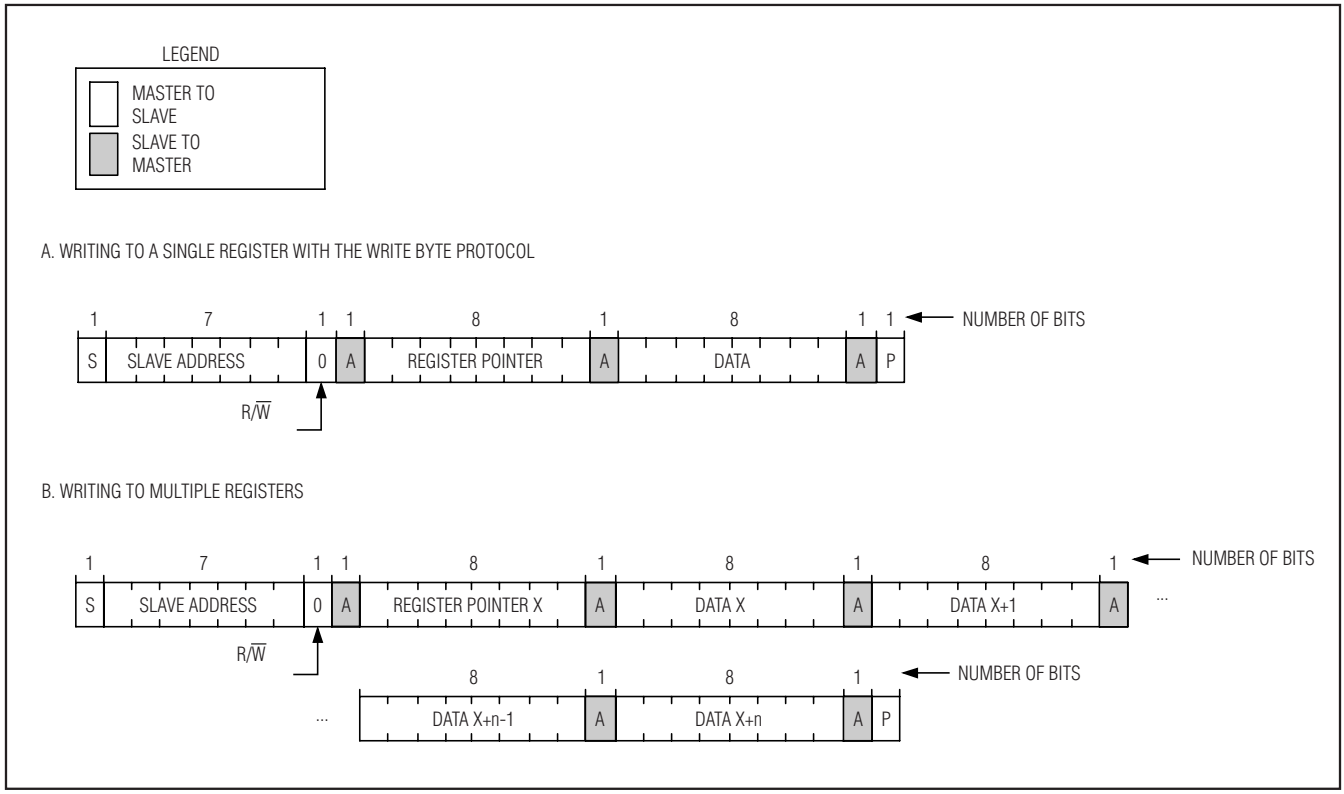


Figure 19. Writing to the MAX8834Y/MAX8834Z

5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START (Sr) condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) The master sends a STOP (P) condition.

In addition, the MAX8834Y/MAX8834Z can read a block of multiple sequential registers as shown in section B of Figure 20. Use the following procedure to read a sequential block of registers:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

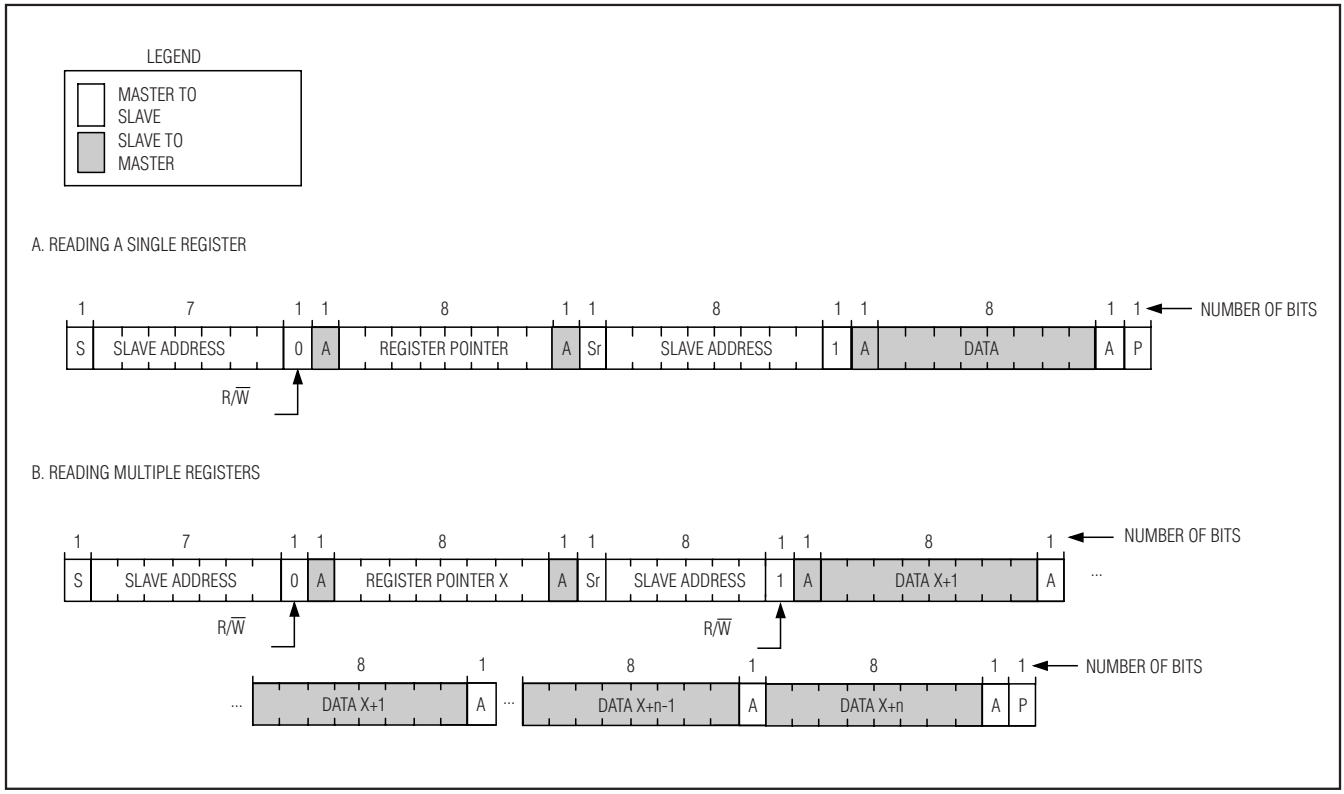


Figure 20. Reading from the MAX8834Y/MAX8834Z

Adaptive Step-Up Converters with 1.5A Flash Driver

Table 1. Register Map

NAME	TABLE	REGISTER ADDRESS (hex)	TYPE	DESCRIPTION
BOOST_CNTL	Table 2	00	R/$\overline{W}$	Step-up converter control
FLASH1_CUR	Table 3	01	R/$\overline{W}$	FLED1 flash current control
FLASH2_CUR	Table 4	02	R/$\overline{W}$	FLED2 flash current control
MOVIE_CUR	Table 5	03	R/$\overline{W}$	FLED1 and FLED2 movie current control
Reserved for future use	—	04	R/$\overline{W}$	Reserved for future use
IND_CUR	Table 6	05	R/$\overline{W}$	Indicator LED current control
Reserved for future use	—	06	R/$\overline{W}$	Reserved for future use
IND_CNTL	Table 7	07	R/$\overline{W}$	Indicator LED ramp and blink control
Reserved for future use	—	08	R/$\overline{W}$	Reserved for future use
LED_CNTL	Table 8	09	R/$\overline{W}$	FLED1, FLED2, and INDLED on/off and mode control, and definition of LED_EN logic input function
TMR_DUR	Table 9	0A	R/$\overline{W}$	Watchdog timer and flash safety timer control
NTC_CNTL	Table 10	0B	R/$\overline{W}$	NTC function control
GSMB_CUR	Table 11	0C	R/$\overline{W}$	FLED1 and FLED2 current control during GSM transmit
MAXFLASH1	Table 12	0D	R/$\overline{W}$	MAXFLASH function register 1
MAXFLASH2	Table 13	0E	R/$\overline{W}$	MAXFLASH function register 2
WDT_RST	Table 14	16	R/$\overline{W}$	Watchdog timer reset
STATUS1	Table 15	17	R	Status register
STATUS2	Table 16	18	R	Status register
Reserved for future use	—	19	R/$\overline{W}$	Reserved for future use
CHIP_ID1	Table 17	1A	R	Die type information
CHIP_ID2	Table 18	1B	R	Die type and mask revision information

Table 2. BOOST_CNTL

This register contains step-up converter control values.

REGISTER NAME	BOOST_CNTL
Address	0x00
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	0
B6	BOOST_EN	0 = Step-up converter off 1 = Step-up converter on	0
B5	BOOST_MODE	00 = Step-up voltage set adaptively 01 = Step-up voltage set programmatically according to BOOST_CNTL[3:0] 10 = Step-up converter runs in dropout 11 = Step-up converter automatically changes between adaptive regulation and dropout mode depending on operating conditions	00
B4			
B3	BOOST_CNTL[3:0]	0000 = 3.7V 0001 = 3.8V 0010 = 3.9V 0011 = 4.0V 0100 = 4.1V 0101 = 4.2V 0110 = 4.3V 0111 = 4.4V 1000 = 4.5V 1001 = 4.6V 1010 = 4.7V 1011 = 4.8V 1100 = 4.9V 1101 = 5.0V 1110 = 5.1V 1111 = 5.2V	0000
B2			
B1			
B0 (LSB)			

Table 3. FLASH1_CUR

This register contains FLED1 flash current control values.

REGISTER NAME	FLASH1_CUR
Address	0x01
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FLASH1[4:0]	**FLED1 Flash Mode Current Setting** 00000 = 23.44mA 00001 = 46.88mA 00010 = 70.32mA 00011 = 93.76mA 00100 = 117.20mA 00101 = 140.64mA 00110 = 164.08mA 00111 = 187.52mA 01000 = 210.96mA 01001 = 234.40mA 01010 = 257.84mA 01011 = 281.28mA 01100 = 304.72mA 01101 = 328.16mA 01110 = 351.60mA 01111 = 375.04mA 10000 = 398.48mA 10001 = 421.92mA 10010 = 445.36mA 10011 = 468.80mA 10100 = 492.24mA 10101 = 515.68mA 10110 = 539.12mA 10111 = 562.56mA 11000 = 586.00mA 11001 = 609.44mA 11010 = 632.88mA 11011 = 656.32mA 11100 = 679.76mA 11101 = 703.20mA 11110 = 726.56mA 11111 = 750.00mA	00000
B6			
B5			
B4			
B3			
B2	—	Reserved for future use	—
B1	—	Reserved for future use	—
B0 (LSB)	—	Reserved for future use	—

Table 4. FLASH2_CUR

This register contains FLED2 flash current control values.

REGISTER NAME	FLASH2_CUR
Address	0x02
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FLASH2[4:0]	**FLED2 Flash Mode Current Setting** 00000 = 23.44mA 00001 = 46.88mA 00010 = 70.32mA 00011 = 93.76mA 00100 = 117.20mA 00101 = 140.64mA 00110 = 164.08mA 00111 = 187.52mA 01000 = 210.96mA 01001 = 234.40mA 01010 = 257.84mA 01011 = 281.28mA 01100 = 304.72mA 01101 = 328.16mA 01110 = 351.60mA 01111 = 375.04mA 10000 = 398.48mA 10001 = 421.92mA 10010 = 445.36mA 10011 = 468.80mA 10100 = 492.24mA 10101 = 515.68mA 10110 = 539.12mA 10111 = 562.56mA 11000 = 586.00mA 11001 = 609.44mA 11010 = 632.88mA 11011 = 656.32mA 11100 = 679.76mA 11101 = 703.20mA 11110 = 726.56mA 11111 = 750.00mA	00000
B6			
B5			
B4			
B3			
B2	—	Reserved for future use	—
B1	—	Reserved for future use	—
B0 (LSB)	—	Reserved for future use	—

Table 5. MOVIE_CUR

This register contains FLED1 and FLED2 movie current control values.

REGISTER NAME	MOVIE_CUR
Address	0x03
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT NAME
B7 (MSB)	—	Reserved for future use	—
B6	MOVIE1[2:0]	**FLED1 Movie Mode Current Setting** 000 = 15.625mA 001 = 31.250mA 010 = 49.875mA 011 = 62.500mA 100 = 78.125mA 101 = 93.750mA 110 = 109.375mA 111 = 125.000mA	000
B5			
B4			
B3	—	Reserved for future use	—
B2	MOVIE2[2:0]	**FLED2 Movie Mode Current Setting** 000 = 15.625mA 001 = 31.250mA 010 = 49.875mA 011 = 62.500mA 100 = 78.125mA 101 = 93.750mA 110 = 109.375mA 111 = 125.000mA	000
B1			
B0 (LSB)			

Table 6. IND_CUR

This register contains indicator LED current control values.

REGISTER NAME	IND_CUR
Address	0x05
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	0
B6	IND_BL_EN	**INDLED Indicator Blink Timer Enable** 0 = Indicator blink is disabled 1 = Indicator blink is enabled	0
B5	IND_RP_EN	**INDLED Indicator Ramp-Up/Down Enable** 0 = Indicator ramp-up/down is disabled 1= Indicator ramp-up/down is enabled	0
B4 B3 B2 B1 B0 (LSB)	IND[4:0]	**INDLED Indicator Mode Current Setting** 00000 = 0.5mA 00001 = 1.0mA 00010 = 1.5mA 00011 = 2.0mA 00100 = 2.5mA 00101 = 3.0mA 00110 = 3.5mA 00111 = 4.0mA 01000 = 4.5mA 01001 = 5.0mA 01010 = 5.5mA 01011 = 6.0mA 01100 = 6.5mA 01101 = 7.0mA 01110 = 7.5mA 01111 = 8.0mA 10000 = 8.5mA 10001 = 9.0mA 10010 = 9.5mA 10011 = 10.0mA 10100 = 10.5mA 10101 = 11.0mA 10110 = 11.5mA 10111 = 12.0mA 11000 = 12.5mA 11001 = 13.0mA 11010 = 13.5mA 11011 = 14.0mA 11100 = 14.5mA 11101 = 15.0mA 11110 = 15.5mA 11111 = 16.0mA	00000

Table 7. IND_CNTL

This register contains indicator LED ramp and blink timer control.

REGISTER NAME	IND_CNTL
Address	0x07
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	IND_OFF	**INDLED Indicator Off Blink Timer Control** 00 = 512ms 01 = 1024ms 10 = 2048ms 11 = 4096ms	00
B6			
B5	IND_ON	**INDLED Indicator On Blink Timer Control** 00 = 128ms 01 = 256ms 10 = 512ms 11 = 1024ms	00
B4			
B3	IND_RU[1:0]	**INDLED Indicator Ramp-Up Timer Control** 00 = 128ms 01 = 256ms 10 = 512ms 11 = 1024ms	00
B2			
B1	IND_RD[1:0]	**INDLED Indicator Ramp-Down Timer Control** 00 = 128ms 01 = 256ms 10 = 512ms 11 = 1024ms	00
B0 (LSB)			

Table 8. LED_CNTL

This register contains FLED1, FLED2 and INDLED on/off and mode control.

REGISTER NAME	LED_CNTL
Address	0x09
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB) B6	IND_EN[1:0]	**INDLED Indicator Current Regulator Enable** 00 = INDLED indicator LED is disabled 01 = INDLED indicator LED is disabled 10 = INDLED indicator LED is enabled 11 = INDLED indicator LED is controlled by LED_EN input	00
B5 B4 B3	MOVIE_EN[2:0]	**FLED1/FLED2 MOVIE Mode Current Regulator Enable** 000 = FLED1 and FLED2 movie mode disabled 001 = FLED1 movie mode is enabled, FLED2 movie mode is disabled 010 = FLED2 movie mode is enabled, FLED1 movie mode is disabled 011 = FLED1 and FLED2 movie mode is enabled 101 = FLED1 movie mode is controlled by LED_EN, FLED2 movie mode is disabled 110 = FLED2 movie mode is controlled by LED_EN, FLED1 movie mode is disabled 111 = FLED1 and FLED2 movie mode is controlled by LED_EN	000
B2 B1 B0 (LSB)	FLASH_EN[2:0]	**FLED1/FLED2 Flash Mode Current Regulator Enable** 000 = FLED1 and FLED2 flash mode disabled 001 = FLED1 flash mode is enabled, FLED2 flash mode is disabled 010 = FLED2 flash mode is enabled, FLED1 flash mode is disabled 011 = FLED1 and FLED2 flash mode is enabled 101 = FLED1 flash mode is controlled by LED_EN, FLED2 flash mode is disabled 110 = FLED2 flash mode is controlled by LED_EN, FLED1 flash mode is disabled 111 = FLED1 and FLED2 flash mode is controlled by LED_EN	000

Table 9. TMR_DUR

This register contains watchdog timer and flash safety time-control values.

REGISTER NAME	TMR_DUR
Address	0x0A
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	WDT_EN	**Enable/Disable Of Watchdog Timer Function** 0 = WDT is disabled 1 = WDT is enabled	0
B6	WDT_DUR[1:0]	**Watchdog Timer Duration** 00 = 4s 01 = 8s 10 = 12s 11 = 16s	00
B5			
B4	TMR_MODE	**Safety Timer Control** 0 = One-shot mode—generates a flash with a duration of TMR_DUR regardless of LED:EN and I^2C setting; pulling V_{DD} low in this condition terminates flash operating and puts the IC into power-down mode 1 = Maximum timer mode—ensures that flash duration does not exceed the timer defined in TMR:DUR	0
B3	TMR_DUR [3:0]	**Safety Timer Duration Control** 0000 = 50ms 0001 = 100ms 0010 = 150ms 0011 = 200ms 0100 = 250ms 0101 = 300ms 0110 = 350ms 0111 = 400ms 1000 = 450ms 1001 = 500ms 1010 = 550ms 1011 = 600ms 1100 = 650ms 1101 = 700ms 1110 = 750ms 1111 = 800ms	0000
B2			
B1			
B0 (LSB)			

Table 10. NTC_CNTL

This register contains NTC function control values.

REGISTER NAME	NTC_CNTL
Address	0x0B
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FLASH_TMR_CNTL	**Flash Safety Timer Reset Control** 0 = Enable FLASH reset timer, only valid when FLASH mode is enabled using the LED_EN; LED_EN needs to be pulled low for minimum 30ms (typ) to reset the flash safety 1 = Disable FLASH reset timer; flash safety timer is reset as soon as LED_EN is pulled low	0
B6	—	Reserved for future use	0
B5	—	Reserved for future use	0
B4	—	Reserved for future use	0
B3	NTC_EN	**Finger-Burn Feature Enable** 0 = Disable NTC function 1 = Enable NTC function	0
B2	NTC[2:0]	**Finger-Burn Threshold Control** 000 = 200mV 001 = 250mV 010 = 300mV 011 = 350mV 100 = 400mV 101 = 450mV 110 = 500mV 111 = 550mV	000
B1			
B0 (LSB)			

Table 11. GSMB_CUR

This register contains FLED1 and FLED2 current control values for the GSMB function.

REGISTER NAME	GSMB_CUR
Address	0x0C
Reset Value	0xC0
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	GSMB_EN	**GSM Blank Enable** 0 = GSMB input is disabled 1 = GSMB input is enabled	1
B6	GSMB_POL	**GSM Blank Polarity Control** 0 = GSMB is active-low 1 = GSMB is active-high	1
B5 B4 B3 B2	ILIM[3:0]	**Input Current Limit During GSMB** 0000 = 50mA 0001 = 100mA 0010 = 150mA 0011 = 200mA 0100 = 250mA 0101 = 300mA 0110 = 350mA 0111 = 400mA 1000 = 450mA 1001 = 500mA 1010 = 550mA 1011 = 600mA 1100 = 650mA 1101 = 700mA 1110 = 750mA 1111 = 800mA	0000
B1 B0 (LSB)	HC_TMR[1:0]	**GSMB Reset Timer** 00 = 10µs 01 = 20µs 10 = 40µs 11 = 80µs	00

Table 12. MAXFLASH1

This register contains MAXFLASH control function.

REGISTER NAME	MAXFLASH1
Address	0x0D
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	LB_EN	**MAXFLASH Function Enable** 0 = Disabled 1 = Low-battery function is enabled	0
B6 B5 B4 B3 B2	LB_TH[4:0]	**Low-Battery Detection Threshold** 00000 = 2.400V [Do not use] 00001 = 2.433V [Do not use] 00010 = 2.466V [Do not use] 00011 = 2.500V 00100 = 2.533V 00101 = 2.566V 00110 = 2.600V 00111 = 2.633V 01000 = 2.666V 01001 = 2.700V 01010 = 2.733V 01011 = 2.766V 01100 = 2.800V 01101 = 2.833V 01110 = 2.866V 01111 = 2.900V 10000 = 2.933V 10001 = 2.966V 10010 = 3.000V 10011 = 3.033V 10100 = 3.066V 10101 = 3.100V 10110 = 3.133V 10111 = 3.166V 11000 = 3.200V 11001 = 3.233V 11010 = 3.266V 11011 = 3.300V 11100 = 3.333V 11101 = 3.366V 11110 = 3.400V 11111 = 3.400V	00000
B1 B0 (LSB)	LB_HYS[1:0]	**Low-Battery Detection Hysteresis** 00 = 100mV 01 = 200mV 10 = Reserved for future use 11 = Hysteresis is disabled—flash current is only reduced	00

Table 13. MAXFLASH2

This register contains MAXFLASH control function.

REGISTER NAME	MAXFLASH2
Address	0x0E
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	0
B6	—	Reserved for future use	0
B4	—	Reserved for future use	0
B3	—	Reserved for future use	0
B3	—	Reserved for future use	0
B2	—	Reserved for future use	0
B1	LB_TMR[1:0]	**Low-Battery Reset Timer** 00 = 0.250ms 01 = 0.500ms 10 = Reserved for future use 11 = Reserved for future use	00
B0 (LSB)			

Table 14. WDT_RST

This register contains watchdog reset function.

REGISTER NAME	WDT_RST
Address	0x16
Reset Value	0x00
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	0
B6	—	Reserved for future use	0
B4	—	Reserved for future use	0
B3	—	Reserved for future use	0
B3	—	Reserved for future use	0
B2	—	Reserved for future use	0
B1	—	Reserved for future use	0
B0 (LSB)	—	**Watchdog Reset** 0 = Default 1 = Writing a 1 resets the watchdog timer; after writing a 1, this bit is cleared upon watchdog timer reset	—

Table 15. STATUS1

This register contains status information.

REGISTER NAME	STATUS1
Address	0x17
Reset Value	N/A
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	NTC_FLT	**NTC Status Readback** 0 = NTC status OK 1 = Fault (short) occurred on NTC	0
B6	GSMB	**GSMB Status Readback** 0 = No GSMB event has occurred 1 = GSMB event has occurred	0
B5	POK_FLT	**POK Window Cooperator Status Readback** 0 = Output voltage is within POK window 1 = POK fault has occurred	0
B4	OVER_TEMP	**Die Temperature Overload Condition Status Readback** 0 = Die temp is within spec 1 = Die overtemp event has occurred	0
B3	NTC_OVT	**NTC Status Readback** 0 = NTC temperature is within spec 1 = NTC temperature threshold has tripped	0
B2	INDLED_FLT	**INDLED Status Readback** 0 = INDLED status is OK 1 = Fault (open/short) has occurred on INDLED	0
B1	FLED2_FLT	**FLED2 Status Readback** 0 = FLED2 status is OK 1 = Fault (open/short) has occurred on FLED2	0
B0 (LSB)	FLED1_FLT	**FLED1 Status Readback** 0 = FLED1 status is OK 1 = Fault (open/short) has occurred on FLED1	0

Note: *All faults are latched. Bit(s) are cleared after reading register contents. If the fault is still present, the bit is set again.*

Table 16. STATUS2

This register contains status information.

REGISTER NAME	STATUS2
Address	0x18
Reset Value	N/A
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	MAXFLASH_STAT	**Indication of if MAXFLASH Function Has Been Triggered Since Last Read Operation of This Register** 0 = MAXFLASH event has not occurred 1 = MAXFLASH event has occurred	0
B6	GSMB_ILIM	**Indication of if Input Current Limit Has Been Reached During GSMB Since Last Read Operation of This Register** 0 = Input current limit not reached 1 = Input current limit reached	0
B5	—	Reserved for future use	0
B4	—	Reserved for future use	0
B3	—	Reserved for future use	0
B2	—	Reserved for future use	0
B1	—	Reserved for future use	0
B0 (LSB)	—	Reserved for future use	0

Table 17. CHIP_ID1

This register contains the MAX8834Y/MAX8834Z die type number.

REGISTER NAME	CHIP_ID1
Address	0x1A
Reset Value	N/A
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	DIE_TYPE[7:4]	BCD Character 1	[0001]
B6			
B5			
B4			
B3	DIE_TYPE[3:0]	BCD Character 1	[0001]
B2			
B1			
B0 (LSB)			

Note: *This register value is fixed in metal.*

Table 18. CHIP_ID2

This register contains the die type dash number (0 = plain) and mask revision level.

REGISTER NAME	CHIP_ID2
Address	0x1B
Reset Value	N/A
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	DASH	BCD Character representing dash number	—
B6			
B5			
B4			
B3	MASK_REV	BCD Character representing die revision	—
B2			
B1			
B0 (LSB)			

Applications Information

Inductor Selection

See Table 19 for a list of recommended inductors. To prevent core saturation, ensure that the inductor saturation current rating exceeds the peak inductor current for the application. Calculate the worst-case peak inductor current as follows:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times f_{SW} \times L}$$

where f_{SW} is the switching frequency.

Capacitor Selection

Bypass IN to AGND and PGND with a ceramic capacitor. Ceramic capacitors with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over wide temperature ranges. Place the capacitor as close as possible to the IC. The recommended minimum value for the input capacitor is 10µF; however, larger value capacitors can be used to reduce input ripple at the expense of size and higher cost.

The output capacitance required depends on the output current. A 10µF ceramic capacitor works well in most situations, but a 4.7µF ceramic capacitor is acceptable for lower load currents.

Compensation Network Selection

The step-up converter is compensated for stability through an external compensation network from COMP to AGND. See Table 20 for recommended compensation networks.

PCB Layout

Due to fast-switching waveforms and high-current paths, careful PCB layout is required. Connect AGND, FGND, and PGND directly to the ground plane. The IN bypass capacitor should be placed as close as possible to the IC. R_{COMP} and C_{COMP} should be connected between COMP and AGND as close as possible to the IC. Minimize trace lengths between the IC and the inductor, the input capacitor, and the output capacitor; keep these traces short, direct, and wide. The ground connections of C_{IN} and C_{OUT} should be as close together as possible and connected to PGND. The traces from the input to the inductor and from the output capacitor to the LEDs may be longer. Figure 21 illustrates an example PCB layout and routing scheme. Refer to the MAX8834Y/MAX8834Z Evaluation Kit for a PCB layout example.

Table 19. Suggested Inductors

MANUFACTURER	PART/SERIES	INDUCTANCE (µH)	DCR (mΩ)	ISAT (A)	DIMENSIONS (I_{TYP} x W_{TYP} x H_{MAX}) (mm)
Coilcraft	LPS4012-222ML	2.2	100	2.3	4 x 4 x 1.1
	LPS4018-222ML	2.2	70	2.7	4 x 4 x 1.7
	LPS5030-220ML	2.2	57	3.1	5 x 5 x 2.9
	LPS6225-222ML	2.2	45	3.9	6.2 x 6.2 x 2.5
	LPO3310-102ML	1	76	1.6	3 x 3 x 1
	LPS3015-102ML	1	75	1.6	3 x 3 x 1
	LPO3010-102NLC	1	140	1.7	3 x 3 x 1
	DO3314-102ML	1	110	2.1	3 x 3 x 1.4
	LPS3314-102ML	1	45	2.3	3 x 3 x 1.4
	DP1605T-102ML	1	40	2.5	4 x 4 x 1.8
	LPS4012-102ML	1	60	2.8	4 x 4 x 1.1
	LPS4018-102ML	1	40	2.8	4 x 4 x 1.7
	LPS5015-102ML	1	50	3.8	5 x 5 x 1.5
Taiyo Yuden	NR4018T2R2M	2.2	72	2.7	4 x 4 x 1.8
	NR3012T1R0N	1	60	1.5	3 x 3 x 1.2
	NR4010T1R0N	1	120	1.8	4 x 4 x 1
	NR3015T1R0N	1	36	2.1	3 x 3 x 1.5
	NR4012T1R0N	1	72	2.5	4 x 4 x 1.2
	NP03SB1R0M	1	27	2.6	4 x 4 x 1.8
	NP04SZB1R0N	1	30	4	5 x 5 x 2
	NR4018T1R0N	1	36	4	4 x 4 x 1.8
TOKO	1117AS-1R2N	1.2	65	1.2	3 x 3 x 1
	1098AS-1R2N	1.2	56	1.8	3 x 3 x 1.2
	A997AS-1R0N	1	40	1.8	4 x 4 x 1.8
	1072AS-1R0N	1	30	1.95	3 x 3 x 1.8
	1071AS-1R0N	1	40	2.1	3 x 3 x 1.5

Table 20. Suggested Compensation Networks

INDUCTANCE	R_{COMP} (kΩ)	C_{COMP} (pF)
1.0µH Inductor (dynamic loads)	5.5	2200
2.2µH Inductor (dynamic loads)	4.3	2200
4.7µH Inductor (dynamic loads)	3	4700
10µH Inductor (dynamic loads)	3	6800
Other (non-LED) Loads (1µH to 10µH)	0 (short)	22000

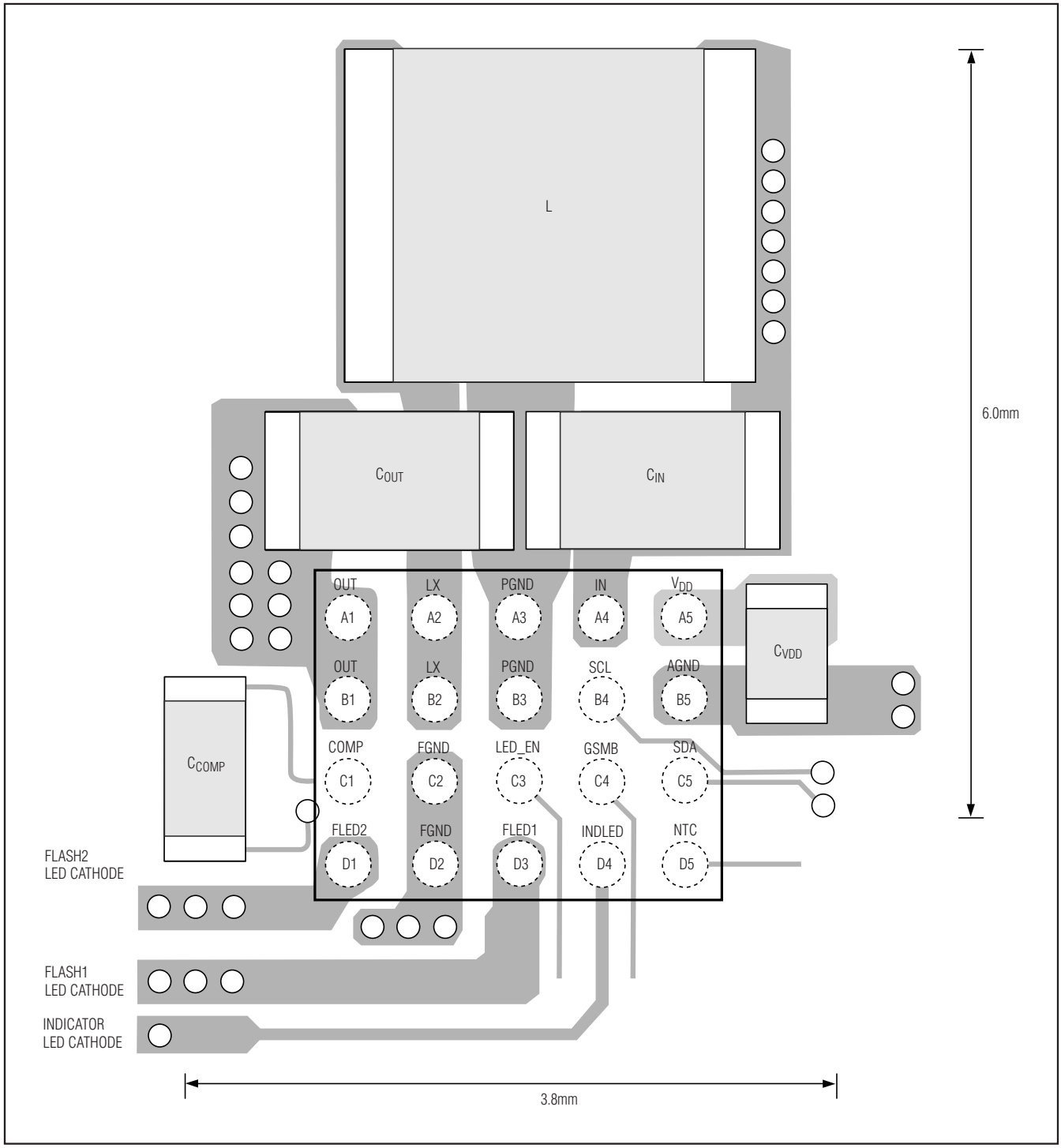
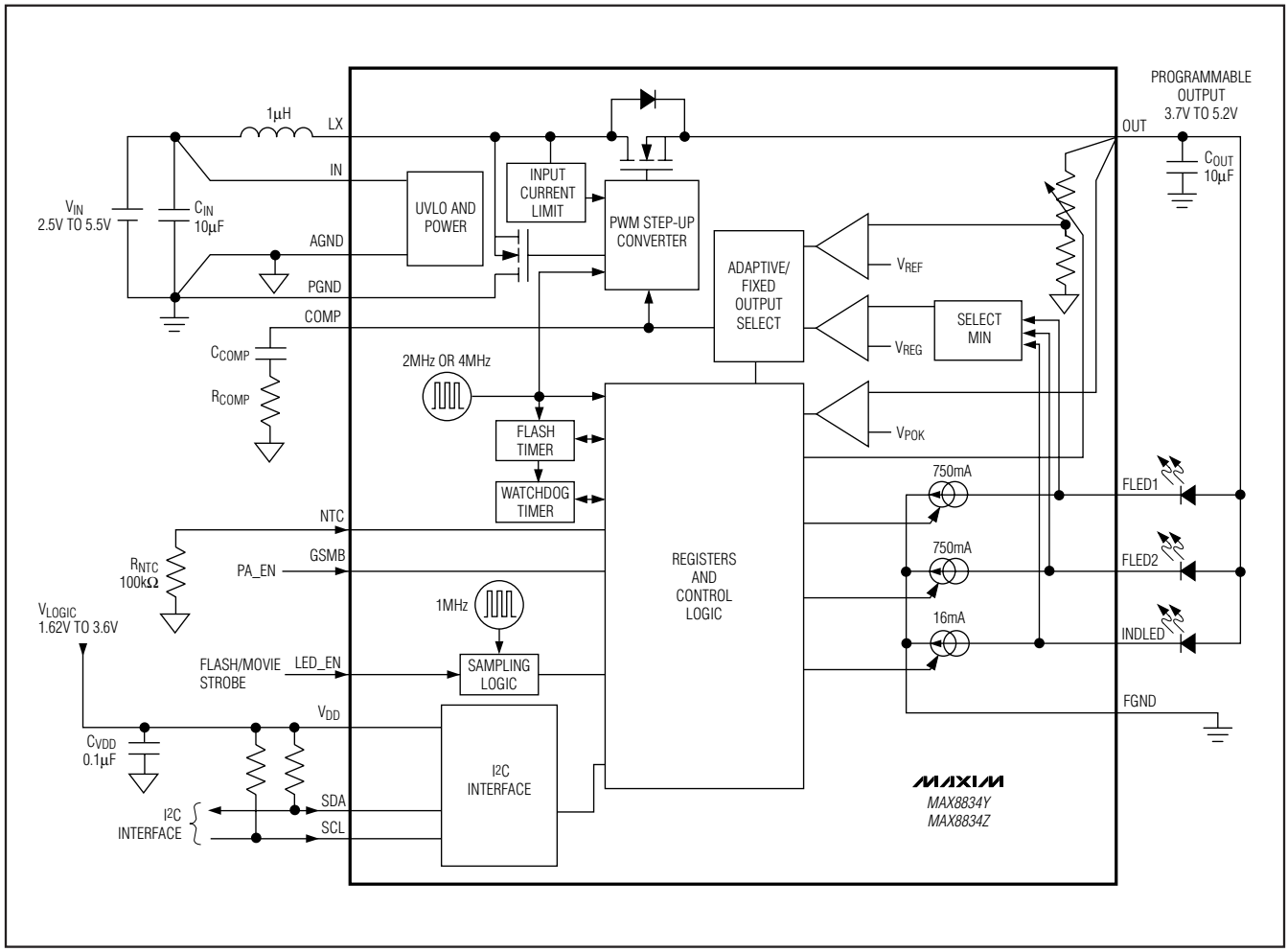


Figure 21. Recommended PCB Layout

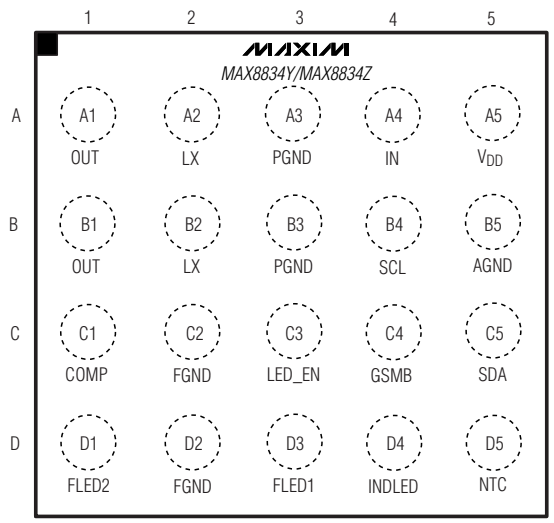
Adaptive Step-Up Converters with 1.5A Flash Driver

Block Diagram and Typical Application Circuit



Adaptive Step-Up Converters with 1.5A Flash Driver

Pin Configuration



WLP
(2.5mm × 2.0mm)

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 WLP	W202A2+2	**21-0059**