TAIWAN SEMICONDUCTOR

Pb RoHS COMPLIANCE

Preliminary   **TSM2N70**

700V N-Channel Power MOSFET

TO-251 (IPAK)   **TO-252 (DPAK)**

1 2 3   1 2 3

Pin Definition:
1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(Ω)	I_D (A)
700	7 @ V_{GS} =10V	0.8

General Description

The TSM2N70 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.
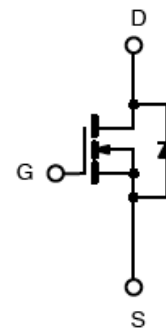
Features

- Low $R_{DS(ON)}$ 7Ω (Max.)
- Low gate charge typical @ 11.4nC (Typ.)
- Low Crss typical @ 6.5pF (Typ.)
- Fast Switching

Block Diagram

N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2N70CH C5	TO-252	70pcs / Tube
TSM2N70CP RO	TO-251	2.5Kpcs / 13" Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	1.6	A
Pulsed Drain Current *	I_{DM}	6.4	A
Avalanche Current (Single) (Note 2)	I_{AS}	1.6	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	110	mJ
Maximum Power Dissipation @TC = 25°C	P_D	45	W
Peak Diode Recovery Voltage Slope (Note 2)	dv/dt	4.5	V/ns
Operating Junction Temperature	T_J	150	^{o}C
Storage Temperature Range	T_{STG}	-55 to +150	^{o}C

* Limited by maximum junction temperature

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Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R\Theta_{JC}$	2.78	$^{o}C/W$
Thermal Resistance - Junction to Ambient	$R\Theta_{JA}$	100	$^{o}C/W$

Notes: Surface mounted on FR4 board t ≤ 10sec

Electrical Specifications (Ta = 25°C unless otherwise noted)

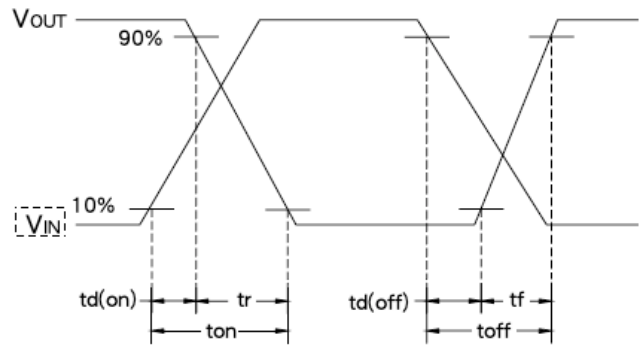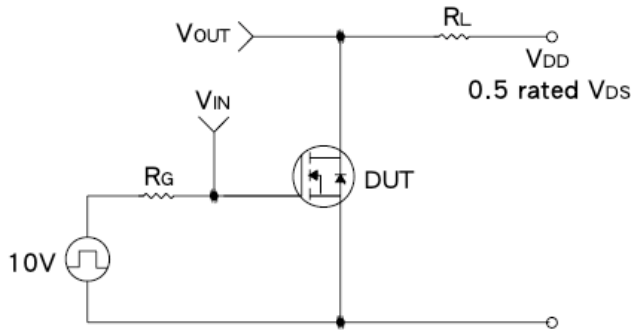| Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	700	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 0.8A	$R_{DS(ON)}$	--	6	7	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50uA	$V_{GS(TH)}$	3.0	--	4.5	V
Zero Gate Voltage Drain Current	V_{DS} = 700V, V_{GS} = 0V	I_{DSS}	--	--	1	uA
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±10	nA
Forward Transconductance	V_{DS} = 15V, I_D = 0.8A	g_{fs}	--	1.4	--	S
Diode Forward Voltage	I_S = 1.6A, V_{GS} = 0V	V_{SD}	--	1.6	--	V
Dynamic [b]						
Total Gate Charge	V_{DS} = 560V, I_D = 0.8A, V_{GS} = 10V	Q_g	--	11.4	--	nC
Gate-Source Charge		Q_{gs}	--	2	--	
Gate-Drain Charge		Q_{gd}	--	6.8	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	280	--	pF
Output Capacitance		C_{oss}	--	35	--	
Reverse Transfer Capacitance		C_{rss}	--	6.5	--	
Switching [c]						
Turn-On Delay Time	V_{GS} = 10V, I_D = 0.8A, V_{DD} = 350V, R_G = 4.7Ω	$t_{d(on)}$	--	7	--	nS
Turn-On Rise Time		t_r	--	17	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20	--	
Turn-Off Fall Time		t_f	--	35	--	
Reverse Recovery Time	V_{GS} = 0V, I_S = 13A, V_{DD} = 50V dI$_F$/dt = 100A/us	t_{fr}	--	334	--	nS
Reverse Recovery Charge		Q_{fr}	--	918	--	uC
Reverse Recovery Current		I_{RRM}	--	5.5	--	A

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. V_{DD} = 50V, I_{AS}=13A, L=8mH, R_G=25Ω
3. Pulse test: pulse width ≤300uS, duty cycle ≤1.5%
4. Essentially Independent of Operating Temperature
5. For design reference only, not subject to production testing.
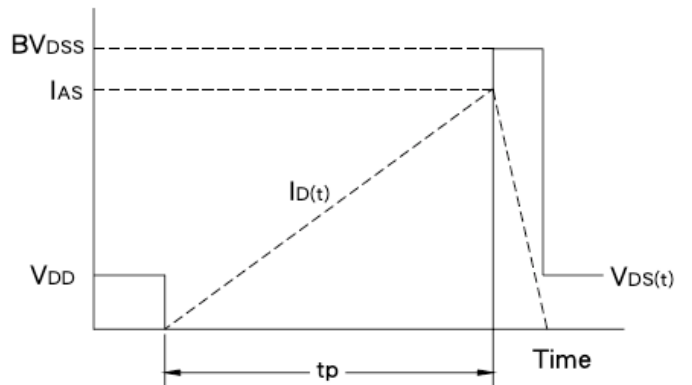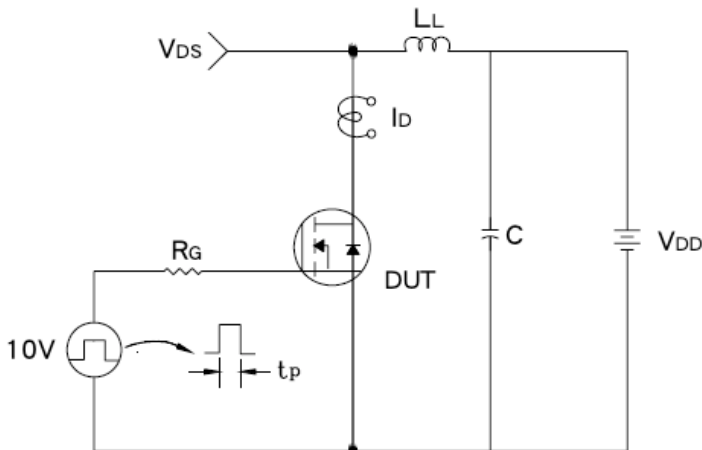6. Switching time is essentially independent of operating temperature.
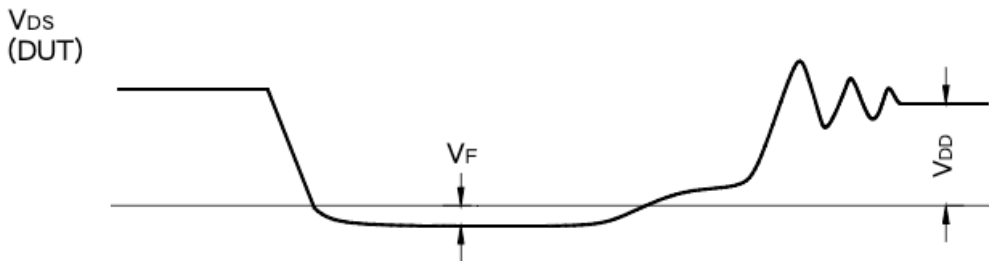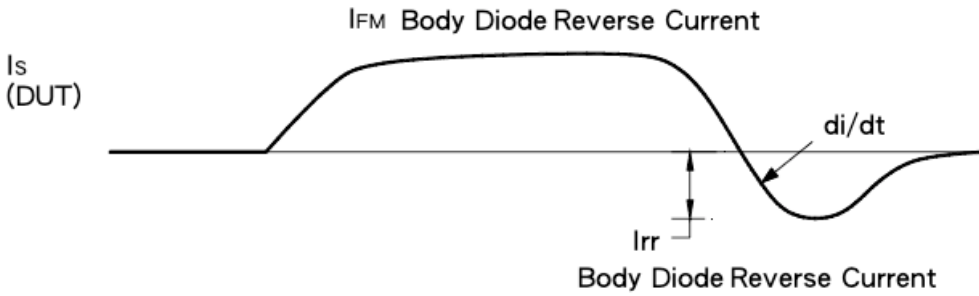
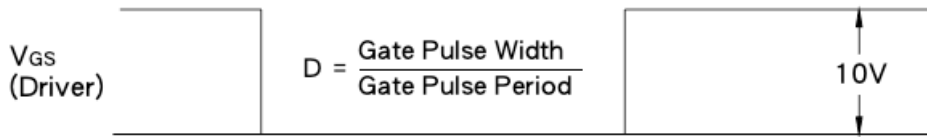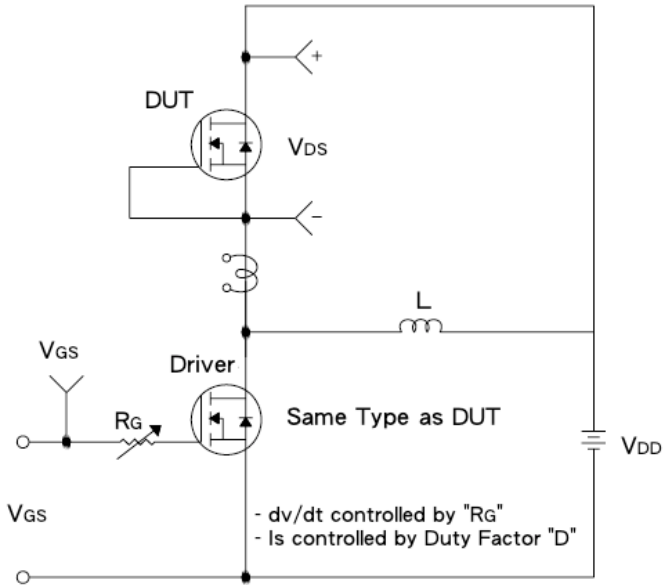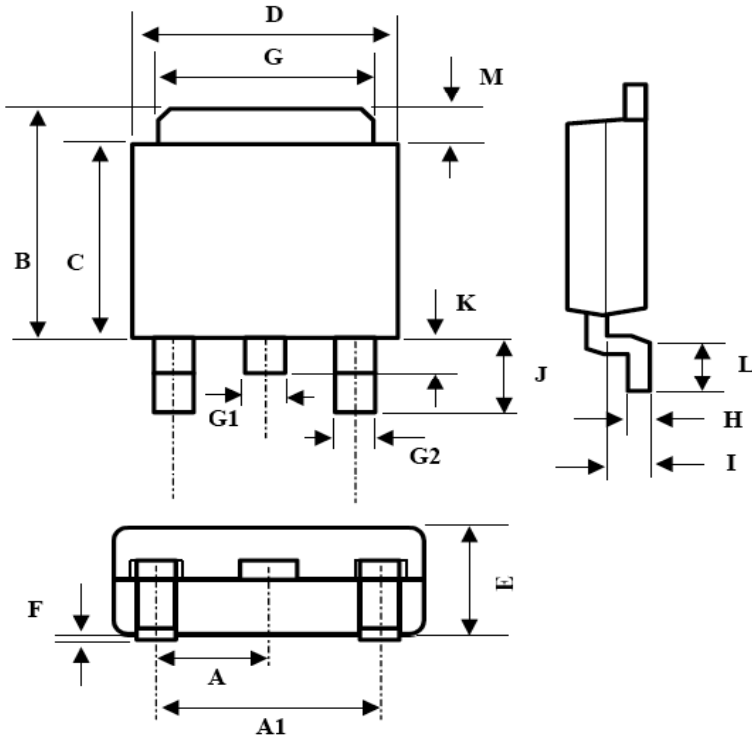## Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveform

E_{AS} Test Circuit & Waveform
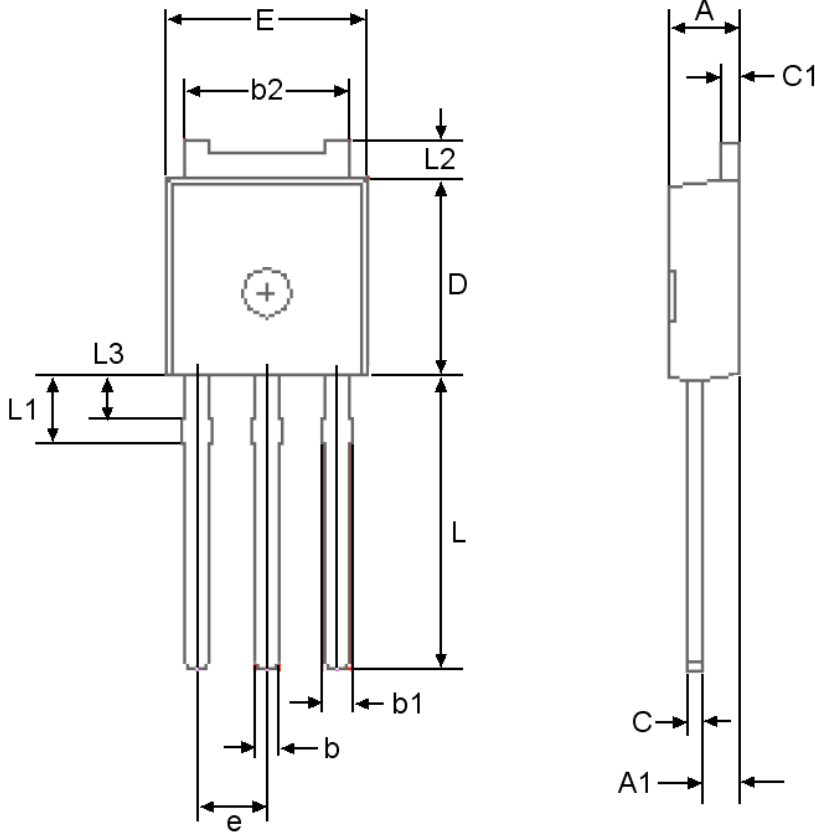
Diode Reverse Recovery Time Test Circuit & Waveform

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

- dv/dt controlled by "RG"
- Is controlled by Duty Factor "D"

700V N-Channel Power MOSFET

SOT-252 Mechanical Drawing

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.3BSC		0.09BSC	
A1	4.6BSC		0.18BSC	
B	6.80	7.20	0.268	0.283
C	5.40	5.60	0.213	0.220
D	6.40	6.65	0.252	0.262
E	2.20	2.40	0.087	0.094
F	0.00	0.20	0.000	0.008
G	5.20	5.40	0.205	0.213
G1	0.75	0.85	0.030	0.033
G2	0.55	0.65	0.022	0.026
H	0.35	0.65	0.014	0.026
I	0.90	1.50	0.035	0.059
J	2.20	2.80	0.087	0.110
K	0.50	1.10	0.020	0.043
L	0.90	1.50	0.035	0.059
M	1.30	1.70	0.051	0.67

TO-252 DIMENSION

Version: Preliminary

700V N-Channel Power MOSFET

SOT-251 Mechanical Drawing

DIM	TO-251 DIMENSION			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.19	2.38	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.76	1.14	0.030	0.045
b2	5.21	5.46	0.205	0.215
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.10	0.235	0.240
E	6.35	6.73	0.250	0.265
e	2.28 BSC.		0.90 BSC.	
L	8.89	9.65	0.350	0.380
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060

Notice