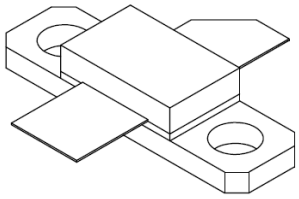
# 1011LD110B

## 110 Watts, 32 Volts
## Pulsed Avionics 1030 to 1090 MHz
## LDMOS FET

## GENERAL DESCRIPTION

The 1011LD110B is a COMMON SOURCE N-Channel enhancement mode lateral MOSFET capable of providing 110$W_{pk}$ of RF power from 1030MHz to 1090 MHz. The device is nitride passivated and utilizes gold metallization to ensure highest MTTF. The transistor includes input and output prematch for broadband capability. Low thermal resistance package reduces junction temperature, extends life. Integrated ESD protection makes the device robust.

**CASE OUTLINE**
**55QT**
**(Common Source)**



## ABSOLUTE MAXIMUM RATINGS

**Voltage and Current**

| | |
|---|---|
| Drain-Source ($V_{DSS}$) | +65V |
| Gate-Source ($V_{GS}$, $V_{DS}$=0) | +20V |

**Temperatures**

| | |
|---|---|
| Storage Temperature | -65 to +150°C |
| Operating Case Temperature[1] | +100°C |

**ELECTRICAL CHARACTERISTICS @ 25°C**

| SYMBOL | CHARACTERISTICS | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown | $V_{GS}$ = 0V, $I_D$ = 2mA | 65 | | | V |
| $I_{DSSF}$ | Drain-Source Leakage Current | $V_{DS}$ = 32V, $V_{GS}$ = 0V | | | 5 | µA |
| $I_{GSSF}$ | Gate-Source Leakage Current | $V_{GS}$ = 10V, $V_{DS}$ = 0V | | | 2 | µA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = 10V, $I_D$ = 3mA | 2 | | 4 | V |
| $V_{DS(ON)}$ | Drain-Source On Voltage | $V_{GS}$ = 10V, $I_D$ = 1A | | | 0.25 | V |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10V, $I_D$ = 1A | | 2.2 | | S |
| $\theta_{JC}$[1] | Thermal Resistance | | | | 0.12 | ºC/W |

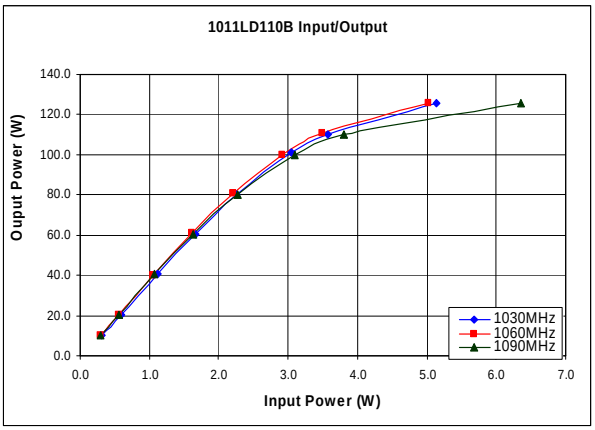
**FUNCTIONAL CHARACTERISTICS @ 25°C, Vds = 32V, $I_{DQ}$ = 250mA**

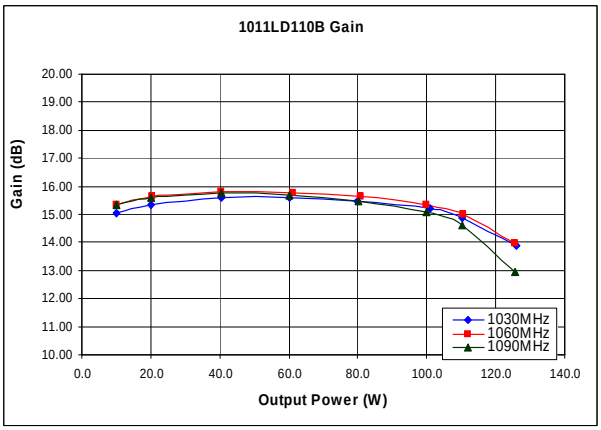
| | | | | | | |
|---|---|---|---|---|---|---|
| $G_{PS}$ | Common Source Power Gain | Pulse width = 32µs, LTDC=2%, | 13.5 | 14.5 | | dB |
| Pd | Pulse Droop | F=1030/1090 MHz, $P_{out}$ = 110W | | | 0.5 | dB |
| $P_{1dB}$ | Output Power at 1dB Gain Compression | Pulse width = 32µs, LTDC=2%, F=1030/1090 MHz | | 110 | | W |
| $\eta_D$ | Drain Efficiency | F = 1030 MHz, $P_{out}$ = 110W | 45 | 50 | | % |
| ψ | Load Mismatch | F = 1090 MHz, $P_{out}$ = 110W | | | 5:1 | |

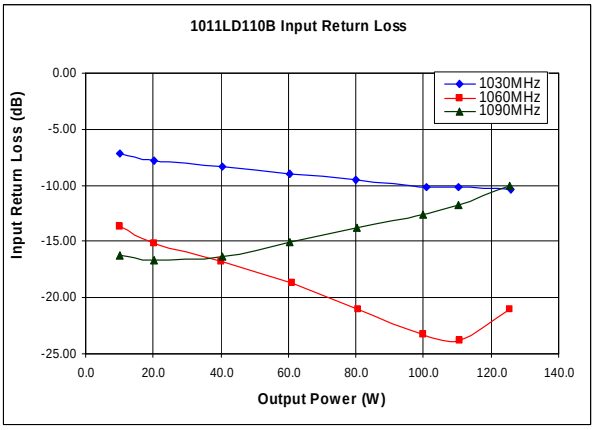
NOTES: 1. At rated output power and pulse conditions
2. Pulse Format 1: 32µs, 2% Long Term Duty Factor
3. Pulsed Bias: $I_{DQ-PULSED}$ = 6.5mA (@ 42us ON, 1.6msec)

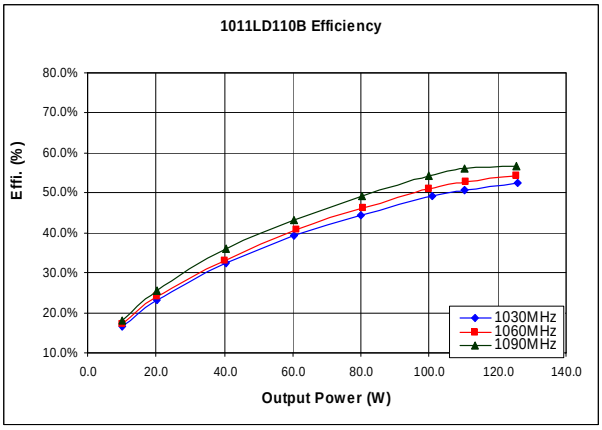
Rev. 0 – Apr. 2007

## Typical Performance (1030MHz ~ 1090MHz)

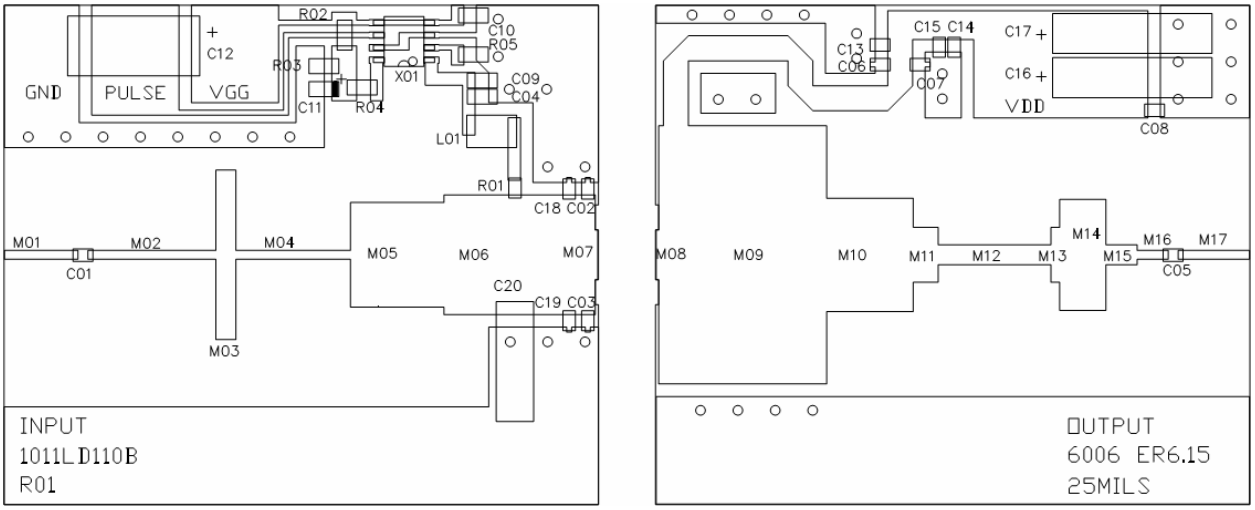


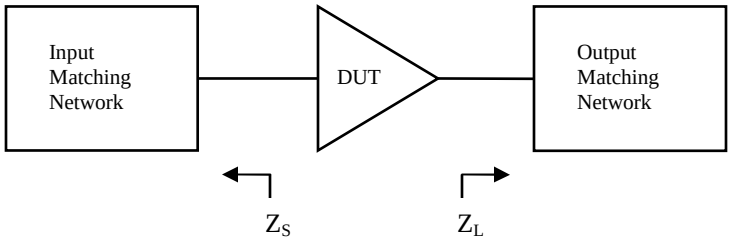
**1011LD110B Test Circuit Layout**




**1011LD110B Test Circuit Component Designations and Values**

| Part | Description | Part | Description |
|---|---|---|---|
| C01, C04, C05, C06 | 43pF Chip Capacitor (ATC 100A) | C10, C14, C15 | 0.033uF Chip Capacitor |
| C07, C08 | 100pF Chip Capacitor (ATC 100A) | C11 | 1uF 16V Tantalum Capacitor |
| C02, C03 | 7.5pF Chip Capacitor (ATC 100A) | C12 | 47uF 63V Electrolytic Capacitor |
| C18, C19 | 4.7pF Chip Capacitor (ATC 100A) | C16 | 470uF, 63V Electrolytic Capacitor |
| C20 | .35-3.5pF Johanson Capacitor, JMC5801 | C17 | 1000uF, 63V Electrolytic Capacitor |
| C09, C13 | 1000pF Chip Capacitor | L01 | 6 Turns, 24 AWG, IDIA 0.092″ |
| X01 | ADG419, Analog Device | R01, R04 | 15Ω, 1/4W Chip Resistor |
| R02, R03 | 200Ω, 1/4W Chip Resistor | R05 | 82.5Ω, 1/4W Chip Resistor |
| M01 | 36 x 295 mils (W x L) | M02 | 36 x 513 mils (W x L) |
| M03 | 680 x 80 mils (W x L) | M04 | 36 x 460 mils (W x L) |
| M05 | 420 x 375 mils (W x L) | M06 | 480 x 608 mils (W x L) |
| M07 | 200 x 10 mils (W x L) | M08 | 200 x 10 mils (W x L) |
| M09 | 1034 x 674 mils (W x L) | M10 | 454 x 348 mils (W x L) |
| M11 | 220 x 100 mils (W x L) | M12 | 80 x 452 mils (W x L) |
| M13 | 220 x 35 mils (W x L) | M14 | 445 x 186 mils (W x L) |
| M15 | 80 x 125 mils (W x L) | M16 | 36 x 125 mils (W x L) |
| M17 | 36 x 286 mils (W x L) | PCB | Rogers RT6006, $\varepsilon_r$=6.15, 25mils, 1oz |

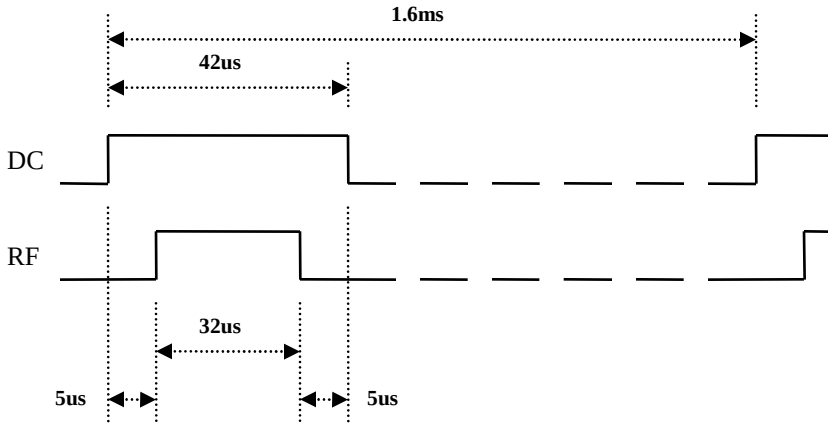
## Typical Impedance Values



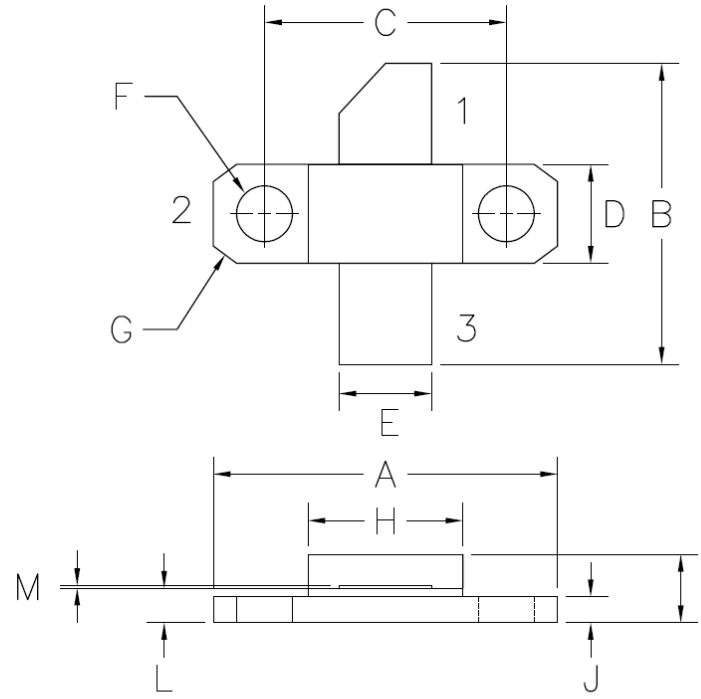

| Frequency (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) |
|---|---|---|
| **1030** | **0.88 - j1.21** | **1.95 - j1.59** |
| **1060** | **0.80 - j1.05** | **1.68 - j1.50** |
| **1090** | **0.73 - j0.88** | **1.43 - j1.34** |

* $V_{DS}$ = 32V, $I_{DQ}$ = 250mA, $P_{out}$ = 110W
* Pulse Format: 32µs, 2% Long Term Duty Factor

## Timing Diagram for Pulsed Bias

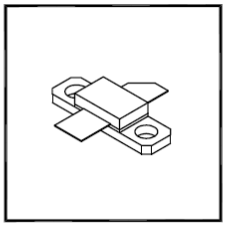


| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |




| DIM | MILLIMETER | ±TOL | INCHES | ±TOL |
|---|---|---|---|---|
| A | 25.40 | 1.3 | .800 | .050 |
| B | 17.78 | .13 | .700 | .005 |
| C | 14.27 | .13 | .562 | .005 |
| D | 5.84 | .13 | .230 | .005 |
| E | 5.46 | .13 | .215 | .005 |
| F | 3.30 Dia | .13 | .130 Dia | .005 |
| G | 45° | 5° | 45° | 5° |
| H | 9.14 | .13 | .360 | .005 |
| J | 1.52 | .13 | .060 | .005 |
| K | 3.51 | .13 | .138 | .005 |
| L | 2.03 | .13 | .080 | .005 |
| M | 0.10 | .02 | .004 | .001 |

**STYLE 1:**
**PIN 1 = DRAIN**
**2 = SOURCE**
**3 = GATE**



Microsemi
POWER PRODUCTS GROUP

| CAGE | DWG NO. | REV |
|---|---|---|
| 0PJR2 | 55QT | A |
| | SCALE 3/1 | SHEET |