BLA6H1011-600

LDMOS avionics power transistor

Rev. 01 — 22 April 2010 **Product data sheet**

1. Product profile

1.1 General description

600 W LDMOS pulsed power transistor intended for TCAS and IFF applications in the 1030 MHz to 1090 MHz range.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C; t_p = 50 µs; δ = 2 %; I_{Dq} = 100 mA; in a class-AB production test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	1030 to 1090	48	600	17	52	11	5

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

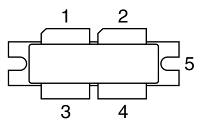
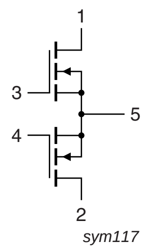
- Typical pulsed RF performance at a frequency of 1030 MHz to 1090 MHz, a supply voltage of 48 V, an I_{Dq} of 100 mA, a t_p of 50 µs with δ of 2 %:
  - Output power = 600 W
  - Power gain = 17 dB
  - Efficiency = 52 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- 600 W LDMOS pulsed power transistor intended for TCAS and IFF applications in the 1030 MHz to 1090 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA6H1011-600	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		0.5	13	V
I_D	drain current		-	72	A
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-case)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 600 W		
		t_p = 100 μs; δ = 10 %	0.06	K/W
		t_p = 50 μs; δ = 2 %	0.035	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.25	1.8	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	32	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 270 mA	1.6	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.5 A	-	100	169	mΩ

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 50 μs; δ = 2 %; RF performance at V_{DS} = 48 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		600	-	-	W
V_{DS}	drain-source voltage	P_L = 600 W	-	-	48	V
G_p	power gain	P_L = 600 W	16	17	-	dB
RL_{in}	input return loss	P_L = 600 W	8	12	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	700	-	W
η_D	drain efficiency	P_L = 600 W	47	52	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 600 W	-	0	0.3	dB
t_r	rise time	P_L = 600 W	-	11	30	ns
t_f	fall time	P_L = 600 W	-	5	30	ns

6.1 Ruggedness in class-AB operation

The BLA6H1011-600 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 48 V; I_{Dq} = 100 mA; P_L = 600 W; t_p = 50 μs; δ = 2 %; f = 1030 MHz.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
1030	1.702 – j1.816	0.977 + j0.049
1060	1.815 – j1.760	1.033 + j0.221
1090	1.912 – j1.751	1.086 + j0.379

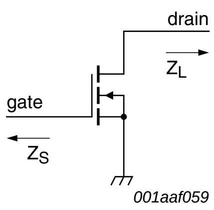
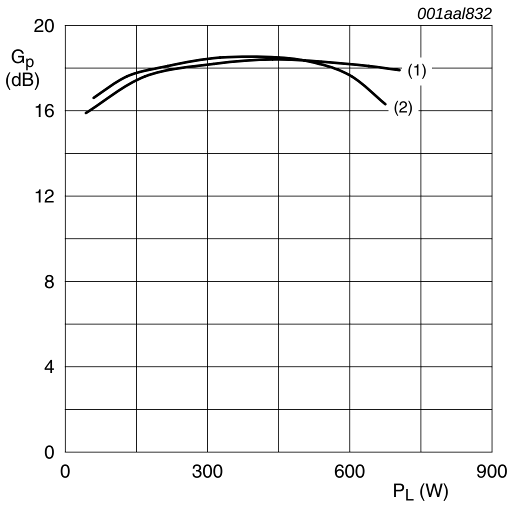


Fig 1. Definition of transistor impedance

7.2 Performance curves

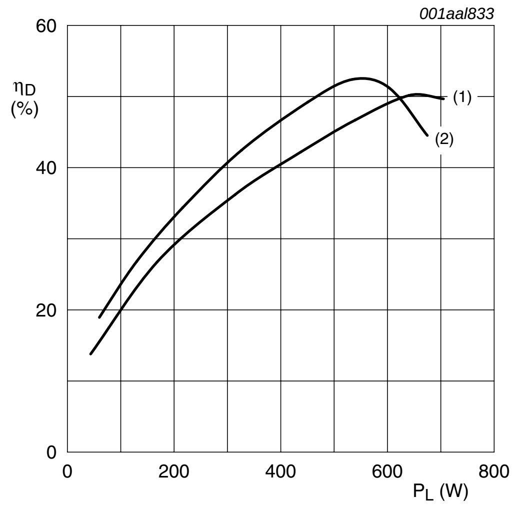


T_h = 25 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 µs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1090 MHz

Fig 2. Power gain as a function of load power; typical values

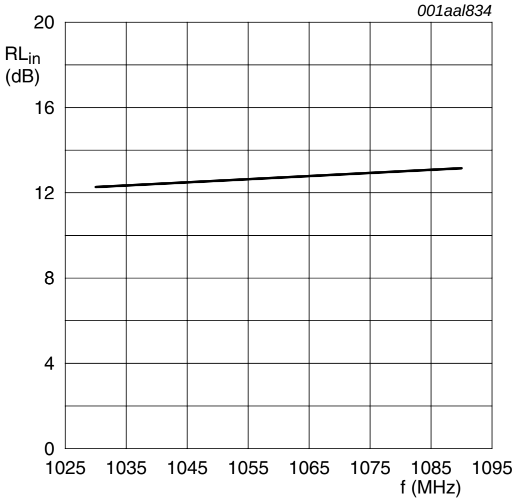


T_h = 25 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 µs; δ = 2 %.

(1) f = 1030 MHz

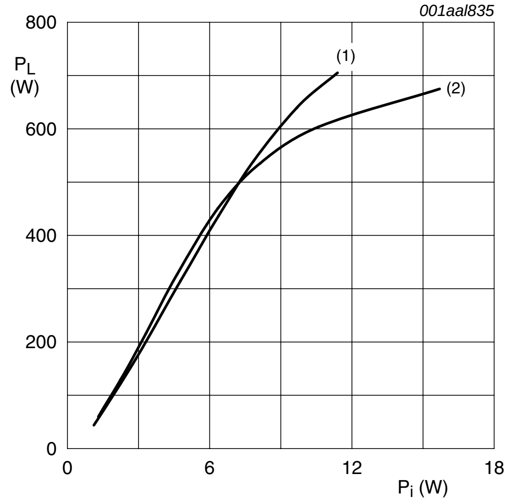
(2) f = 1090 MHz

Fig 3. Drain efficiency as a function of load power; typical values



T_h = 25 °C; P_L = 600 W; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

Fig 4. Input return loss as a function of frequency; typical values

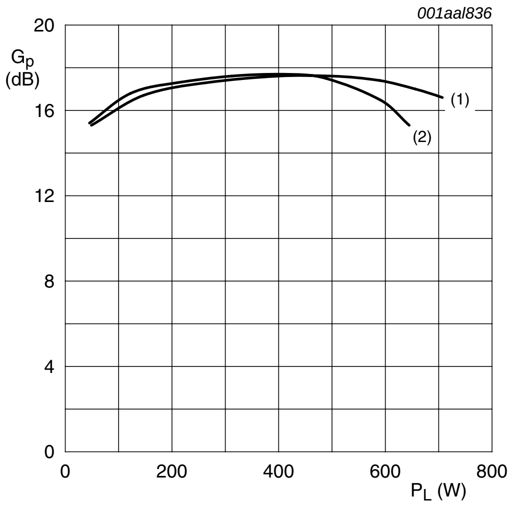


T_h = 25 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1090 MHz

Fig 5. Load power as a function of input power; typical values

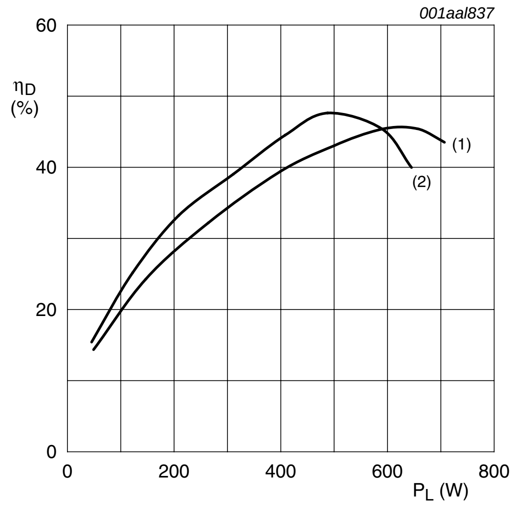


T_h = 65 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1090 MHz

Fig 6. Power gain as a function of load power; typical values

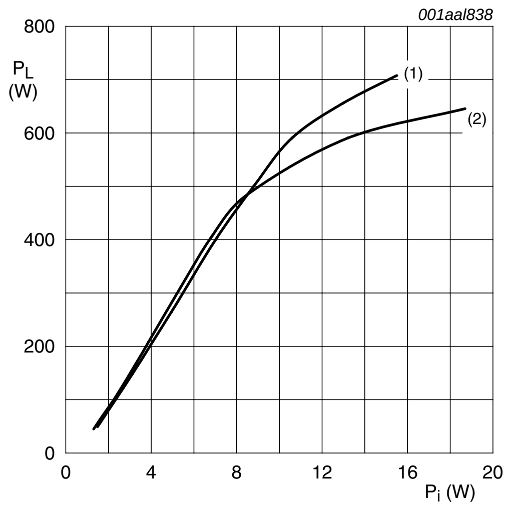


T_h = 65 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 μs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1090 MHz

Fig 7. Drain efficiency as a function of load power; typical values



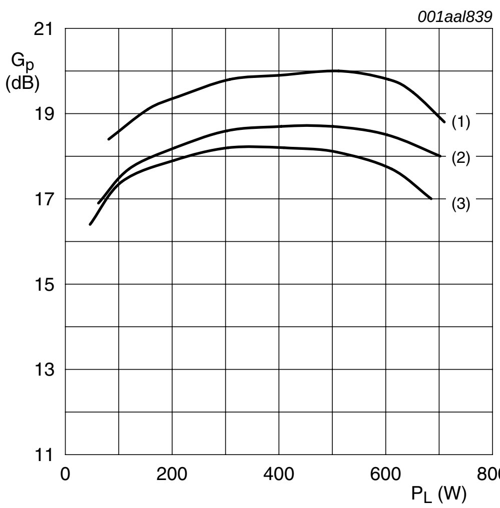
T_h = 65 °C; V_{DS} = 48 V; I_{Dq} = 100 mA; t_p = 50 µs; δ = 2 %.

(1) f = 1030 MHz

(2) f = 1090 MHz

Fig 8. Load power as a function of input power; typical values

7.3 Curves measured under Mode-S ELM pulse-conditions



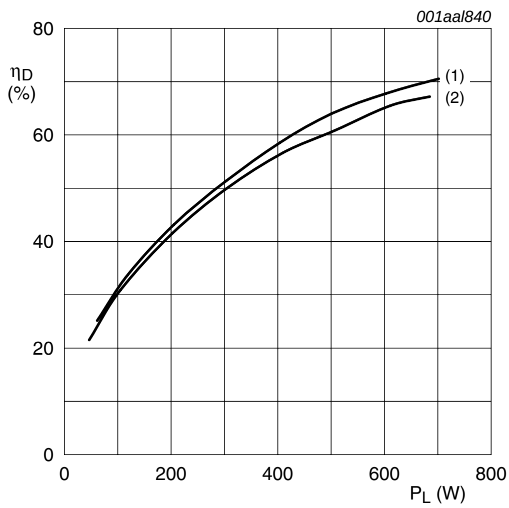
f = 1030 MHz; I_{Dq} = 100 mA.

(1) T_h = –40 °C

(2) T_h = +25 °C

(3) T_h = +65 °C

Fig 9. Power gain as a function of load power; typical values

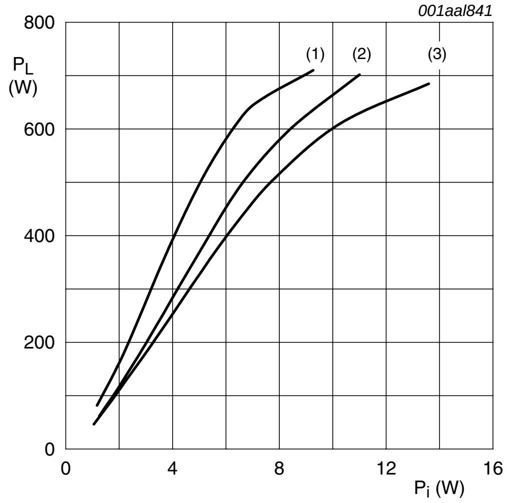


f = 1030 MHz; I_{Dq} = 100 mA.

(1) T_h = 25 °C

(2) T_h = 65 °C

Fig 10. Drain efficiency as a function of load power; typical values



f = 1030 MHz; I_{Dq} = 100 mA.

(1) T_h = −40 °C

(2) T_h = +25 °C

(3) T_h = +65 °C

Fig 11. Load power as a function of input power; typical values

8. Test information

Table 9. List of components

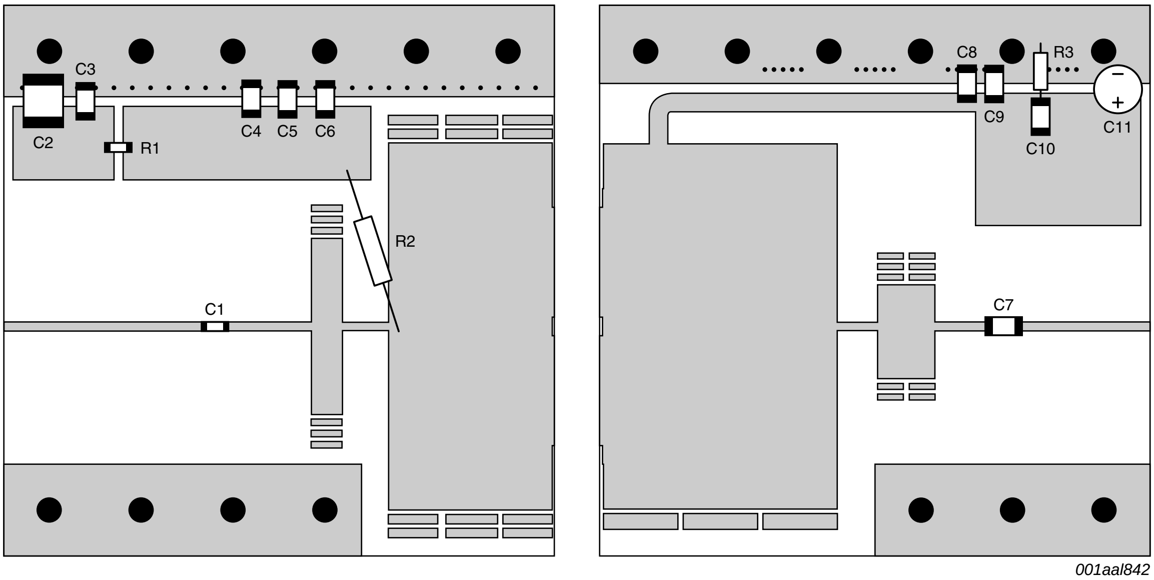
For test circuit see Figure 12.

Component	Description	Value		Remarks
C1, C4, C7	multilayer ceramic chip capacitor	82 pF	[1]	
C2	multilayer ceramic chip capacitor	22 μF; 35 V		
C3, C5, C8	multilayer ceramic chip capacitor	39 pF	[2]	
C6, C9	multilayer ceramic chip capacitor	1 nF	[2]	
C10	multilayer ceramic chip capacitor	20 nF	[3]	
C11	electrolytic capacitor	47 μF; 63 V		
R1	SMD resistor	56 Ω		0603
R2	metal film resistor	51 Ω		
R3	resistor	11 Ω		

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 200B or capacitor of same quality.



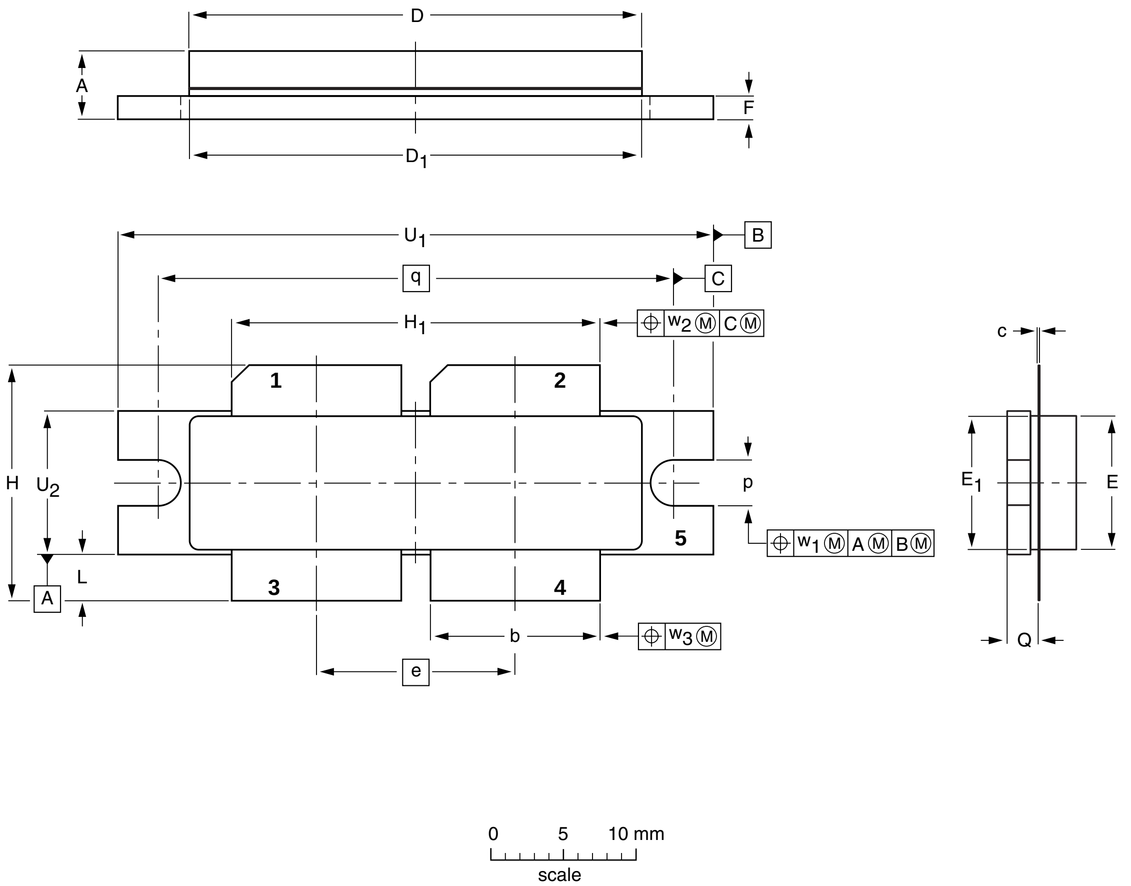
Printed-Circuit Board (PCB): Duroid 6006; ε_r = 6.15 F/m; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 12. Component layout for class-AB production test circuit

9. Package outline

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~00-03-03~~ 10-02-02

Fig 13. Package outline SOT539A

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
IFF	Identification Friend or Foe
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
TCAS	Traffic Collision Avoidance System
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6H1011-600_1	20100422	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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