

## 32-Mbit (2M x 16) Static RAM

### Features

- **Very high speed: 55 ns and 70 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Ultra-low active power**
  - Typical active current: 2 mA @ f = 1 MHz
  - Typical active current: 15 mA @ f = f<sub>max</sub>
- **Ultra low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

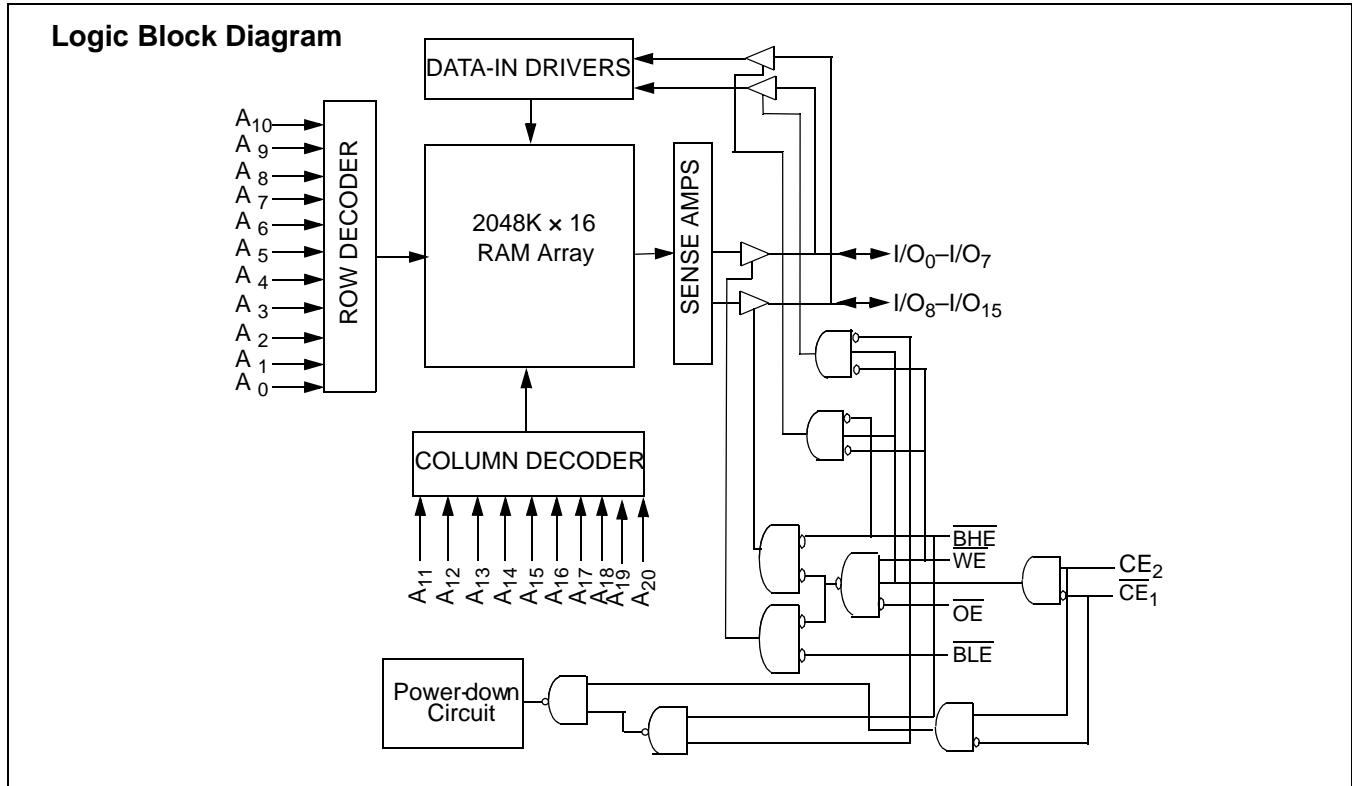
### Functional Description<sup>[1]</sup>

The CY62177DV30 is a high-performance CMOS static RAM organized as 2M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly

reduces power consumption. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW or both BHE and BLE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>).

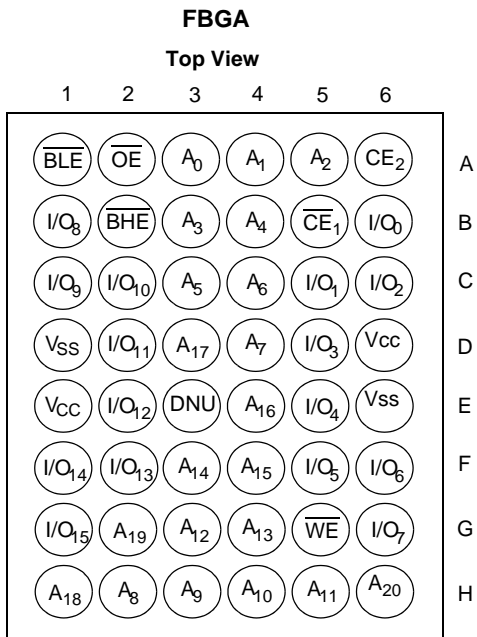
Reading from the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table for a complete description of read and write modes.



**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**



**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> ( $\mu$ A)	
	f = 1 MHz		f = f <sub>max</sub>		Typ. <sup>[3]</sup>	Max.				
	Min.	Typ. <sup>[3]</sup>	Max.				Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62177DV30L	2.20	3.0	3.60	55	2	4	15	30	5	60
				70			12	25		
CY62177DV30LL	2.20	3.0	3.60	55	2	4	15	30	5	50
				70			12	25		

**Notes:**

2. DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C  
 Ambient Temperature with Power Applied..... -55°C to + 125°C  
 Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC} + 0.3V$   
 DC Voltage Applied to Outputs in High Z State<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC} + 0.3V$   
 DC Input Voltage<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current .....>200 mA

### Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62177DV30L	Industrial	-40°C to +85°C	2.20V to 3.60V
CY62177DV30LL			

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62177DV30-55			CY62177DV30-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	Min.	Typ. <sup>[3]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$ , $V_{CC} = 2.20V$	2.0			2.0			V
		$I_{OH} = -1.0 \text{ mA}$ , $V_{CC} = 2.70V$	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$ , $V_{CC} = 2.20V$			0.4			0.4	V
		$I_{OL} = 2.1 \text{ mA}$ , $V_{CC} = 2.70V$			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$	1.8		$V_{CC} + 0.3V$	1.8		$V_{CC} + 0.3V$	V
		$V_{CC} = 2.7V \text{ to } 3.6V$	2.2		$V_{CC} + 0.3V$	2.2		$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 2.2V \text{ to } 2.7V$	-0.3		0.6	-0.3		0.6	V
		$V_{CC} = 2.7V \text{ to } 3.6V$	-0.3		0.8	-0.3		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-1		+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ , $V_{CC} = V_{CCmax}$ , $I_{OUT} = 0 \text{ mA}$ , CMOS levels		15	30		12	25	mA
		$f = 1 \text{ MHz}$		2	4		2	4	mA
$I_{SB1}$	Automatic CE Power-Down Current—CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$ , $CE_2 < 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ , $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE and BLE), $V_{CC} = 3.60V$	L	5	100		5	100	$\mu\text{A}$
			LL	5	100		5	100	
$I_{SB2}$	Automatic CE Power-Down Current—CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$ , $CE_2 < 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = 3.60V$	L	5	60		5	60	$\mu\text{A}$
			LL	5	50		5	50	

**Notes:**

- $V_{IL(min.)} = -2.0V$  for pulse durations less than 20 ns.
- $V_{IH(Max)} = V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- Full Device AC operation requires linear  $V_{CC}$  ramp from 0 to  $V_{CC(min)} \geq 500 \mu\text{s}$ .

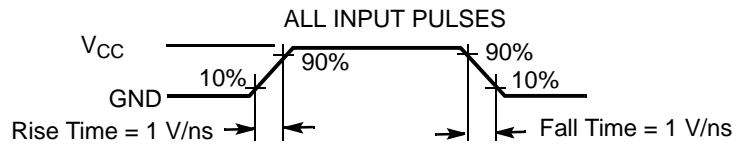
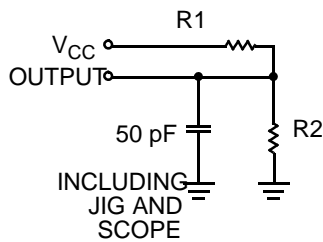
**Capacitance<sup>[7, 8]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	12	pF
C <sub>OUT</sub>	Output Capacitance		12	pF

**Thermal Resistance<sup>[7]</sup>**

Parameter	Description	Test Conditions	BGA	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		16	°C/W

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

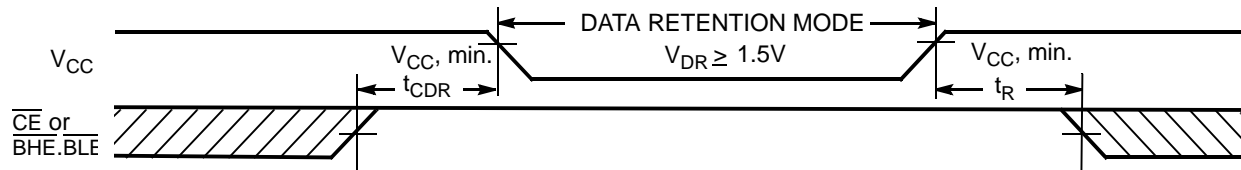
**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> < 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	L		30	μA
			LL		25	
t <sub>CDR</sub> <sup>[7]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Notes:**

7. Tested initially and after any design or process changes that may affect these parameters.
8. This applies for all packages.
9. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.

**Data Retention Waveform<sup>[10, 11]</sup>**



**Switching Characteristics Over the Operating Range<sup>[11, 12]</sup>**

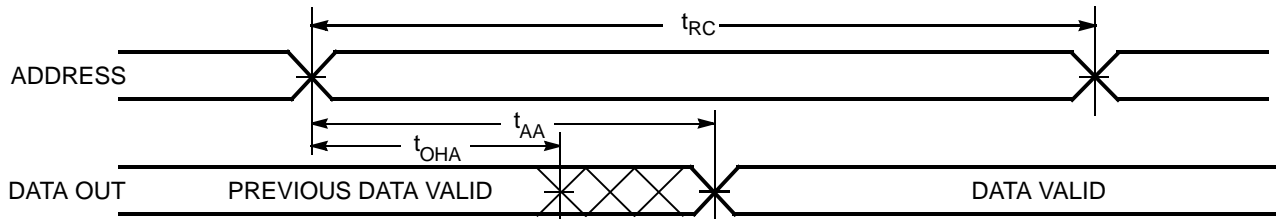
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to LOW Z <sup>[13]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[13, 14]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[13]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[13, 14]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW HIGH to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t <sub>DBE</sub>	BLE/BHE LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Low Z <sup>[13]</sup>	10		5		ns
t <sub>HZBE</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ HIGH to HIGH Z <sup>[13, 14]</sup>		20		25	ns
<b>WRITE CYCLE<sup>[15]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	40		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	40		45		ns
t <sub>BW</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Write End	40		60		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High-Z <sup>[13, 14]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[13]</sup>	10		10		ns

**Notes:**

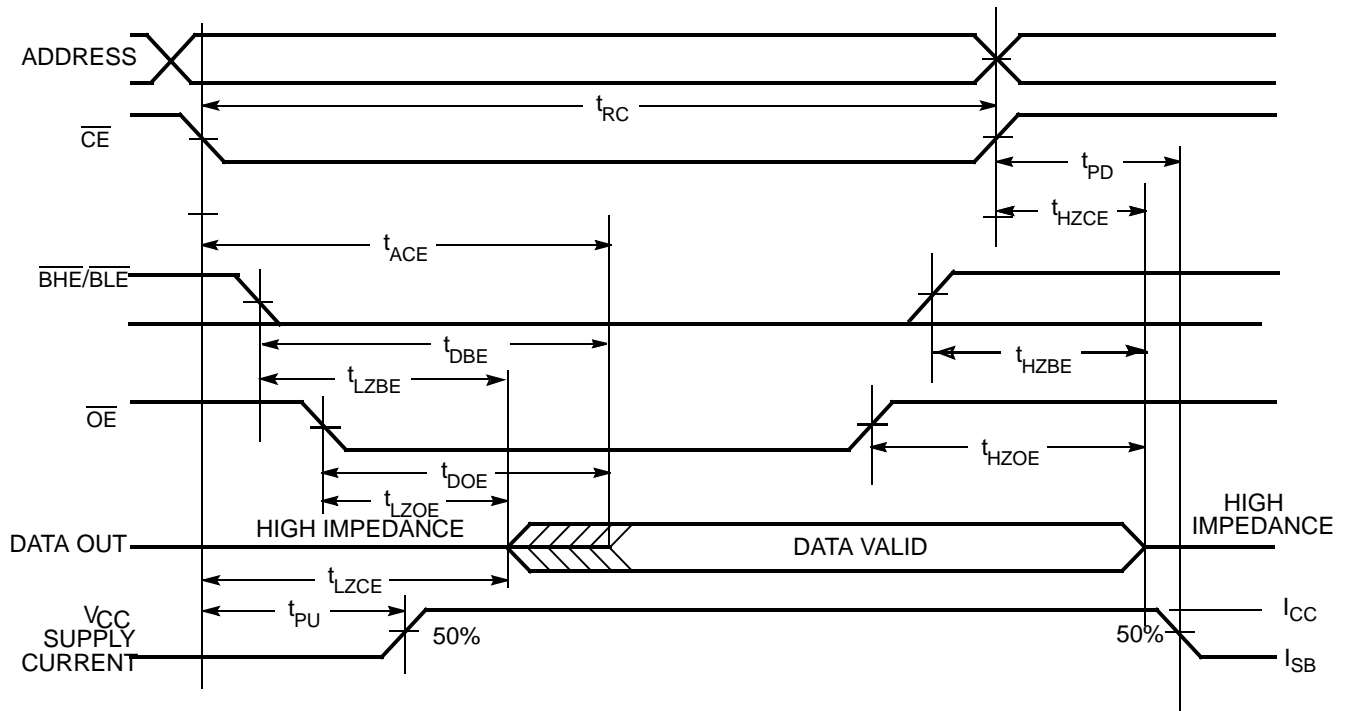
10.  $\overline{\text{BHE}}/\overline{\text{BLE}}$  is the AND of both  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$ . Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$ .
11.  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\overline{\text{CE}}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\overline{\text{CE}}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\overline{\text{CE}}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of  $V_{CC(\text{typ})}/2$ , input pulse levels of 0 to  $V_{CC(\text{typ})}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
15. The internal Write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

#### Read Cycle 1 (Address Transition Controlled)<sup>[16, 17]</sup>



#### Read Cycle 2 ( $\overline{\text{OE}}$ Controlled)<sup>[11, 17, 18]</sup>

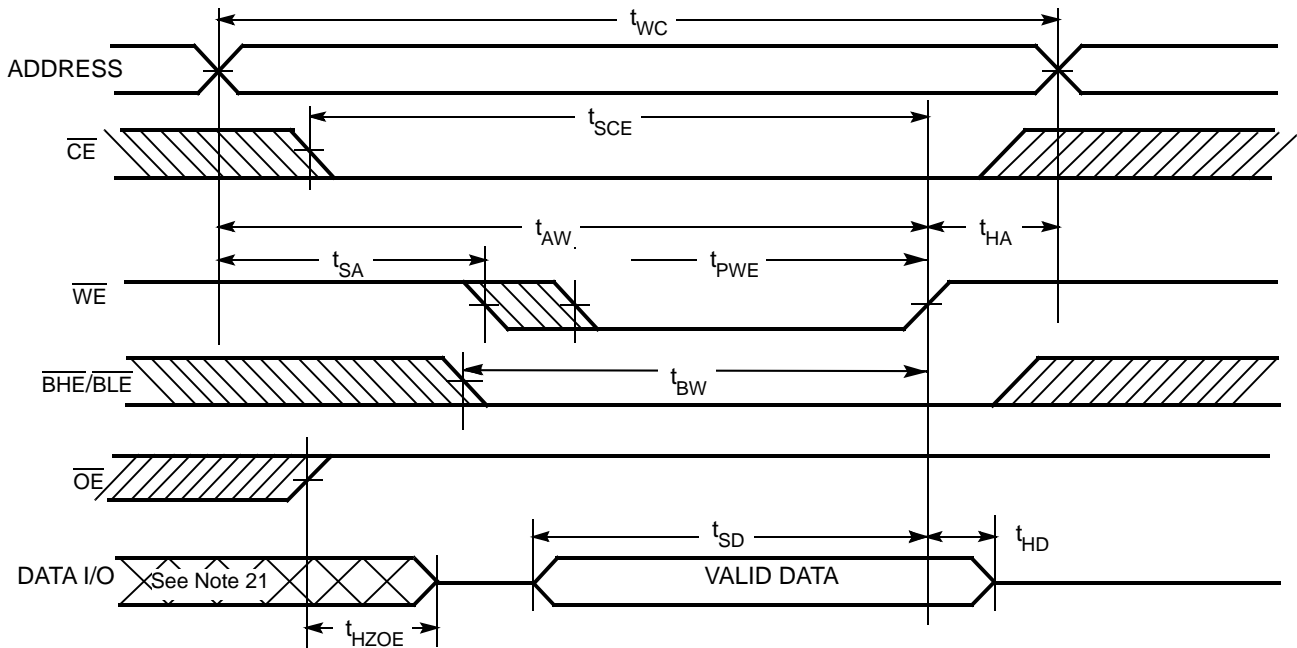


**Notes:**

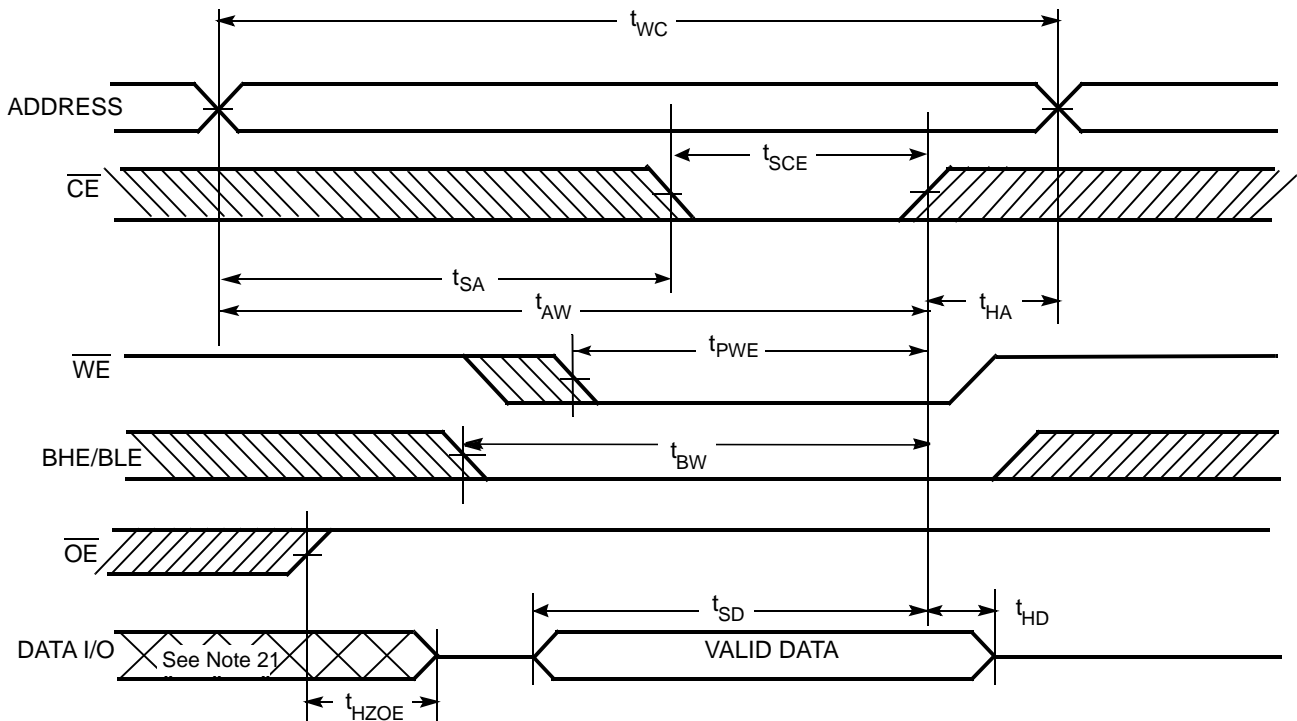
- 16. The device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}, \overline{\text{BHE}} \text{ and/or } \overline{\text{BLE}} = V_{\text{IL}}$ .
- 17.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 18. Address valid prior to or coincident with  $\overline{\text{CE}}, \overline{\text{BHE}}, \overline{\text{BLE}}$  transition LOW.

**Switching Waveforms (continued)**

**Write Cycle 1 (WE Controlled)**<sup>[11, 15, 19, 20, 21]</sup>



**Write Cycle 2 (CE Controlled)**<sup>[11, 15, 19, 20, 21]</sup>

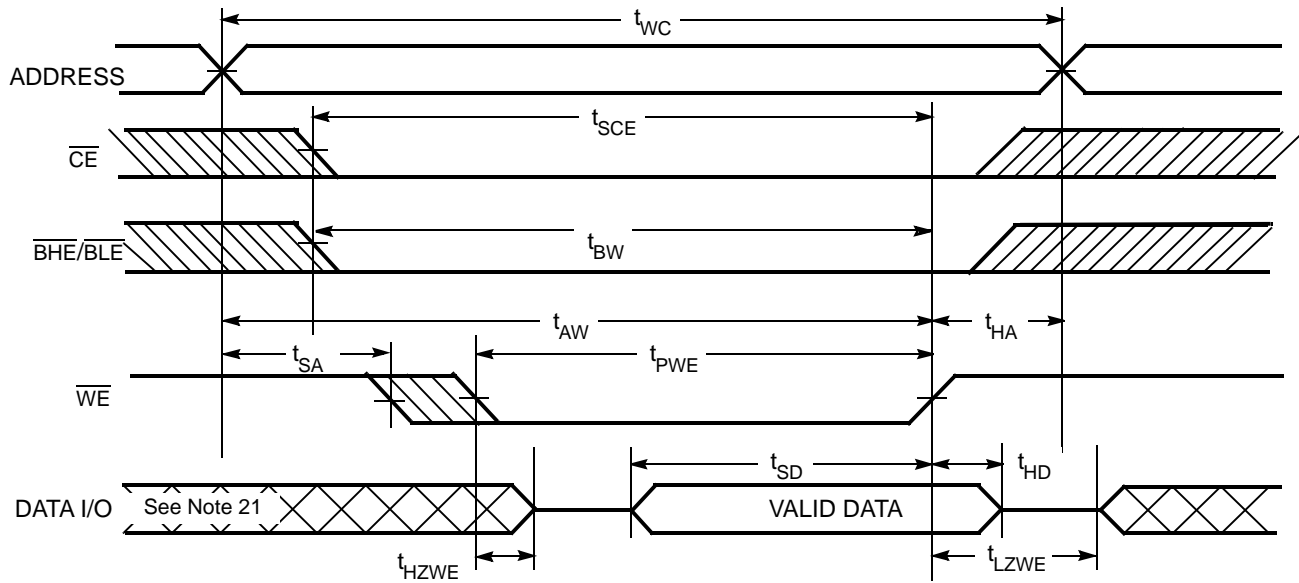


**Notes:**

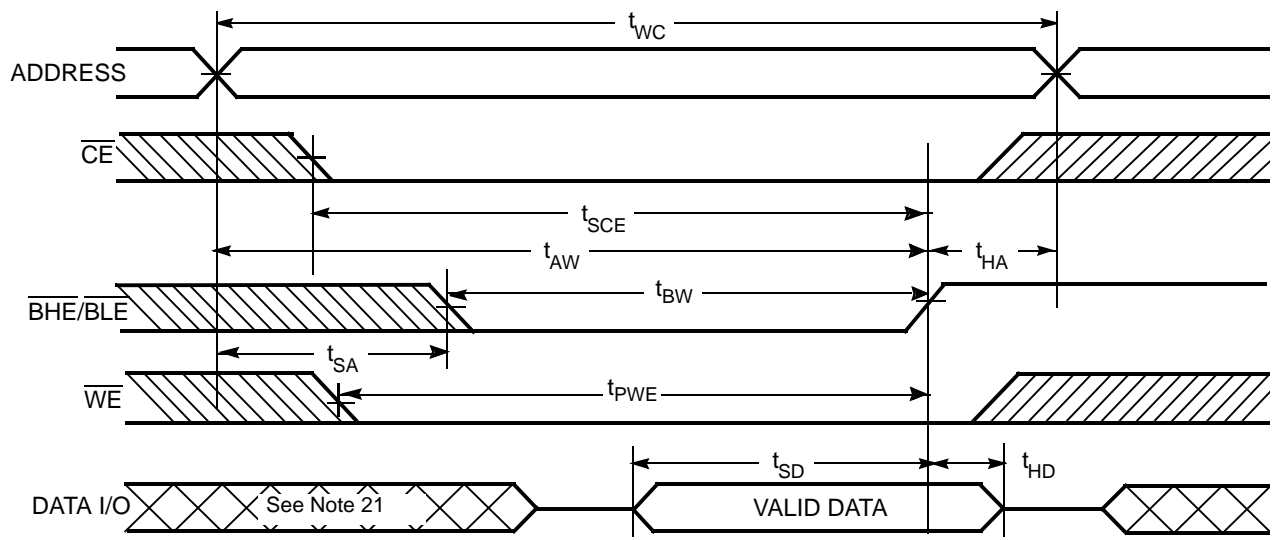
- 19. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 20. If CE goes HIGH simultaneously with  $WE = V_{IH}$ , the output remains in a high-impedance state.
- 21. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)<sup>[11, 20, 21]</sup>



Write Cycle 4 (BHE/BLE Controlled, OE LOW)<sup>[11, 20, 21]</sup>





**Truth Table**

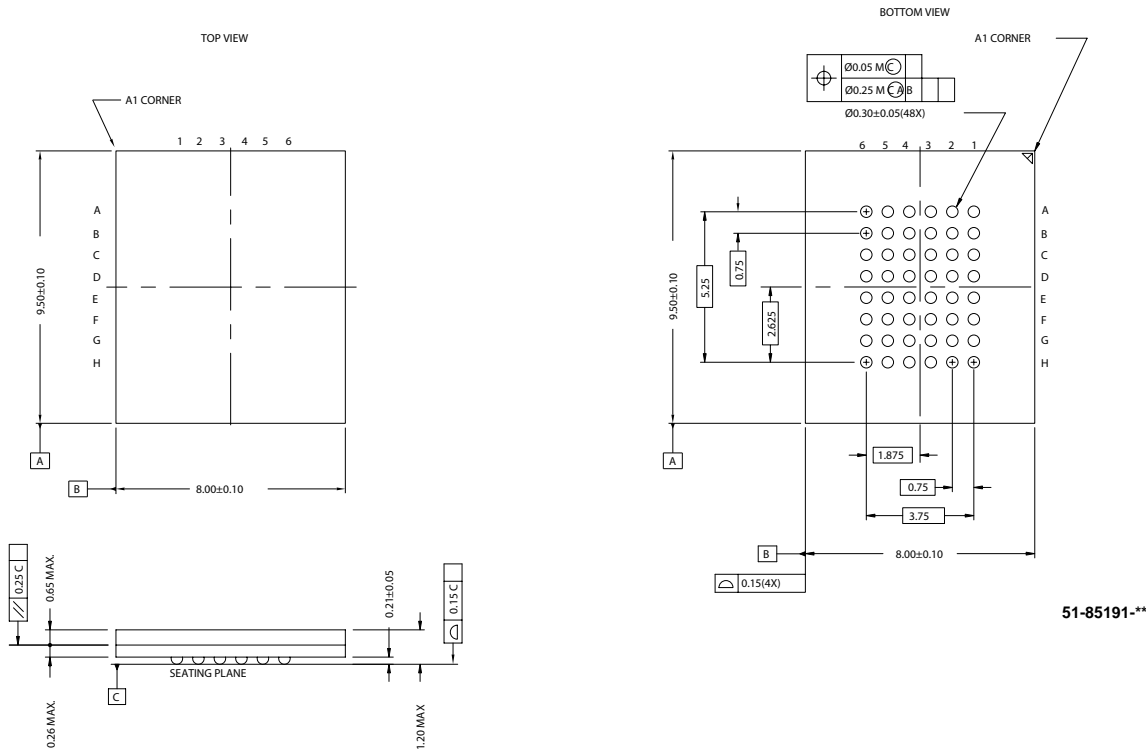
CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> ); High Z (I/O <sub>8</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	H	High Z (I/O <sub>0</sub> -I/O <sub>7</sub> ); Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O <sub>0</sub> -I/O <sub>7</sub> ); High Z (I/O <sub>8</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	H	L	X	L	H	High Z (I/O <sub>0</sub> -I/O <sub>7</sub> ); Data In (I/O <sub>8</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177DV30L-55BAI	51-85191	48-ball FBGA (8 mm × 9.5mm × 1.2 mm)	Industrial
	CY62177DV30LL-55BAI			
	CY62177DV30LL-55BAXI		48-ball FBGA (8 mm × 9.5mm × 1.2 mm) (Pb-free)	
70	CY62177DV30L-70BAI	51-85191	48-ball FBGA (8 mm × 9.5mm × 1.2 mm)	Industrial

**Package Diagram**

**48 FBGA (8 x 9.5 x 1.2 MM) (51-85191)**



51-85191-\*\*-

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**Document History Page**

Document Title: CY62177DV30 MoBL <sup>®</sup> 32-Mbit (2M x 16) Static RAM Document #: 38-05633				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	251075	See ECN	AJU	New Data Sheet
*A	330363	See ECN	AJU	Changed title of data sheet from CYM62177DV30 to CY62177DV30 Added second chip enable (CE <sub>2</sub> ) Added footnote #12 on page 5
*B	400960	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed I <sub>SB1</sub> from 60 and 40 μA to 100 μA for the L and LL versions for both the 55 and the 70 ns speed bins respectively.
*C	469187	See ECN	NXR	Converted from Preliminary to Final Changed the I <sub>SB2(Max)</sub> from 40 μA to 50 μA for LL version of both 45 ns and 55 ns speed bins Changed the I <sub>CCDR(Max)</sub> from 20 μA to 25 μA for LL version Updated the Ordering Information table