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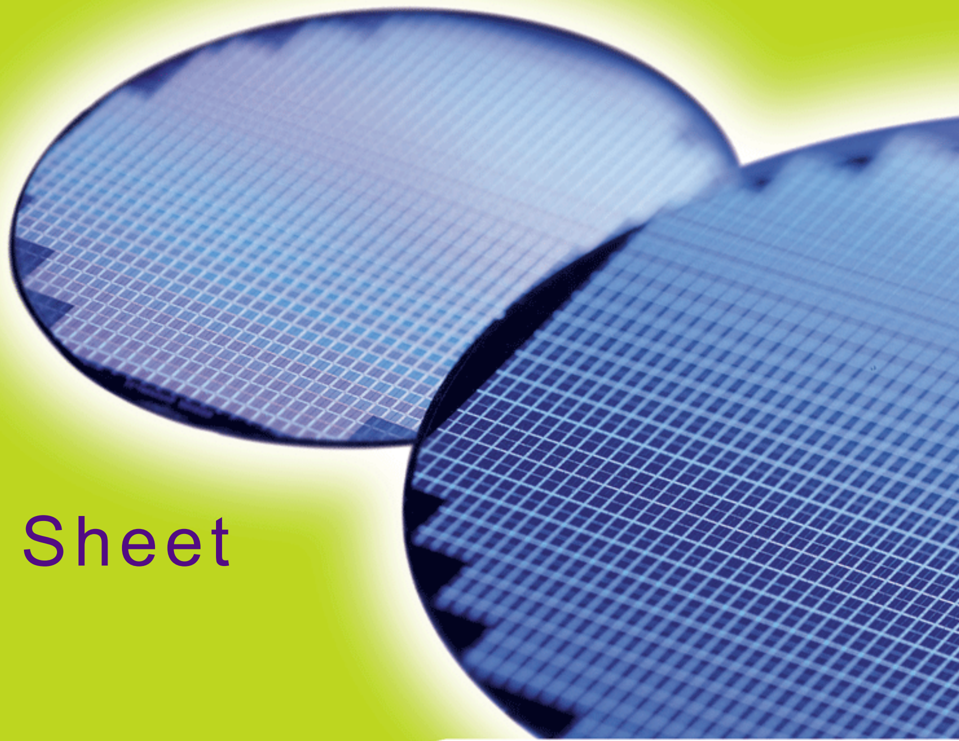
HYS72T64000HR–[3S/3.7/5]–B
HYS72T1280x0HR–[3S/3.7/5]–B
HYS72T256220HR–[3S/3.7/5]–B

240-Pin Registered DDR2 SDRAM Modules
RDIMM SDRAM
DDR2 SDRAM
RoHS Compliant



Internet Data Sheet

Rev. 1.2

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HYS72T64000HR–[3S/3.7/5]–B, HYS72T1280x0HR–[3S/3.7/5]–B, HYS72T256220HR–[3S/3.7/5]–B **Revision History: 2007-01, Rev. 1.2**	
Page	**Subjects (major changes since last revision)**
All	Adapted internet edition
All	Added Product Type HYS72T64000HR-3S-B, HYS72T128000HR-3S-B, HYS72T128020HR-3S-B and HYS72T256220HR-3S-B
Previous Revision: 2006-09, Rev. 1.11	
All	Qimonda update
Previous Revision: 2006-03, Rev. 1.1	
5	Removed product types for DDR800,DRR667 these are to be found in a separate data sheet
8	Removed DDR800, DDR667 raw card figures
23,25,35, 36	Removed DDR800, DDR667 tables
45	Removed DDR800, DDR667 package outlines
Previous Revision: 2005-07, Rev. 1.0	

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1 Overview

This chapter gives an overview of the 1.8 V 240-Pin Registered DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 240-Pin PC2–5300, PC2–4200 and PC2–3200 DDR2 SDRAM memory modules for PC, Workstation and Server main memory applications
- One rank 64M × 72, 128M × 72 and two ranks 128M × 72, 256M x 72 module organization and 512M ×8, 512M × 4 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512 Mbit DDR2 SDRAMs in P-TFBGA-60 chipsize packages.
- Programmable CAS Latencies (3, 4 and 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- RDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference card layouts Raw Card “A”, “B“, “C“, ”J”
- All speed grades faster than DDR2–400 comply with DDR2–400 timing specifications.
- RoHS compliant products[1)]

TABLE 1
Performance Table

Product Type Speed Code			**–3S**	**–3.7**	**–5**	**Unit**
Speed Grade			**PC2–5300 5–5–5**	**PC2–4200 4–4–4**	**PC2–3200 3–3–3**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	333	266	200	MHz
	@CL4	f_{CK4}	266	266	200	MHz
	@CL3	f_{CK3}	200	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	15	15	ns
Min. Row Precharge Time		t_{RP}	15	15	15	ns
Min. Row Active Time		t_{RAS}	45	45	40	ns
Min. Row Cycle Time		t_{RC}	60	60	55	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The QIMONDA HYS72T[64/128/256]xxxHR–[3S/3.7/5]–B module family are Registered DIMM modules with 30 mm height based on DDR2 technology. DIMMs are available as ECC modules in 64M × 72 (512 MB), 128M × 72 (1GB), 256M × 72 (2GB) organization and density, intended for mounting into 240-Pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1]	Compliance Code[2]	Description	SDRAM Technology
PC2–5300			
HYS72T64000HR–3S–B	512 MB 1Rx8 PC2-5300R-555-12-A0	1 Rank ECC	512 Mbit (×8)
HYS72T128000HR–3S–B	1 GB 1Rx4 PC2-5300R-555-12-C0	1 Rank ECC	512 Mbit (×4)
HYS72T128020HR–3S–B	1 GB 2Rx8 PC2-5300R-555-12-B0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HR–3S–B	2 GB 2Rx4 PC2-5300R-555-12-J1	2 Ranks, ECC	512 Mbit (×4)
PC2–4200			
HYS72T64000HR–3.7–B	512 MB 1Rx8 PC2-4200R-444-12-A0	1 Rank ECC	512 Mbit (×8)
HYS72T128000HR–3.7–B	1 GB 1Rx4 PC2-4200R-444-12-C0	1 Rank ECC	512 Mbit (×4)
HYS72T128020HR–3.7–B	1 GB 2Rx8 PC2-4200R-444-12-B0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HR–3.7–B	2 GB 2Rx4 PC2-4200R-444-12-J1	2 Ranks, ECC	512 Mbit (×4)
PC2–3200			
HYS72T64000HR–5–B	512 MB 1Rx8 PC2-3200R-333-12-A0	1 Rank ECC	512 Mbit (×8)
HYS72T128000HR–5–B	1 GB 1Rx4 PC2-3200R-333-12-C0	1 Rank ECC	512 Mbit (×4)
HYS72T128020HR–5–B	1 GB 2Rx8 PC2-3200R-333-12-B0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HR–5–B	2 GB 2Rx4 PC2-3200R-333-12-J1	2 Ranks, ECC	512 Mbit (×4)

1) All Product Type numbers end with a place code, designating the silicon die revision. Example: HYS72T64000HR–3.7–B, indicating Rev. “B” dies are used for DDR2 SDRAM components. For all QIMONDA DDR2 module and component nomenclature see **Chapter 6** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200R–444–12–A0”, where 4200R means Registered DIMM modules with 4.26 GB/sec Module Bandwidth and “444-12” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card “A”.

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
512 MB	64M ×72	1	ECC	9	14/2/10	A
1 GB	128M ×72	1	ECC	18	14/2/11	C
1 GB	128M ×72	2	ECC	18	14/2/10	B
2 GB	256M ×72	2	ECC	36	14/2/11	J

TABLE 4
Components on Modules

Product Type[1)]	DRAM Components[1)]	DRAM Density	DRAM Organisation	Note[2)]
HYS72T64000HR	HYB18T512800BF	512 Mbit	512M ×8	—
HYS72T128000HR	HYB18T512400BF	512 Mbit	512M ×4	—
HYS72T128020HR	HYB18T512800BF	512 Mbit	512M ×8	—
HYS72T256220HR	HYB18T512400BF	512 Mbit	512M ×4	—

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configuration

This chapter describes the pin configuration.

2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 5
Pin Configuration of RDIMM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signal CK0, Complementary Clock Signal CK0**
186	$\overline{CK0}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enables 1:0**
171	CKE1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
Control Signals				
193	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0**
76	$\overline{S1}$	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
192	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
74	$\overline{CAS}$	I	SSTL	
73	$\overline{WE}$	I	SSTL	
18	$\overline{RESET}$	I	CMOS	**Register Reset**
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0**
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	**Not Connected** Less than 1Gb DDR2 SDRAMS

Ball No.	Name	Pin Type	Buffer Type	Function
188	A0	I	SSTL	**Address Bus 12:0, Address Signal 10/AutoPrecharge**
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13**
	NC	NC	—	**Not Connected** *Note: Non CA parity modules based on 256 Mbit component*
174	A14	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module. Less than 1 GBit per DRAM die.*
173	A15	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module. Less than 1 GBit per DRAM die.*

Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
206	DQ39	I/O	SSTL	**Data Bus 63:0**
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bits				
42	CB0	I/O	SSTL	**Check Bits 7:0** *Note: NC on Non-ECC module*
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobes 17:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
125	DQS9	I/O	SSTL	
126	$\overline{\text{DQS9}}$	I/O	SSTL	
134	DQS10	I/O	SSTL	
135	$\overline{\text{DQS10}}$	I/O	SSTL	
146	DQS11	I/O	SSTL	
147	$\overline{\text{DQS11}}$	I/O	SSTL	
155	DQS12	I/O	SSTL	
156	$\overline{\text{DQS12}}$	I/O	SSTL	
202	DQS13	I/O	SSTL	
203	$\overline{\text{DQS13}}$	I/O	SSTL	
211	DQS14	I/O	SSTL	
212	$\overline{\text{DQS14}}$	I/O	SSTL	
223	DQS15	I/O	SSTL	
224	$\overline{\text{DQS15}}$	I/O	SSTL	
232	DQS16	I/O	SSTL	
233	$\overline{\text{DQS16}}$	I/O	SSTL	
164	DQS17	I/O	SSTL	
165	$\overline{\text{DQS17}}$	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
Data Mask				
125	DM0	I	SSTL	**Data Masks 8:0** *Note: ×8 based module*
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock**
119	SDA	I/O	OD	**Serial Bus Data**
239	SA0	I	CMOS	**Serial Address Select Bus 2:0**
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Parity				
55	$\overline{\text{ERR_OUT}}$	O	CMOS	**Parity bits**
68	PAR_IN	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197	V_{DD}	PWR	—	**Power Supply**
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	—	**Ground Plane**

Ball No.	Name	Pin Type	Buffer Type	Function
Other Pins				
19, 102, 137, 138, 220, 221	NC	NC	—	**Not connected**
195	ODT0	I	SSTL	**On-Die Termination Control 1:0**
77	ODT1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	*Note: 1-Rank modules*

TABLE 6
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

TABLE 7
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

FIGURE 1
Pin Configuration for RDIMM (240 pins)

FRONT SIDE Pin	Signal	BACK SIDE Pin	Signal
Pin 001	VREF	Pin 121	V_{SS}
Pin 002	V_{SS}	Pin 122	DQ4
Pin 003	DQ0	Pin 123	DQ5
Pin 004	DQ1	Pin 124	V_{SS}
Pin 005	V_{SS}	Pin 125	DM0/DQS9
Pin 006	$\overline{DQS0}$	Pin 126	NC/$\overline{DQS9}$
Pin 007	DQS0	Pin 127	V_{SS}
Pin 008	V_{SS}	Pin 128	DQ6
Pin 009	DQ2	Pin 129	DQ7
Pin 010	DQ3	Pin 130	V_{SS}
Pin 011	V_{SS}	Pin 131	DQ12
Pin 012	DQ8	Pin 132	DQ13
Pin 013	DQ9	Pin 133	V_{SS}
Pin 014	V_{SS}	Pin 134	DM1/DQS10
Pin 015	$\overline{DQS1}$	Pin 135	NC/$\overline{DQS10}$
Pin 016	DQS1	Pin 136	V_{SS}
Pin 017	V_{SS}	Pin 137	NC
Pin 018	$\overline{RESET}$	Pin 138	NC
Pin 019	NC	Pin 139	V_{SS}
Pin 020	V_{SS}	Pin 140	DQ14
Pin 021	DQ10	Pin 141	DQ15
Pin 022	DQ11	Pin 142	V_{SS}
Pin 023	V_{SS}	Pin 143	DQ20
Pin 024	DQ16	Pin 144	DQ21
Pin 025	DQ17	Pin 145	V_{SS}
Pin 026	V_{SS}	Pin 146	DM2/DQS11
Pin 027	$\overline{DQS2}$	Pin 147	NC/$\overline{DQS11}$
Pin 028	DQS2	Pin 148	V_{SS}
Pin 029	V_{SS}	Pin 149	DQ22
Pin 030	DQ18	Pin 150	DQ23
Pin 031	DQ19	Pin 151	V_{SS}
Pin 032	V_{SS}	Pin 152	DQ28
Pin 033	DQ24	Pin 153	DQ29
Pin 034	DQ25	Pin 154	V_{SS}
Pin 035	V_{SS}	Pin 155	DM3/DQS12
Pin 036	$\overline{DQS3}$	Pin 156	NC/$\overline{DQS12}$
Pin 037	DQS3	Pin 157	V_{SS}
Pin 038	V_{SS}	Pin 158	DQ30
Pin 039	DQ26	Pin 159	DQ31
Pin 040	DQ27	Pin 160	V_{SS}
Pin 041	V_{SS}	Pin 161	CB4
Pin 042	CB0	Pin 162	CB5
Pin 043	CB1	Pin 163	V_{SS}
Pin 044	V_{SS}	Pin 164	DM8/DQS17
Pin 045	$\overline{DQS8}$	Pin 165	NC/$\overline{DQS17}$
Pin 046	DQS8	Pin 166	V_{SS}
Pin 047	V_{SS}	Pin 167	CB6
Pin 048	CB2	Pin 168	CB7
Pin 049	CB3	Pin 169	V_{SS}
Pin 050	V_{SS}	Pin 170	V_{DDQ}
Pin 051	V_{DDQ}	Pin 171	NC/CKE1
Pin 052	CKE0	Pin 172	V_{DD}
Pin 053	V_{DD}	Pin 173	NC
Pin 054	NC/BA2	Pin 174	NC/A14
Pin 055	NC	Pin 175	V_{DDQ}
Pin 056	V_{DDQ}	Pin 176	A12
Pin 057	A11	Pin 177	A9
Pin 058	A7	Pin 178	V_{DD}
Pin 059	V_{DD}	Pin 179	A8
Pin 060	A5	Pin 180	A6
Pin 061	A4	Pin 181	V_{DDQ}
Pin 062	V_{DDQ}	Pin 182	A3
Pin 063	A2	Pin 183	A1
Pin 064	V_{DD}	Pin 184	V_{DD}
Pin 065	V_{SS}	Pin 185	CK0
Pin 066	V_{SS}	Pin 186	$\overline{CK0}$
Pin 067	V_{DD}	Pin 187	V_{DD}
Pin 068	NC	Pin 188	A0
Pin 069	V_{DD}	Pin 189	V_{DD}
Pin 070	A10/AP	Pin 190	BA1
Pin 071	BA0	Pin 191	V_{DDQ}
Pin 072	V_{DDQ}	Pin 192	$\overline{RAS}$
Pin 073	$\overline{WE}$	Pin 193	$\overline{S0}$
Pin 074	$\overline{CAS}$	Pin 194	V_{DDQ}
Pin 075	V_{DDQ}	Pin 195	ODT0
Pin 076	NC/$\overline{S1}$	Pin 196	NC/A13
Pin 077	NC/ODT1	Pin 197	V_{DD}
Pin 078	V_{DDQ}	Pin 198	V_{SS}
Pin 079	V_{SS}	Pin 199	DQ36
Pin 080	DQ32	Pin 200	DQ37
Pin 081	DQ33	Pin 201	V_{SS}
Pin 082	V_{SS}	Pin 202	DM4/DQS13
Pin 083	$\overline{DQS4}$	Pin 203	NC/$\overline{DQS13}$
Pin 084	DQS4	Pin 204	V_{SS}
Pin 085	V_{SS}	Pin 205	DQ38
Pin 086	DQ34	Pin 206	DQ39
Pin 087	DQ35	Pin 207	V_{SS}
Pin 088	V_{SS}	Pin 208	DQ44
Pin 089	DQ40	Pin 209	DQ45
Pin 090	DQ41	Pin 210	V_{SS}
Pin 091	V_{SS}	Pin 211	DM5/DQS14
Pin 092	$\overline{DQS5}$	Pin 212	NC/$\overline{DQS14}$
Pin 093	DQS5	Pin 213	V_{SS}
Pin 094	V_{SS}	Pin 214	DQ46
Pin 095	DQ42	Pin 215	DQ47
Pin 096	DQ43	Pin 216	V_{SS}
Pin 097	V_{SS}	Pin 217	DQ52
Pin 098	DQ48	Pin 218	DQ53
Pin 099	DQ49	Pin 219	V_{SS}
Pin 100	V_{SS}	Pin 220	NC
Pin 101	SA2	Pin 221	NC
Pin 102	NC	Pin 222	V_{SS}
Pin 103	V_{SS}	Pin 223	DM6/DQS15
Pin 104	$\overline{DQS6}$	Pin 224	NC/$\overline{DQS15}$
Pin 105	DQS6	Pin 225	V_{SS}
Pin 106	V_{SS}	Pin 226	DQ54
Pin 107	DQ50	Pin 227	DQ55
Pin 108	DQ51	Pin 228	V_{SS}
Pin 109	V_{SS}	Pin 229	DQ60
Pin 110	DQ56	Pin 230	DQ61
Pin 111	DQ57	Pin 231	V_{SS}
Pin 112	V_{SS}	Pin 232	DM7/DQS16
Pin 113	$\overline{DQS7}$	Pin 233	NC/$\overline{DQS16}$
Pin 114	DQS7	Pin 234	V_{SS}
Pin 115	V_{SS}	Pin 235	DQ62
Pin 116	DQ58	Pin 236	DQ63
Pin 117	DQ59	Pin 237	V_{SS}
Pin 118	V_{SS}	Pin 238	VDDSPD
Pin 119	SDA	Pin 239	SA0
Pin 120	SCL	Pin 240	SA1

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3 Electrical Characteristics

This chapter describes the electrical characteristics.

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 8** at any time.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 9
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs.
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50 %

3.2 DC Characteristics

This chapter describes the DC characteristics.

TABLE 10
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	—
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	—
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	—
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	—
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin.

TABLE 11
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	—
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	—
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	—

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported.
3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%.
5) Up to 3000 m

3.3 Timing Characteristics

This chapter contains the AC characteristics.

3.3.1 Speed Grade Definitions

All Speed grades faster than DDR2-400B comply with DDR2-400B timing specifications(t_{CK} = 5ns with t_{RAS} = 40ns).

TABLE 12
Speed Grade Definition

Speed Grade			DDR2–667		DDR2–533C		DDR2–400B		Unit	Note
QAG Sort Name			–3S		–3.7		–5			
CAS-RCD-RP latencies			5–5–5		4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the “Reference Load for Timing Measurements”
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 Component AC Timing Parameters

List of AC timing parameter tables.

- **Table 13 "DRAM Component Timing Parameter by Speed Grade - DDR2–667" on Page 17**
- **Table 14 "DRAM Component Timing Parameter by Speed Grade - DDR2–533" on Page 21**
- **Table 15 "DRAM Component Timing Parameter by Speed Grade - DDR2-400" on Page 23**

TABLE 13
DRAM Component Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Note1)2)3)4)5)6)7)8)
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	9)
CAS to CAS command delay	t_{CCD}	2	—	nCK	—
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	—
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	12)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	13)14)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK.AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	19)20)15)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	—
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	9)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	—
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	—
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	240	ps	16)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	17)
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	18)19)20)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	17)
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	17)
CK half pulse width	t_{HP}	Min ($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	21)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	9)22)
Address and control input hold time	$t_{IH.BASE}$	275	—	ps	25)23)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	—
Address and control input setup time	$t_{IS.BASE}$	200	—	ps	24)25)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
MRS command to ODT update delay	t_{MOD}	0	12	ns	1)
Mode register set command cycle time	t_{MRD}	2	—	nCK	—
OCD drive mode output delay	t_{OIT}	0	12	ns	1)

Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	ps	26)
DQ hold skew factor	t_{QHS}	—	340	ps	27)
Average periodic refresh Interval 0°C ≤ T_{CASE} ≤ 85°C 85°C ≤ T_{CASE} ≤ 95°C	t_{REFI}	 – –	 7.8 3.9	µs	—
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	28)29)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	28)30)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	1)
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	—
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	—
Write recovery time	t_{WR}	15	—	ns	1)
Internal write to read command delay	t_{WTR}	7.5	—	ns	1)31)
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	nCK	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	—
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	1)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	—
Write command to DQS associated clock edges	WL	RL–1		nCK	—

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
12) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

13) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
14) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 3**.
16) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
17) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
18) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 3**.
19) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
20) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
21) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
22) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
23) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 4**.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 4**.
25) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
26) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
27) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
28) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
29) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)}$ = $t_{RPRE.MIN}$ + $t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)}$ = $t_{RPRE.MAX}$ + $t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
30) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)}$ = $t_{RPST.MIN}$ + $t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)}$ = $t_{RPST.MAX}$ + $t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
31) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

FIGURE 2
Method for calculating transitions and endpoint

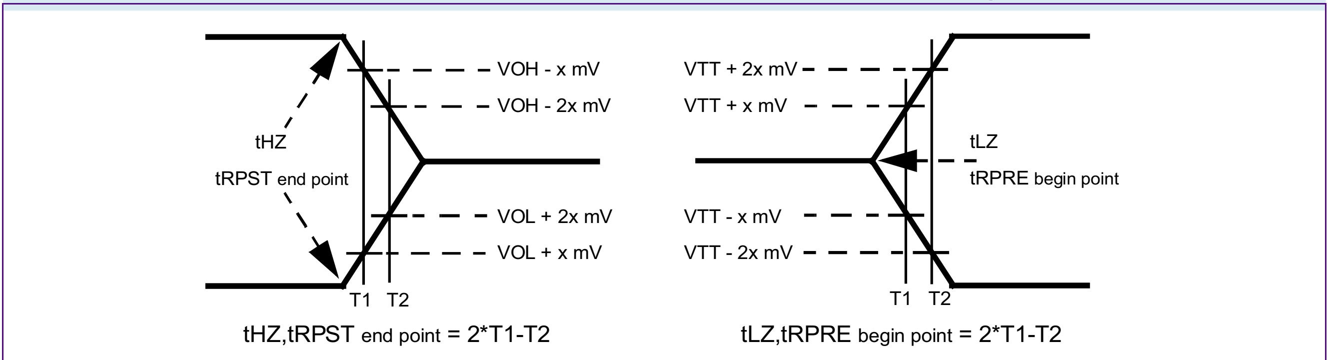

FIGURE 3
Differential input waveform timing - t_{DS} and t_{DS}

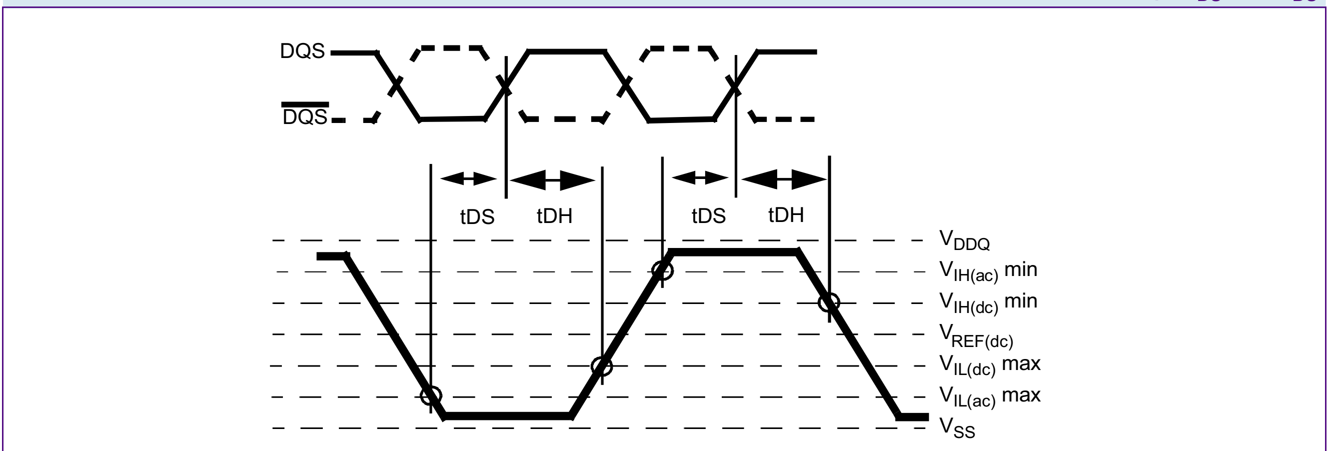

FIGURE 4
Differential input waveform timing - t_{IS} and t_{IH}

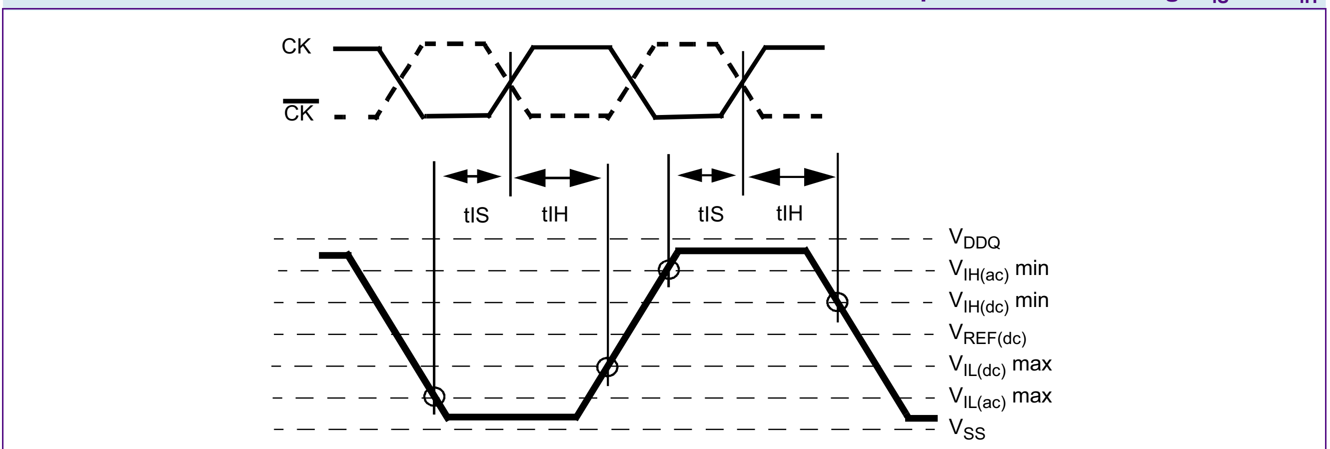

TABLE 14
DRAM Component Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	—
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. ($t_{CL,}$ t_{CH})			12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	375	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	t_{IS}(base)	250	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		—
Data hold skew factor	t_{QHS}	—	400	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
Average periodic refresh Interval	t_{REFI}	—	3.9	μs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	—
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	—
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	16)22)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	0.25	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	21)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	22)

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 "Ordering Information for RoHS Compliant Products" on Page 4**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.
22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

TABLE 15
DRAM Component Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	—
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)21)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	t_{DS} (base)	150	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		—	12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	475	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	t_{IS}(base)	350	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	—	—
Data hold skew factor	t_{QHS}	—	450	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
Average periodic refresh Interval	t_{REFI}	—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	—
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	—
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	16)22)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	0.25	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Internal Write to Read command delay	t_{WTR}	10	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	21)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	—

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	22)

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes [5)6)7)8)]
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 "Ordering Information for RoHS Compliant Products" on Page 4**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.
22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

3.3.3 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

TABLE 16
ODT AC Character. and Operating Conditions for DDR2-667

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	nCK	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	nCK	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	nCK	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	nCK	1)

1) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 × $t_{CK.AVG}$ + $t_{EPR.2PER(MIN)}$.
2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.
3) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK.AVG}$ = 3 ns is assumed, t_{AOFD}= 1.5 ns (0.5 × 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edge.

TABLE 17
ODT AC Characteristics and Operating Conditions for DDR2-533 & DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	—
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	—
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	—
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	—

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

- **Table 18 "IDD Measurement Conditions" on Page 27**
- **Table 21 "IDD Specification for HYS72T[64/128/256]xxxHR–3.7–B" on Page 30**
- **Table 22 "IDD Specification for HYS72T[64/128/256]xxxHR–5–B" on Page 31**

TABLE 18
I_{DD} Measurement Conditions

Parameter	Symbol	Note 1)2)3)4)5)
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	—
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	—
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	—
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	—
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	—
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	—
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	—
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	—

Parameter	Symbol	Note 1)2)3)4)5)
Burst Refresh Current $t_{CK} = t_{CK.MIN}$., Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	—
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	—
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	—
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 19**
4) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
5) For details and notes see the relevant Qimonda component data sheet
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 19
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \le V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \ge V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

TABLE 20
I_{DD} Specification for HYS72T[64/128/256]xxxHR–3S–B

Product Type	HYS72T64000HR–3S–B	HYS72T128000HR–3S–B	HYS72T128020HR–3S–B	HYS72T256220HR–3S–B	Unit	Note[1]
Organization	512 MB	1 GB	1 GB	2 GB		
	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×72	×72	×72	×72		
	-3S	-3S	-3S	-3S		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	1020	1870	1300	2000	mA	2)
I_{DD1}	1150	2130	1420	2250	mA	2)
I_{DD2P}	450	720	720	850	mA	3)
I_{DD2N}	790	1410	1410	2220	mA	3)
I_{DD2Q}	750	1320	1320	2040	mA	3)
$I_{DD3P(MRS = 0)}$	680	1190	1190	1780	mA	3)
$I_{DD3P(MRS = 1)}$	470	760	760	920	mA	3)
I_{DD3N}	840	1500	1500	2400	mA	3)
I_{DD4R}	1560	2940	1830	3060	mA	2)
I_{DD4W}	1560	2940	1830	3060	mA	2)
I_{DD5B}	1650	3120	1920	3240	mA	2)
I_{DD5D}	470	760	760	920	mA	3)4)
I_{DD6}	63	126	126	252	mA	3)4)
I_{DD7}	1750	3330	2030	3460	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes currents of Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD} current mode
4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C

TABLE 21
I_{DD} Specification for HYS72T[64/128/256]xxxHR–3.7–B

Product Type	HYS72T64000HR–3.7–B	HYS72T128000HR–3.7–B	HYS72T128020HR–3.7–B	HYS72T256220HR–3.7–B	Unit	Note[1]
Organization	512 MB	1 GB	1 GB	2 GB		
	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×72	×72	×72	×72		
	-3.7	-3.7	-3.7	-3.7		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	920	1670	1150	1800	mA	2)
I_{DD1}	1010	1850	1240	1980	mA	2)
I_{DD2P}	390	630	630	750	mA	3)
I_{DD2N}	670	1180	1180	1870	mA	3)
I_{DD2Q}	650	1130	1130	1760	mA	3)
$I_{DD3P(\ MRS\ =\ 0)}$	580	1000	1000	1510	mA	3)
$I_{DD3P(\ MRS\ =\ 1)}$	410	660	660	820	mA	3)
I_{DD3N}	720	1270	1270	2050	mA	3)
I_{DD4R}	1320	2480	1550	2610	mA	2)
I_{DD4W}	1320	2480	1550	2610	mA	2)
I_{DD5B}	1500	2840	1730	2970	mA	2)
I_{DD5D}	410	660	660	820	mA	3)4)
I_{DD6}	63	126	126	252	mA	3)4)
I_{DD7}	1640	3110	1870	3240	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes currents of Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD} current mode
4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C

TABLE 22
I_{DD} Specification for HYS72T[64/128/256]xxxHR–5–B

Product Type	HYS72T64000HR–5–B	HYS72T128000HR–5–B	HYS72T128020HR–5–B	HYS72T256220HR–5–B	Unit	Note[1]
Organization	512 MB	1 GB	1GB	2 GB		
	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×72	×72	×72	×72		
	-5	-5	-5	-5		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	820	1500	1020	1630	mA	[2]
I_{DD1}	910	1670	1100	1790	mA	[2]
I_{DD2P}	340	530	530	660	mA	[3]
I_{DD2N}	580	1020	1020	1630	mA	[3]
I_{DD2Q}	560	980	980	1560	mA	[3]
$I_{DD3P(MRS = 0)}$	490	840	840	1270	mA	[3]
$I_{DD3P(MRS = 1)}$	360	570	570	730	mA	[3]
I_{DD3N}	630	1110	1110	1810	mA	[3]
I_{DD4R}	1130	2120	1320	2240	mA	[2]
I_{DD4W}	1130	2120	1320	2240	mA	[2]
I_{DD5B}	1400	2660	1590	2780	mA	[2]
I_{DD5D}	360	570	570	730	mA	[3][4]
I_{DD6}	63	126	126	252	mA	[3][4]
I_{DD7}	1540	2940	1740	3070	mA	[2]

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes currents of Registers and PLL. ODT disabled. $I_{DD1,}$ $I_{DD4R,}$ and $I_{DD7,}$ are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode.
3) Both ranks are in the same I_{DD}current mode.
4) I_{DD5D} and I_{DD6} values are for 0 °C ≤ T_{Case} ≤ 85 °C.

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- **Table 23 "HYS72T[64/128/256]xx0HR–3S–B" on Page 32**
- **Table 24 "HYS72T[64/128/256]xx0HR–3.7–B" on Page 37**
- **Table 25 "HYS72T[64/128/256]xx0HR–5–B" on Page 41**

TABLE 23
HYS72T[64/128/256]xx0HR–3S–B

Product Type		HYS72T64000HR–3S–B	HYS72T128000HR–3S–B	HYS72T128020HR–3S–B	HYS72T256220HR–3S–B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2–5300R–555	PC2–5300R–555	PC2–5300R–555	PC2–5300R–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B
5	DIMM Rank and Stacking Information	60	60	61	61
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82

Product Type		**HYS72T64000HR–3S–B**	**HYS72T128000HR–3S–B**	**HYS72T128020HR–3S–B**	**HYS72T256220HR–3S–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
13	Primary SDRAM Width	08	04	08	04
14	Error Checking SDRAM Width	08	04	08	04
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	04	05	05	07
22	Component Attributes	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E

Product Type		**HYS72T64000HR–3S–B**	**HYS72T128000HR–3S–B**	**HYS72T128020HR–3S–B**	**HYS72T256220HR–3S–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22	22
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A
49	ΔT_0 (DT0)	4B	4B	4B	4B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	2E	2E	2E	2E
51	ΔT_{2P} (DT2P)	36	36	36	36
52	ΔT_{3N} (DT3N)	27	27	27	27
53	$\Delta T_{3P.fast}$ (DT3P fast)	4C	4C	4C	4C
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4C	4C	4C	4C
56	ΔT_{5B} (DT5B)	20	20	20	20
57	ΔT_7 (DT7)	23	23	23	23
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	68	68	68	68
61	ΔT_{REG} (DTREG) / Toggle Rate	94	94	94	94
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	8A	05	8C	08
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F

Product Type		HYS72T64000HR–3S–B	HYS72T128000HR–3S–B	HYS72T128020HR–3S–B	HYS72T256220HR–3S–B
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	31	31	32
77	Product Type, Char 5	34	32	32	35
78	Product Type, Char 6	30	38	38	36
79	Product Type, Char 7	30	30	30	32
80	Product Type, Char 8	30	30	32	32
81	Product Type, Char 9	48	30	30	30
82	Product Type, Char 10	52	48	48	48
83	Product Type, Char 11	33	52	52	52
84	Product Type, Char 12	53	33	33	33
85	Product Type, Char 13	42	53	53	53
86	Product Type, Char 14	20	42	42	42
87	Product Type, Char 15	20	20	20	20
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20

Product Type		**HYS72T64000HR–3S–B**	**HYS72T128000HR–3S–B**	**HYS72T128020HR–3S–B**	**HYS72T256220HR–3S–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
91	Module Revision Code	4x	4x	4x	2x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

TABLE 24
HYS72T[64/128/256]xx0HR–3.7–B

Product Type		**HYS72T64000HR–3.7–B**	**HYS72T128000HR–3.7–B**	**HYS72T128020HR–3.7–B**	**HYS72T256220HR–3.7–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B
5	DIMM Rank and Stacking Information	60	60	61	61
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	08	04	08	04
14	Error Checking SDRAM Width	08	04	08	04
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	04	05	05	07
22	Component Attributes	07	07	07	07

Product Type		**HYS72T64000HR–3.7–B**	**HYS72T128000HR–3.7–B**	**HYS72T128020HR–3.7–B**	**HYS72T256220HR–3.7–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28	28
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A

Product Type		**HYS72T64000HR–3.7–B**	**HYS72T128000HR–3.7–B**	**HYS72T128020HR–3.7–B**	**HYS72T256220HR–3.7–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
49	ΔT_0 (DT0)	43	43	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	29	29	29	29
51	ΔT_{2P} (DT2P)	36	36	36	36
52	ΔT_{3N} (DT3N)	21	21	21	21
53	$\Delta T_{3P.fast}$ (DT3P fast)	41	41	41	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	40	40	40	40
56	ΔT_{5B} (DT5B)	1E	1E	1E	1E
57	ΔT_7 (DT7)	22	22	22	22
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	61	61	61	61
61	ΔT_{REG} (DTREG) / Toggle Rate	78	78	78	78
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	7E	F9	80	FC
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32

Product Type		HYS72T64000HR–3.7–B	HYS72T128000HR–3.7–B	HYS72T128020HR–3.7–B	HYS72T256220HR–3.7–B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2–4200R–444	PC2–4200R–444	PC2–4200R–444	PC2–4200R–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	31	31	32
77	Product Type, Char 5	34	32	32	35
78	Product Type, Char 6	30	38	38	36
79	Product Type, Char 7	30	30	30	32
80	Product Type, Char 8	30	30	32	32
81	Product Type, Char 9	48	30	30	30
82	Product Type, Char 10	52	48	48	48
83	Product Type, Char 11	33	52	52	52
84	Product Type, Char 12	2E	33	33	33
85	Product Type, Char 13	37	2E	2E	2E
86	Product Type, Char 14	42	37	37	37
87	Product Type, Char 15	20	42	42	42
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	4x	4x	4x	2x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

TABLE 25
HYS72T[64/128/256]xx0HR–5–B

Product Type		HYS72T64000HR–5–B	HYS72T128000HR–5–B	HYS72T128020HR–5–B	HYS72T256220HR–5–B
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B
5	DIMM Rank and Stacking Information	60	60	61	61
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60	60	60	60
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	08	04	08	04
14	Error Checking SDRAM Width	08	04	08	04
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	04	05	05	07
22	Component Attributes	07	07	07	07

Product Type		**HYS72T64000HR–5–B**	**HYS72T128000HR–5–B**	**HYS72T128020HR–5–B**	**HYS72T256220HR–5–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	50	50	50	50
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	60	60	60	60
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28	28
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D	2D
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A

Product Type		**HYS72T64000HR–5–B**	**HYS72T128000HR–5–B**	**HYS72T128020HR–5–B**	**HYS72T256220HR–5–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
49	ΔT_0 (DT0)	3B	3B	3B	3B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	25	25	25
51	ΔT_{2P} (DT2P)	36	36	36	36
52	ΔT_{3N} (DT3N)	1E	1E	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	38	38	38	38
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	38	38	38	38
56	ΔT_{5B} (DT5B)	1D	1D	1D	1D
57	ΔT_7 (DT7)	21	21	21	21
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	59	59	59	59
61	ΔT_{REG} (DTREG) / Toggle Rate	5C	5C	5C	5C
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	B2	2D	B4	30
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32

Product Type		**HYS72T64000HR–5–B**	**HYS72T128000HR–5–B**	**HYS72T128020HR–5–B**	**HYS72T256220HR–5–B**
Organization		**512MB**	**1 GByte**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	31	31	32
77	Product Type, Char 5	34	32	32	35
78	Product Type, Char 6	30	38	38	36
79	Product Type, Char 7	30	30	30	32
80	Product Type, Char 8	30	30	32	32
81	Product Type, Char 9	48	30	30	30
82	Product Type, Char 10	52	48	48	48
83	Product Type, Char 11	35	52	52	52
84	Product Type, Char 12	42	35	35	35
85	Product Type, Char 13	20	42	42	42
86	Product Type, Char 14	20	20	20	20
87	Product Type, Char 15	20	20	20	20
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	4x	4x	4x	2x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

5 Package Outlines

This chapter contains the package outlines.

FIGURE 5
Package Outline Raw Card A L-DIM-240-11

Burr max. 0.4 allowed

GLD09655

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 6
Package Outline Raw Card C L-DIM-240-13

Detail of contacts

— — Burr max. 0.4 allowed

GLD09657

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 7
Package Outline Raw Card B L-DIM-240-12

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 8
Package Outline Raw Card J L-DIM-240-20

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some propriatory coding. **Table 26** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 27** and for components in **Table 28**.

TABLE 26
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	—

TABLE 27
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–2.5F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 28
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–25F	DDR2-800 5-5-5
		–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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