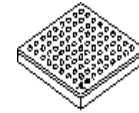




MCIMX35



Package Information

Plastic package
Case 5284 17 x 17 mm, 0.8 mm Pitch

i.MX35 Applications Processors for Industrial and Consumer Products

Silicon Revisions 2.0 and 2.1

Ordering Information

See [Table 1 on page 3](#) for ordering information.

1 Introduction

The i.MX353 and the i.MX357 multimedia applications processors represent the next generation of ARM11 products with the right performance and integration to address applications within the industrial and consumer markets for applications such as HMI and display controllers. Unless otherwise specified, the material in this data sheet is applicable to both the i.MX353 and i.MX357 devices and referred to singularly throughout this document as i.MX35 or MCIMX35. The i.MX353 devices do not include a graphics processing unit (GPU). For information on i.MX35 devices for automotive applications, please refer to document number, MCIMX35SR2AEC.

The i.MX35 processor takes advantage of the ARM1136JF-S™ core running at 532 MHz that is boosted by a multi-level cache system and integrated features such as LCD controller, Ethernet, and graphics acceleration for creating rich user interfaces.

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The i.MX35 supports connections to various types of external memories, such as SDRAM, mobile DDR, and DDR2, SLC and MLC NAND Flash, NOR Flash and SRAM. The devices can be connected to a variety of external devices such as USB 2.0 OTG, ATA, MMC/SDIO, and Compact Flash.

1.1 Features

It provides low-power solutions for applications demanding high-performance multimedia and graphics.

The i.MX35 is based on the ARM1136 platform, which has the following features:

- ARM1136JF-S processor, version r1p3
- 16-Kbyte L1 instruction cache
- 16-Kbyte L1 data cache
- 128-Kbyte L2 cache, version r0p4
- 128 Kbytes of internal SRAM
- Vector floating point unit (VFP11)

To boost multimedia performance, the following hardware accelerators are integrated:

- Image processing unit (IPU)
- OpenVG 1.1 graphics processing unit (GPU)

The MCIMX35 provides the following interfaces to external devices (some of these interfaces are muxed and not available simultaneously):

- 2 controller area network (CAN) interfaces
- 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface
- 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133 MHz)
- 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
- Enhanced serial audio interface (ESAI)
- 2 synchronous serial interfaces (SSI)
- Ethernet MAC 10/100 Mbps
- 1 USB 2.0 host with ULPI interface or internal full-speed PHY. Up to 480 Mbps if external HS PHY is used.
- 1 USB 2.0 OTG (up to 480 Mbps) controller with internal high-speed OTG PHY
- Flash controller—MLC/SLC NAND and NOR
- GPIO with interrupt capabilities
- 3 I²C modules (up to 400 Kbytes each)
- JTAG
- Key pin port
- Asynchronous sample rate converter (ASRC)
- 1-Wire
- Parallel camera sensor (4/8/10/16-bit data port for video color models: YCC, YUV, 30 Mpixels/s)
- Parallel display (primary up to 24-bit, 1024 x 1024)

- Parallel ATA (up to 66 Mbytes)
- PWM
- SPDIF transceiver
- 3 UART (up to 4.0 Mbps each)

1.2 Ordering Information

Table 1 provides the ordering information for the i.MX35 processors for consumer and industrial applications.

Table 1. Ordering Information

Description	Part Number ¹	Silicon Revision	Package ²	Speed	Operating Temperature Range (°C)	Signal Ball Map Locations	Ball Map
i.MX353	MCIMX353CVM5B!	2.0	5284	532 MHz	-40 to 85	Table 90	Table 92
i.MX353	MCIMX353DVM5B!	2.0	5284	532 MHz	-20 to 70	Table 90	Table 92
i.MX357	MCIMX357CVM5B!	2.0	5284	532 MHz	-40 to 85	Table 90	Table 92
i.MX357	MCIMX357DVM5B!	2.0	5284	532 MHz	-20 to 70	Table 90	Table 92
i.MX353	MCIMX353CJQ5C	2.1	5284	532MHz	-40 to 85	Table 91	Table 93
i.MX353	MCIMX353DJQ5C	2.1	5284	532MHz	-20 to 70	Table 91	Table 93
i.MX357	MCIMX357CJQ5C	2.1	5284	532MHz	-40 to 85	Table 91	Table 93
i.MX357	MCIMX357DJQ5C	2.1	5284	532MHz	-20 to 70	Table 91	Table 93

¹ Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

² Case 5284 is RoHS-compliant, lead-free, MSL = 3, 1.

The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout. See Section 5, “Package Information and Pinout.”

1.3 Block Diagram

Figure 1 is the i.MX35 simplified interface block diagram.

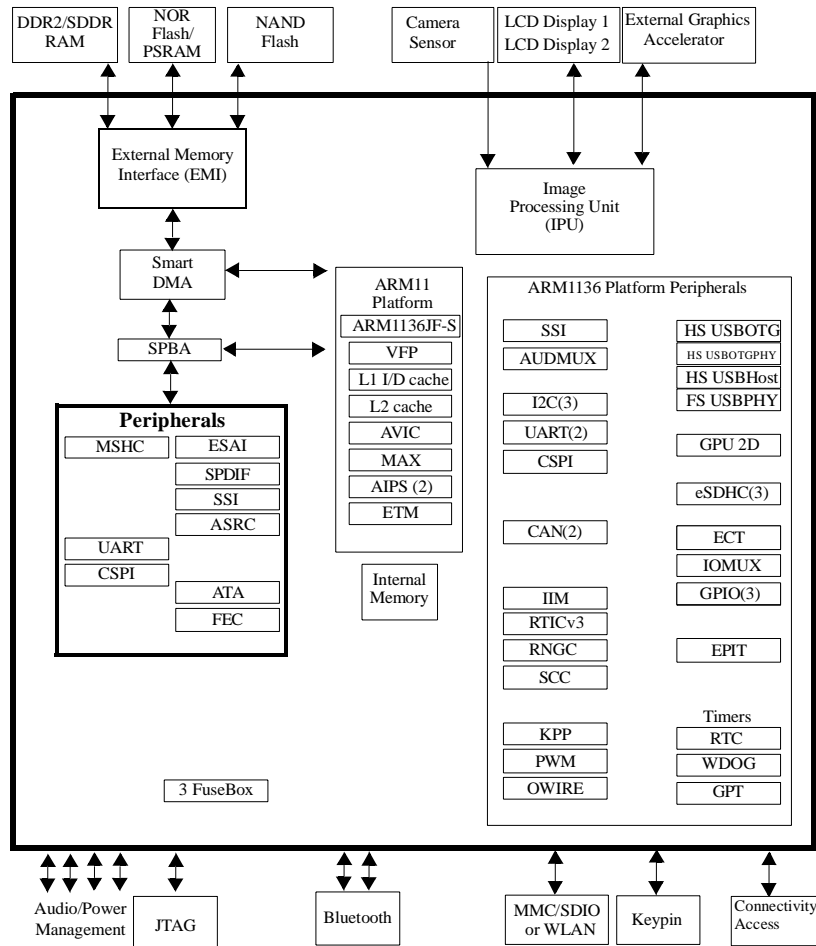


Figure 1. i.MX35 Simplified Interface Block Diagram

2 Functional Description and Application Information

The i.MX35 consists of the following major subsystems:

- ARM1136 Platform—AP domain
- SDMA Platform and EMI—Shared domain

2.1 Application Processor Domain Overview

The applications processor (AP) and its domain are responsible for running the operating system and applications software, providing the user interface, and supplying access to integrated and external peripherals. The AP domain is built around an ARM1136JF-S core with 16-Kbyte instruction and data L1 caches, an MMU, a 128-Kbyte L2 cache, a multiported crossbar switch, and advanced debug and trace interfaces.

The i.MX35 core is intended to operate at a maximum frequency of 532 MHz to support the required multimedia use cases. Furthermore, an image processing unit (IPU) is integrated into the AP domain to offload the ARM11 core from performing functions such as color space conversion, image rotation and scaling, graphics overlay, and pre- and post-processing.

The functionality of AP Domain peripherals includes the user interface; the connectivity, display, security, and memory interfaces; and 128 Kbytes of multipurpose SRAM.

2.2 Shared Domain Overview

The shared domain is composed of the shared peripherals, a smart DMA engine (SDMA) and a number of miscellaneous modules. For maximum flexibility, some peripherals are directly accessible by the SDMA engine.

The i.MX35 has a hierarchical memory architecture including L1 caches and a unified L2 cache. This reduces the bandwidth demands for the external bus and external memory. The external memory subsystem supports a flexible external memory system, including support for SDRAM (SDR, DDR2 and mobile DDR) and NAND Flash.

2.3 Advanced Power Management Overview

To address the continuing need to reduce power consumption, the following techniques are incorporated in the i.MX35:

- Clock gating
- Power gating
- Power-optimized synthesis
- Well biasing

The insertion of gating into the clock paths allows unused portions of the chip to be disabled. Because static CMOS logic consumes only leakage power, significant power savings can be realized.

“Well biasing” is applying a voltage that is greater than V_{DD} to the nwells, and one that is lower than V_{SS} to the pwells. The effect of applying this well back bias voltage reduces the subthreshold channel leakage. For the 90-nm digital process, it is estimated that the subthreshold leakage is reduced by a factor of ten over the nominal leakage. Additionally, the supply voltage for internal logic can be reduced from 1.4 V to 1.22 V.

2.4 ARM11 Microprocessor Core

The CPU of the i.MX35 is the ARM1136JF-S core, based on the ARM v6 architecture. This core supports the ARM Thumb[®] instruction sets, features Jazelle[®] technology (which enables direct execution of Java byte codes) and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features are as follows:

- Integer unit with integral EmbeddedICE[™] logic
- Eight-stage pipeline

- Branch prediction with return stack
- Low-interrupt latency
- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with hit-under-miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)[™] L2 interface
- Vector floating point co-processor (VFP) for 3D graphics and hardware acceleration of other floating-point applications
- ETM[™] and JTAG-based debug support

Table 2 summarizes information about the i.MX35 core.

Table 2. i.MX35 Core

Core Acronym	Core Name	Brief Description	Integrated Memory Features
ARM11 or ARM1136	ARM1136 Platform	The ARM1136 [™] platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 × 5 multi-layer AHB crossbar switch (MAX), and a vector floating processor (VFP). The i.MX35 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	<ul style="list-style-type: none"> • 16-Kbyte instruction cache • 16-Kbyte data cache • 128-Kbyte L2 cache • 32-Kbyte ROM • 128-Kbyte RAM

2.5 Module Inventory

Table 3 shows an alphabetical listing of the modules in the MCIMX35. For extended descriptions of the modules, see the MCIMX35 reference manual.

Table 3. Digital and Analog Modules

Block Mnemonic	Block Name	Domain ¹	Subsystem	Brief Description
1-WIRE	1-Wire interface	ARM	ARM1136 platform peripherals	1-Wire provides the communication line to a 1-Kbit add-only memory. the interface can send or receive 1 bit at a time.
ASRC	Asynchronous sample rate converter	SDMA	Connectivity peripherals	The ASRC is designed to convert the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. It supports a concurrent sample rate conversion of about –120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain ¹	Subsystem	Brief Description
ATA	ATA module	SDMA	Connectivity peripherals	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disk drives and ATAPI optical disk drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	ARM	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CAN(2)	CAN module	ARM	Connectivity peripherals	The CAN protocol is primarily designed to be used as a vehicle serial data bus running at 1 Mbps.
CCM	Clock control module	ARM	Clocks	This block generates all clocks for the peripherals in the SDMA platform. The CCM also manages ARM1136 platform low-power modes (WAIT, STOP), disabling peripheral clocks appropriately for power conservation, and provides alternate clock sources for the ARM1136 and SDMA platforms.
CSPI(2)	Configurable serial peripheral interface	SDMA, ARM	Connectivity peripherals	This module is a serial interface equipped with data FIFOs; each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and slave select (SS) control signals enable fast data communication with fewer software interrupts.
ECT	Embedded cross trigger	SDMA, ARM	Debug	ECT (embedded cross trigger) is an IP for real-time debug purposes. It is a programmable matrix allowing several subsystems to interact with each other. ECT receives signals required for debugging purposes (from cores, peripherals, buses, external inputs, and so on) and propagates them (propagation programmed through software) to the different debug resources available within the SoC.
EMI	External memory interface	SDMA	External memory interface	The EMI module provides access to external memory for the ARM and other masters. It is composed of the following main submodules: M3IF—provides arbitration between multiple masters requesting access to the external memory. SDRAM CTRL—interfaces to mDDR, DDR2 (4-bank architecture type), and SDR interfaces. NANDFC—provides an interface to NAND Flash memories. WEIM—interfaces to NOR Flash and PSRAM.
EPIT(2)	Enhanced periodic interrupt timer	ARM	Timer peripherals	Each EPIT is a 32-bit “set-and-forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain ¹	Subsystem	Brief Description
ESAI	Enhanced serial audio interface	SDMA	Connectivity peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHCv2 (3)	Enhanced secure digital host controller	ARM	Connectivity peripherals	The eSDHCv2 consists of four main modules: CE-ATA, MMC, SD and SDIO. CE-ATA is a hard drive interface that is optimized for embedded applications of storage. The MultiMediaCard (MMC) is a universal, low-cost, data storage and communication media to applications such as electronic toys, organizers, PDAs, and smart phones. The secure digital (SD) card is an evolution of MMC and is specifically designed to meet the security, capacity, performance, and environment requirements inherent in emerging audio and video consumer electronic devices. SD cards are categorized into Memory and I/O. A memory card enables a copyright protection mechanism that complies with the SDMI security standard. SDIO cards provide high-speed data I/O (such as wireless LAN via SDIO interface) with low power consumption. Note:
FEC	Ethernet	SDMA	Connectivity peripherals	The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media
GPIO(3)	General purpose I/O modules	ARM	Pins	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General purpose timers	ARM	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with a programmable prescaler and compare and capture registers. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics processing unit 2Dv1	ARM	Multimedia peripherals	This module accelerates OpenVG and GDI graphics. Note:

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain ¹	Subsystem	Brief Description
I ² C(3)	I ² C module	ARM	ARM1136 platform peripherals	Inter-integrated circuit (I ² C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I ² C is suitable for applications requiring occasional communications over a short distance among many devices. The interface operates at up to 100 kbps with maximum bus loading and timing. The I ² C system is a true multiple-master bus, with arbitration and collision detection that prevent data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC identification module	ARM	Security modules	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	External signals and pin multiplexing	ARM	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution with the following features: <ul style="list-style-type: none"> • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths held at constant levels for reduced power consumption
IPUv1	Image processing unit	ARM	Multimedia peripherals	The IPU supports video and graphics processing functions. It also provides the interface for image sensors and displays. The IPU performs the following main functions: <ul style="list-style-type: none"> • Preprocessing of data from the sensor or from the external system memory • Postprocessing of data from the external system memory • Post-filtering of data from the system memory with support of the MPEG-4 (both deblocking and deringing) and H.264 post-filtering algorithms • Displaying video and graphics on a synchronous (dumb or memory-less) display • Displaying video and graphics on an asynchronous (smart) display • Transferring data between IPU sub-modules and to/from the system memory with flexible pixel reformatting
KPP	Keypin port	ARM	Connectivity peripherals	Can be used for either keypin matrix scanning or general purpose I/O.
OSCAUD	OSC audio reference oscillator	Analog	Clock	The OSCAUDIO oscillator provides a stable frequency reference for the PLLs. This oscillator is designed to work in conjunction with an external 24.576-MHz crystal.
OSC24M	OSC24M 24-MHz reference oscillator	Analog	Clock	The signal from the external 24-MHz crystal is the source of the CLK24M signal fed into USB PHY as the reference clock and to the real time clock (RTC).

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Domain ¹	Subsystem	Brief Description
MPLL PPLL	Digital phase-locked loops	SDMA	Clocks	DPLLs are used to generate the clocks: MCU PLL (MPLL)—programmable Peripheral PLL (PPLL)—programmable
PWM	Pulse-width modulator	ARM	ARM1136 platform peripherals	The pulse-width modulator (PWM) is optimized to generate sound from stored sample audio images; it can also generate tones.
RTC	Real-time clock	ARM	Clocks	Provides the ARM1136 platform with a clock function (days, hours, minutes, seconds) and includes alarm, sampling timer, and minute stopwatch capabilities.
SDMA	Smart DMA engine	SDMA	System controls	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels and has an interface to connect to the ARM1136 platform subsystem, EMI interface, and the peripherals.
SJC	Secure JTAG controller	ARM	Pins	The secure JTAG controller (SJC) provides debug and test control with maximum security.
SPBA	SDMA peripheral bus arbiter	SDMA	System controls	The SPBA controls access to the SDMA peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
S/PDIF	Serial audio interface	SDMA	Connectivity peripherals	Sony/Philips digital transceiver interface
SSI(2)	Synchronous serial interface	SDMA, ARM(2)	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor connected to it to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the I ² C sound (I ² S) bus standard. The SSIs interface to the AUDMUX for flexible audio routing.
UART(3)	Universal asynchronous receiver/transmitters	ARM (UART1,2) SDMA (UART3)	Connectivity peripherals	Each UART provides serial communication capability with external devices through an RS-232 cable using the standard RS-232 non-return-to-zero (NRZ) encoding format. Each module transmits and receives characters containing either 7 or 8 bits (program-selectable). Each UART can also provide low-speed IrDA compatibility through the use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission).
USBOH	High-speed USB on-the-go	SDMA	Connectivity peripherals	The USB module provides high performance USB on-the-go (OTG) functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 low pin count specification. The module has DMA capabilities handling data transfer between internal buffers and system memory.
WDOG	Watchdog modules	ARM	Timer peripherals	Each module protects against system failures by providing a method of escaping from unexpected events or programming errors. Once activated, the timer must be serviced by software on a periodic basis. If servicing does not take place, the watchdog times out and then either asserts a system reset signal or an interrupt request signal, depending on the software configuration.

¹ ARM = ARM1136 platform, SDMA = SDMA platform

3 Signal Descriptions: Special Function Related Pins

Some special functional requirements are supported in the device. The details about these special functions and the corresponding pin names are listed in [Table 4](#).

Table 4. Special Function Related Pins

Function Name	Pin Name	Mux Mode	Detailed Description
External ARM Clock	EXT_ARMCLK	ALT0	External clock input for ARM clock.
External Peripheral Clock	I2C1_CLK	ALT6	External peripheral clock source.
External 32-kHz Clock	CAPTURE	ALT4	External clock input of 32 kHz, used when the internal 24M Oscillator is powered off, which could be configured either from CAPTURE or CSPI1_SS1.
	CSPI1_SS1	ALT2	
Clock Out	CLKO	ALT0	Clock-out pin from CCM, clock source is controllable and can also be used for debug.
Power Ready	GPIO1_0	ALT1	PMIC power-ready signal, which can be configured either from GPIO1_0 or TX1.
	TX1	ALT1	
Tamper Detect	GPIO1_1	ALT6	Tamper-detect logic is used to issue a security violation. This logic is activated if the tamper-detect input is asserted. Tamper-detect logic is enabled by the bit of IOMUXC_GPRA[2]. After enabling the logic, it is impossible to disable it until the next reset.

4 Electrical Characteristics

The following sections provide the device-level and module-level electrical characteristics for the i.MX35 processor.

4.1 i.MX35 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See [Table 5](#) for a quick reference to the individual tables and sections.

Table 5. i.MX35 Chip-Level Conditions

Characteristics	Table/Location
Absolute Maximum Ratings	Table 6 on page 12
i.MX35 Operating Ranges	Table 7 on page 12
Interface Frequency	Table 8 on page 13

CAUTION

Stresses beyond those listed in [Table 6](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in [Table 7](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (core)	$V_{DD_{max}}$ ¹	-0.5	1.47	V
Supply voltage (I/O)	$NVCC_{max}$	-0.5	3.6	V
Input voltage range	$V_{I_{max}}$	-0.5	3.6	V
Storage temperature	$T_{storage}$	-40	125	°C
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000 ²	
Charge Device Model (CDM)		—	500 ³	

¹ VDD is also known as QVCC.

² HBM ESD classification level according to the AEC-Q100-002 standard

³ Corner pins max. 750 V

4.1.1 i.MX35 Operating Ranges

[Table 7](#) provides the recommended operating ranges. The term NVCC in this section refers to the associated supply rail of an input or output.

Table 7. i.MX35 Operating Ranges

Parameter	Symbol	Min.	Typical	Max.	Units
Core Operating Voltage $0 < f_{ARM} < 400$ MHz	V_{DD}	1.22	—	1.47	V
Core Operating Voltage $0 < f_{ARM} < 532$ MHz		1.33	—	1.47	V
State Retention Voltage		1	—	—	V
EMI ¹	$NVCC_{EMI1,2,3}$	1.7	—	3.6	V
WTDG, Timer, CCM, CSPI1	$NVCC_{CRM}$	1.75	—	3.6	V
NANDF	$NVCC_{NANDF}$	1.75	—	3.6	V
ATA, USB generic	$NVCC_{ATA}$	1.75	—	3.6	V
eSDHC1	$NVCC_{SDIO}$	1.75	—	3.6	V
CSI, SDIO2	$NVCC_{CSI}$	1.75	—	3.6	V
JTAG	$NVCC_{JTAG}$	1.75	—	3.6	V
LCDC, TTM, I2C1	$NVCC_{LCDC}$	1.75	—	3.6	V

Table 7. i.MX35 Operating Ranges (continued)

Parameter	Symbol	Min.	Typical	Max.	Units
I2Sx2,ESAI, I2C2, UART2, UART1, FEC	NVCC_MISC	1.75	—	3.6	V
MLB	NVCC_MLB ²	1.75	—	3.6	V
USB OTG PHY	PHY1_VDDA	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_VDDA_BIAS	3.17	3.3	3.43	V
USB OTG PHY	USBPHY1_UPLLVD	3.17	3.3	3.43	V
USB HOST PHY	PHY2_VDD	3.0	3.3	3.6	V
OSC24M	OSC24M_VDD	3.0	3.3	3.6	V
OSC_AUDIO	OSC_AUDIO_VDD	3.0	3.3	3.6	V
MPLL	MVDD	1.4	—	1.65	V
PPLL	PVDD	1.4	—	1.65	V
Fusebox program supply voltage	FUSE_VDD ³	3.0	3.6	3.6	V
Operating Ambient Temperature Range	TA	-20	—	70	°C
Operating Ambient Temperature Range	TA	-40	—	85	°C

¹ EMI I/O interface power supply should be set up according to external memory. For example, if using SDRAM then NVCC_EMI1,2,3 should all be set at 3.3 V (typ.). If using MDDR or DDR2, NVCC_EMI1,2,3 must be set at 1.8 V (typ.).

² MLB Interface I/O pins can be programmed to function as GPIO for the consumer and industrial parts by setting NVCC_MLB to 1.8 or 3.3 V. NVCC_MLB can be left floating.

³ The Fusebox read supply is connected to supply of the full speed USB PHY. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. FUSE_VDD should be supplied by following the power up sequence given in [Section 4.3.1, “Powering Up.”](#)

4.1.2 Interface Frequency Limits

[Table 8](#) provides information on interface frequency limits.

Table 8. Interface Frequency

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
1	JTAG TCK Frequency	f _{JTAG}	DC	5	10	MHz

4.2 Power Modes

Table 9 provides descriptions of the power modes of the i.MX35 processor.

Table 9. i.MX35 Power Modes

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDIO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Wait	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is active. L2 cache is kept powered. MCU PLL is on (400 MHz) PER PLL is off (can be configured) (default: 300 MHz) Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured). RNGC internal osc is off.	16 mA	—	7.2 mA	—	1.2 mA	—
Doze	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted. L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is on(400 MHz) PER PLL is off (can be configured). (300 Mhz). Module clocks are gated off (can be configured by CGR register). OSC 24M is ON. OSC audio is off (can be configured) RNGC internal osc is off	12.4 mA	—	7.2 mA	—	1.2 mA	—
Stop	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24 MHz is on OSC audio is off RNGC internal osc is off	1.1 mA	—	400 μ A	—	1.2 mA	—

Table 9. i.MX35 Power Modes (continued)

Power Mode	Description	QVCC (ARM/L2 Peripheral)		MVDD/PVDD		OSC24M_VDD OSC_AUDIO_VDD	
		Typ.	Max.	Typ.	Max.	Typ.	Max.
Static	VDD1,2,3,4 = 1.1 V (min.) ARM is in wait for interrupt mode. MAX is halted L2 cache is kept powered. L2 cache control logic off. AWB enabled. MCU PLL is off. PER PLL is off. All clocks are gated off. OSC 24MHz is on OSC audio is off RNGC internal osc is off	820 μ A	—	50 μ A	—	24 μ A	—
Note: Typical column: TA = 25 °C							

4.3 Supply Power-Up/Power-Down Requirements and Restrictions

This section provides power-up and power-down sequence guidelines for the i.MX35 processor.

CAUTION

Any i.MX35 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences can result in irreversible damage to the i.MX35 processor (worst-case scenario).

NOTE

Deviation from these sequences may also result in one or more of the following:

- Excessive current during power-up phase
- Prevent the device from booting
- Programming of unprogrammed fuses

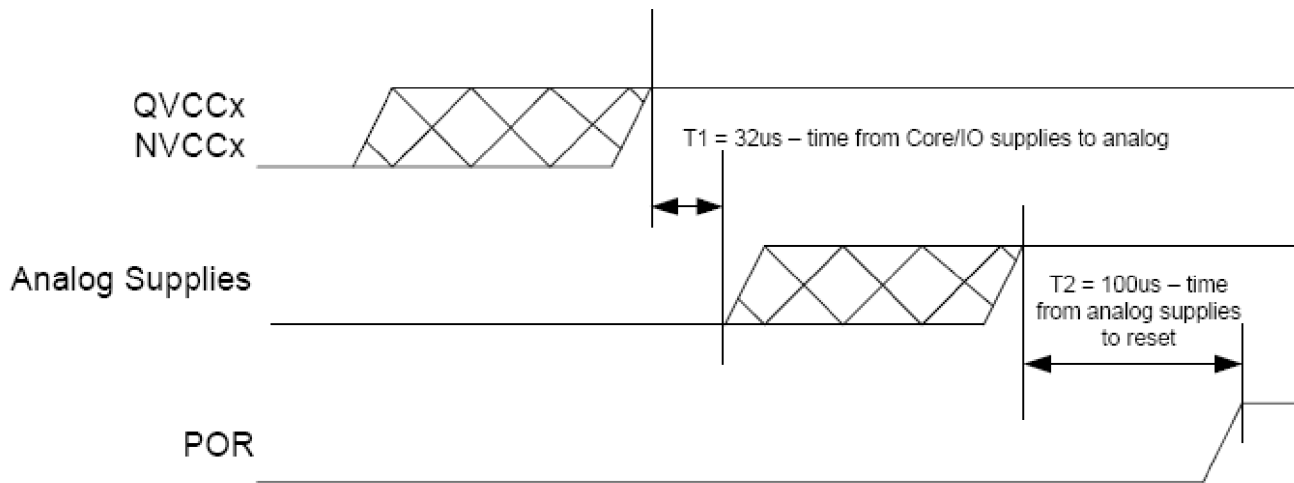
4.3.1 Powering Up

The power-up sequence should be completed as follows:

1. Assert Power on Reset ($\overline{\text{POR}}$).
2. Turn on digital logic domain and IO power supply: VDD $_n$, NVCC $_x$
3. Wait until VDD $_n$ and NVCC $_x$ power supplies are stable + 32 μ s.

4. Turn on all other power supplies: PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, FUSEVDD. (Always FUSE_VDD should be connected to ground, except when eFuses are to be programmed.)
5. Wait until PHY1_VDDA, USBPHY1_VDDA_BIAS, PHY2_VDD, USBPHY1_UPLLVD, OSC24M_VDD, OSC_AUDIO_VDD, MVDD, PVDD, (FUSEVDD, optional). Power supplies are stable + 100 μ s.
6. Deassert the $\overline{\text{POR}}$ signal.

Figure 2 shows the power-up sequence and timing.



Analog supplies include the following:
 PHY1_VDDA, USBPHY1_VDDA_BIAS,
 PHY2_VDD, USBPHY1_UPLLVD,
 OSC24M_VDD, OSC_AUDIO_VDD,
 MVDD, PVDD, FUSEVDD.
 Note: FUSEVDD shall be tied to GND if
 not programming fuse

Figure 2. i.MX35 Power-Up Sequence and Timing

4.3.2 Powering Down

The power-up sequence in reverse order is recommended for powering down. However, all power supplies can be shut down at the same time.

4.4 Reset Timing

There are two ways of resetting the i.MX35 using external pins:

- Power On Reset (using the POR_B pin)

- System Reset (using the RESET_IN_B pin)

4.4.1 Power On Reset

POR_B is normally connected to a power management integrated circuit (PMIC). The PMIC asserts POR_B while the power supplies are turned on and negates POR_B after the power up sequence is finished. See [Figure 2](#).

Assuming the i.MX35 chip is already fully powered; it is still possible to reset all of the modules to their default reset by asserting POR_B for at least 4 CKIL cycles and later de-asserting POR_B. This method of resetting the i.MX35 can also be supported by tying the POR_B and RESET_IN_B pins together.

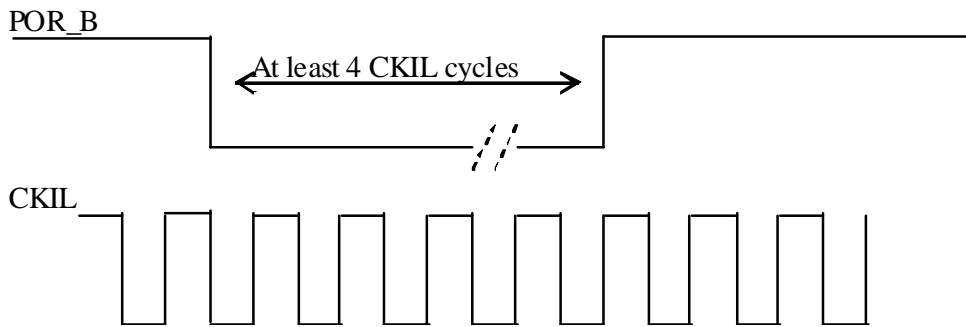


Figure 3. Timing Between POR_B and CKIL for Complete Reset of i.MX35

4.4.2 System Reset

System reset can be achieved by asserting RESET_IN_B for at least 4 CKIL cycles and later negating RESET_IN_B. The following modules are not reset upon system reset: RTC, PLLs, CCM, and IIM. POR_B pin must be deasserted all the time.

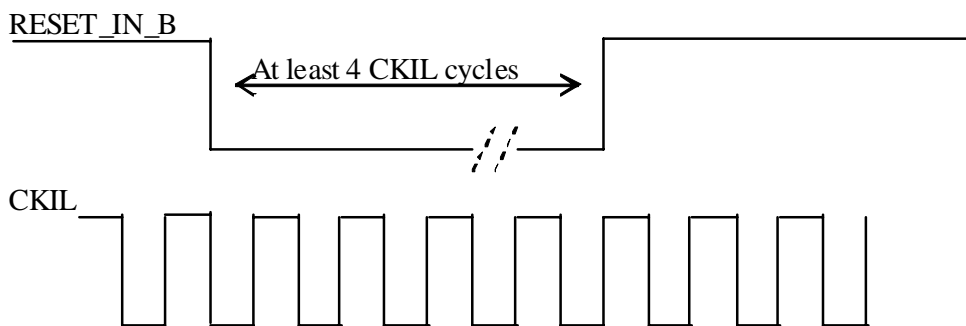


Figure 4. Timing Between RESET_IN_B and CKIL for i.MX35 System Reboot

4.5 Power Characteristics

The table shows values representing maximum current numbers for the i.MX35 under worst case voltage and temperature conditions. These values are derived from the i.MX35 with core clock speeds up to

532 MHz. Common supplies have been bundled according to the i.MX35 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX35 power supply requirements will be satisfied during startup and transient conditions. Freescale recommends that system current measurements be taken with customer-specific use-cases to reflect normal operating conditions in the end system.

Table 10. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVCC	1.47	400
MVDD, PVDD	1.65	20
NVCC_EMI1, NVCC_EMI2, NVCC_EMI3, NVCC_LCDC, NVCC_NFC	1.9	90
FUSE_VDD ¹	3.6	62
NVCC_MISC, NVCC_CSI, NVCC_SDIO, NVCC_CRM, NVCC_ATA, NVCC_MLB, NVCC_JTAG	3.6	60
OSC24M_VDD, OSC_AUDIO_VDD, PHY1_VDDA, PHY2_VDD, USBPHY1_UPLLVD, USBPHY1_VDDA_BIAS	3.6	25

¹ This rail is connected to ground; it only needs a voltage if eFuses are to be programmed. FUSE_VDD should be supplied by following the power up sequence given in [Section 4.3.1, "Powering Up."](#)

The method for obtaining max current is as follows:

1. Measure worst case power consumption on individual rails using directed test on i.MX35.
2. Correlate worst case power consumption power measurements with worst case power consumption simulations.
3. Combine common voltage rails based on power supply sequencing requirements
4. Guard band worst case numbers for temperature and process variation. Guard band is based on process data and correlated with actual data measured on i.MX35.
5. The sum of individual rails is greater than real world power consumption, as a real system does not typically maximize power consumption on all peripherals simultaneously.

4.6 Thermal Characteristics

The thermal resistance characteristics for the device are given in [Table 11](#). These values were measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core via I.D: 0.168 mm, Core via plating 0.016 mm.
- Full array map design, but nearly all balls under die are power or ground.
- Die Attach: 0.033 mm non-conductive die attach, $k = 0.3 \text{ W/m K}$
- Mold compound: $k = 0.9 \text{ W/m K}$

Table 11. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient ¹ natural convection	Single layer board (1s)	R _{eJA}	53	°C/W
Junction to ambient ¹ natural convection	Four layer board (2s2p)	R _{eJA}	30	°C/W
Junction to ambient ¹ (at 200 ft/min)	Single layer board (1s)	R _{eJMA}	44	°C/W
Junction to ambient ¹ (at 200 ft/min)	Four layer board (2s2p)	R _{eJMA}	27	°C/W
Junction to boards ²	—	R _{eJB}	19	°C/W
Junction to case (top) ³	—	R _{eJCTop}	10	°C/W
Junction to package top ⁴	Natural convection	Ψ _{JT}	2	°C/W

¹ Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

² Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for this package.

³ Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

⁴ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

4.7 I/O Pin DC Electrical Characteristics

I/O pins are of two types: GPIO and DDR. DDR pins can be configured in three different drive strength modes: mobile DDR, SDRAM, and DDR2. The SDRAM and mobile DDR modes can be further customized at three drive strength levels: normal, high, and max.

Table 12 shows currents for the different DDR pin drive strength modes.

Table 12. DDR Pin Drive Strength Mode Current Levels

Drive Mode	Normal	High	Max.
Mobile DDR (1.8 V)	3.6 mA	7.2 mA	10.8 mA
SDRAM (1.8 V)	—	—	6.5 mA
SDRAM (3.3 V)	4 mA	8 mA	12 mA
DDR2 (1.8 V)	—	—	13.4 mA

Table 13 shows the DC electrical characteristics for GPIO, DDR2, mobile DDR, and SDRAM pins. The term NVCC refers to the power supply voltage that feeds the I/O of the module in question. For example, NVCC for the SD/MMC interface refers to NVCC_SDIO.

Table 13. I/O Pin DC Electrical Characteristics

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
GPIO	High-level output voltage	Voh	Ioh = -1 mA Ioh = specified drive	NVCC - 0.15 0.8 × NVCC	—	—	V
	Low-level output voltage	Vol	Iol = 1 mA Iol = specified drive	—	—	0.15 0.2 × NVCC	V
	High-level output current for slow mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	-2.0 -4.0 -8.0	—	—	mA
	High-level output current for fast mode (Voh = 0.8 × NVCC)	Ioh	Standard drive High drive Max. drive	-4.0 -6.0 -8.0	—	—	mA
	Low-level output current for slow mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	2.0 4.0 8.0	—	—	mA
	Low-level output current for fast mode (Voh = 0.2 × NVCC)	Iol	Standard drive High drive Max. drive	4.0 6.0 8.0	—	—	mA
	High-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIH	—	0.7 × NVCC	—	NVCC	V
	Low-level DC Input Voltage with 1.8 V, 3.3 V NVCC (for digital cells in input mode)	VIL	—	-0.3 V	—	0.3 × NVCC	V
	Input Hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8 V	—	410 330	—	mV
	Schmitt trigger VT+	VT+	—	0.5 × NVCC	—	—	V
	Schmitt trigger VT-	VT-	—	—	—	0.5 × NVCC	V
	Pull-up resistor (22 kΩ PU)	Rpu	Vi = 0	—	22	—	kΩ
	Pull-up resistor (47 kΩ PU)	Rpu	Vi = 0	—	47	—	kΩ
	Pull-up resistor (100 kΩ PU)	Rpu	Vi = 0	—	100	—	kΩ
	Pull-down resistor (100 kΩ PD)	Rpd	Vi = NVCC	—	100	—	kΩ
External resistance to pull keeper up when enabled	Rkpu	Ipu > 620μA @ min Vddio = 3.0 V	—	—	4.8	kΩ	
External resistance to pull keeper down when enabled	Rkpd	Ipd > 510μA @ min Vddio = 3.0 V	—	—	5.9	kΩ	

Table 13. I/O Pin DC Electrical Characteristics (continued)

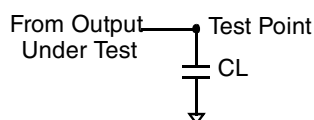
Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
DDR2	High-level output voltage	Voh	—	NVCC – 0.28	—	—	V	
	Low-level output voltage	Vol	—	—	—	0.28	V	
	Output min. source current	Ioh	—	–13.4	—	—	mA	
	Output min. sink current	Iol	—	13.4	—	—	mA	
	DC input logic high	VIH(dc)	—	$NVCC \div 2 + 0.125$	—	$NVCC + 0.3$	V	
	DC input logic low	VIL(dc)	—	–0.3 V	—	$NVCC \div 2 - 0.125$	V	
	DC input signal voltage (for differential signal)	Vin(dc)	—	–0.3	—	$NVCC + 0.3$	V	
	DC differential input voltage	Vid(dc)	—	0.25	—	$NVCC + 0.6$	V	
	Termination voltage	Vtt	—	$NVCC \div 2 - 0.04$	$NVCC \div 2$	$NVCC \div 2 + 0.04$	V	
	Input current (no pull-up/down)	IIN	—	—	—	±1	µA	
	Tri-state I/O supply current	Icc – NVCC	—	—	—	±1	µA	
Mobile DDR	High-level output voltage	—	I _{OH} = –1mA I _{OH} = specified drive	$NVCC - 0.08$ $0.8 \times NVCC$	—	—	V	
	Low-level output voltage	—	I _{OL} = 1mA I _{OL} = specified drive	—	—	0.08 $0.2 \times NVCC$	V	
	High-level output current (Voh = 0.8 × NVCCV)	—	Standard drive High drive Max. drive	–3.6 –7.2 –10.8	—	—	mA	
	Low-level output current (Vol = 0.2 × NVCCV)	—	Standard Drive High Drive Max. Drive	3.6 7.2 10.8	—	—	mA	
	High-Level DC CMOS input voltage	VIH	—	$0.7 \times NVCC$	—	$NVCC + 0.3$	V	
	Low-Level DC CMOS input voltage	VIL	—	–0.3	—	$0.2 \times NVCC$	V	
	Differential receiver VTH+	VTH+	—	—	—	100	mV	
	Differential receiver VTH–	VTH–	—	–100	—	—	mV	
	Input current (no pull-up/down)	IIN	—	VI = 0 VI = NVCC	—	—	±1	µA
	Tri-state I/O supply current	Icc – NVCC	—	VI = NVCC or 0	—	—	±1	µA

Table 13. I/O Pin DC Electrical Characteristics (continued)

Pin	DC Electrical Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SDR (1.8 V)	High-level output voltage	Voh	loh = 5.7 mA	OVDD – 0.28	—	—	V
	Low-level output voltage	Vol	loh = 5.7 mA	—	—	0.4	V
	High-level output current	loh	Max. drive	5.7	—	—	mA
	Low-level output current	lol	Max. drive	7.3	—	—	mA
	High-level DC Input Voltage	VIH	—	1.4	—	1.98	V
	Low-level DC Input Voltage	VIL	—	–0.3	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	150 80	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = OVDD or 0	—	—	1180	μA
	Tri-state core supply current	Icc (NVCC)	VI = VDD or 0	—	—	1220	μA
SDR (3.3 V)	High-level output voltage	Voh	loh=specified drive (loh = –4, –8, –12, –16 mA)	2.4	—	—	V
	Low-level output voltage	Vol	loh=specified drive (loh = 4, 8, 12, 16 mA)	—	—	0.4	V
	High-level output current	loh	Standard drive High drive Max. drive	–4.0 –8.0 –12.0	—	—	mA
	Low-level output current	lol	Standard drive High drive Max. drive	4.0 8.0 12.0	—	—	mA
	High-level DC Input Voltage	VIH	—	2.0	—	3.6	V
	Low-level DC Input Voltage	VIL	—	–0.3V	—	0.8	V
	Input current (no pull-up/down)	IIN	VI = 0 VI = NVCC	—	—	±1	μA
	Tri-state I/O supply current	Icc (NVCC)	VI = NVCC or 0	—	—	±1	μA

4.8 I/O Pin AC Electrical Characteristics

Figure 5 shows the load circuit for output pins.



CL includes package, probe and jig capacitance

Figure 5. Load Circuit for Output Pin

Figure 6 shows the output pin transition time waveform.

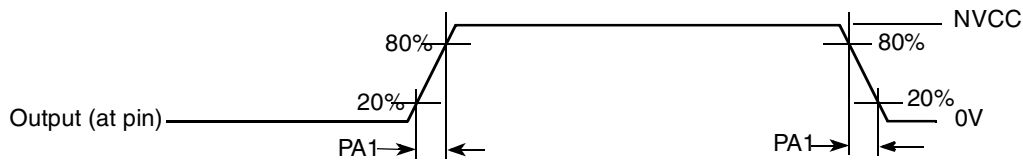


Figure 6. Output Pin Transition Time Waveform

4.8.1 AC Electrical Test Parameter Definitions

AC electrical characteristics in Table 14 through Table 19 are not applicable for the output open drain pull-down driver.

The dI/dt parameters are measured with the following methodology:

- The zero voltage source is connected between pin and load capacitance.
- The current (through this source) derivative is calculated during output transitions.

Table 14. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode
[NVCC = 3.0 V–3.6 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.79/1.12 0.49/0.73	1.30/1.77 0.84/1.23	2.02/2.58 1.19/1.58	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.48/0.72 0.27/0.42	0.76/1.10 0.41/0.62	1.17/1.56 0.63/0.86	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.25/0.40 0.14/0.21	0.40/0.59 0.21/0.32	0.60/0.83 0.32/0.44	V/ns
Output pin dI/dt (max. drive)	tdit	25 pF 50 pF	15 16	36 38	76 80	mA/ns
Output pin dI/dt (high drive)	tdit	25 pF 50 pF	8 9	20 21	45 47	mA/ns
Output pin dI/dt (standard drive)	tdit	25 pF 50 pF	4 4	10 10	22 23	mA/ns

Table 15. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode
[NVCC = 1.65 V–1.95 V]

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.30/0.42 0.20/0.29	0.54/0.73 0.35/0.50	0.91/1.20 0.60/0.80	V/ns

**Table 15. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode
[NVCC = 1.65 V–1.95 V] (continued)**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.19/0.28 0.12/0.18	0.34/0.49 0.34/0.49	0.58/0.79 0.36/0.49	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.12/0.18 0.07/0.11	0.20/0.30 0.11/0.17	0.34/0.47 0.20/0.27	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	21 22	56 58	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	5 5	14 15	38 40	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	2 2	7 7	18 19	mA/ns

**Table 16. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode for
[NVCC = 3.0 V–3.6 V]**

Parameter	Symbol	Test Condition	Min. rise/fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	22 23	52 55	116 121	mA/ns

**Table 17. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode
[NVCC = 1.65 V–1.95 V]**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.40/0.57 0.25/0.36	0.72/0.97 0.43/0.61	1.2/1.5 0.72/0.95	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.38/0.48 0.20/0.30	0.59/0.81 0.34/0.50	0.98/1.27 0.56/0.72	V/ns

**Table 17. AC Electrical Characteristics, GPIO Pins in Fast Slew Rate Mode
[NVCC = 1.65 V–1.95 V] (continued)**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.23/0.32 0.13/0.20	0.40/0.55 0.23/0.34	0.66/0.87 0.38/0.52	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns

**Table 18. AC Electrical Characteristics of GPIO Pins in Slow Slew Rate Mode
[NVCC = 2.25 V–2.75 V]**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	—	60	%
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.63/0.85 0.52/0.67 0.41/0.59	1.10/1.40 0.90/1.10 0.73/0.99	1.86/2.20 1.53/1.73 1.20/1.50	V/ns
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.40/0.58 0.33/0.43 0.25/0.37	0.71/0.98 0.56/0.70 0.43/0.60	1.16/1.40 0.93/1.07 0.68/0.90	V/ns
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.19/0.25 0.13/0.21	0.41/0.59 0.32/0.35 0.23/0.33	0.66/0.87 0.51/0.59 0.36/0.48	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	22 23	62 65	148 151	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	15 16	42 44	102 107	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	7 8	21 22	52 54	mA/ns

**Table 19. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode
[NVCC = 2.25 V–2.75 V]**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Duty cycle	Fduty	—	40	—	60	%	—

**Table 19. AC Electrical Characteristics of GPIO Pins in Fast Slew Rate Mode
[NVCC = 2.25 V–2.75 V] (continued)**

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units	Notes
Output pin slew rate (max. drive)	tps	25 pF 40 pF 50 pF	0.84/1.10 0.68/0.83 0.58/0.72	1.45/1.80 1.14/1.34 0.86/1.10	2.40/2.80 1.88/2.06 1.40/1.70	V/ns	2
Output pin slew rate (high drive)	tps	25 pF 40 pF 50 pF	0.69/0.96 0.55/0.69 0.40/0.59	1.18/1.50 0.92/1.10 0.67/0.95	1.90/2.30 1.49/1.67 1.10/1.30	V/ns	
Output pin slew rate (standard drive)	tps	25 pF 40 pF 50 pF	0.24/0.36 0.37/0.47 0.13/0.21	0.80/1.00 0.62/0.76 0.45/0.65	1.30/1.60 1.00/1.14 0.70/0.95	V/ns	
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	46 49	124 131	310 324	mA/ns	3
Output pin di/dt (high drive)	tdit	25 pF 50 pF	33 35	89 94	290 304	mA/ns	
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	28 29	75 79	188 198	mA/ns	

4.8.2 AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)

Table 20. AC Electrical Characteristics of DDR Type IO Pins in DDR2 Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate	tps	25 pF 50 pF	0.86/0.98 0.46/0.54	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pin di/dt	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns

Table 21. AC Requirements of DDR2 Pins

Parameter ¹	Symbol	Min.	Max.	Units
AC input logic high	V _{IH(ac)}	NVCC ÷ 2 + 0.25	NVCC + 0.3	V
AC input logic low	V _{IL(ac)}	–0.3	NVCC ÷ 2 – 0.25	V
AC differential cross point voltage for output ²	V _{ox(ac)}	NVCC ÷ 2 – 0.125	NVCC ÷ 2 + 0.125	V

¹ The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

² The typical value of V_{ox(ac)} is expected to be about 0.5 × NVCC and V_{ox(ac)} is expected to track variation in NVCC. V_{ox(ac)} indicates the voltage at which the differential output signal must cross. Clload = 25 pF.

Table 22. AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	45	50	55	%
Clock frequency	f	—	—	133	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns

Table 23. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode

Parameter	Symbol	Test Condition	Min. Rise/Fall	Min. Clock Frequency	Max. Rise/Fall	Units
Clock frequency	f	—	—	125	—	MHz
Output pin slew rate (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pin slew rate (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns
Output pin slew rate (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pin di/dt (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pin di/dt (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pin di/dt (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns

Table 24. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Clock frequency	f	—	125	—	—	MHz
Output pin slew rate (max. drive) ¹	tps	25 pF 50 pF	2.83/2.68 1.59/1.49	1.84/1.85 1.03/1.05	1.21/1.40 0.70/0.75	V/ns

Table 24. AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V) (continued)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pin di/dt (max. drive) ²	didt	25 pF 50 pF	89 95	202 213	435 456	mA/ns
Input pin transition times ³	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pin propagation delay, 50%–50%	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pin propagation delay, 40%–60%	tpi	1.0 pF	1.18/1.99	1.45/2.35	1.97/2.85	ns

¹ Min. condition for tps: wcs model, 1.1 V, IO 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

² Max. condition for didt: bcs model, 1.3 V, IO 1.95 V, and –40 °C.

³ Max. condition for tpi and trfi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Min. condition for tpi and trfi: bcs model, 1.3 V, IO 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

4.9 Module-Level AC Electrical Specifications

This section contains the AC electrical information (including timing specifications) for the modules of the i.MX35. The modules are listed in alphabetical order.

4.9.1 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. See the electrical specification for SSI.

4.9.2 CSPI AC Electrical Specifications

The i.MX35 provides two CSPI modules. CSPI ports are multiplexed in the i.MX35 with other pins. See the “External Signals and Multiplexing” chapter of the reference manual for more details.

Figure 7 and Figure 8 depict the master mode and slave mode timings of the CSPI, and Table 25 lists the timing parameters.

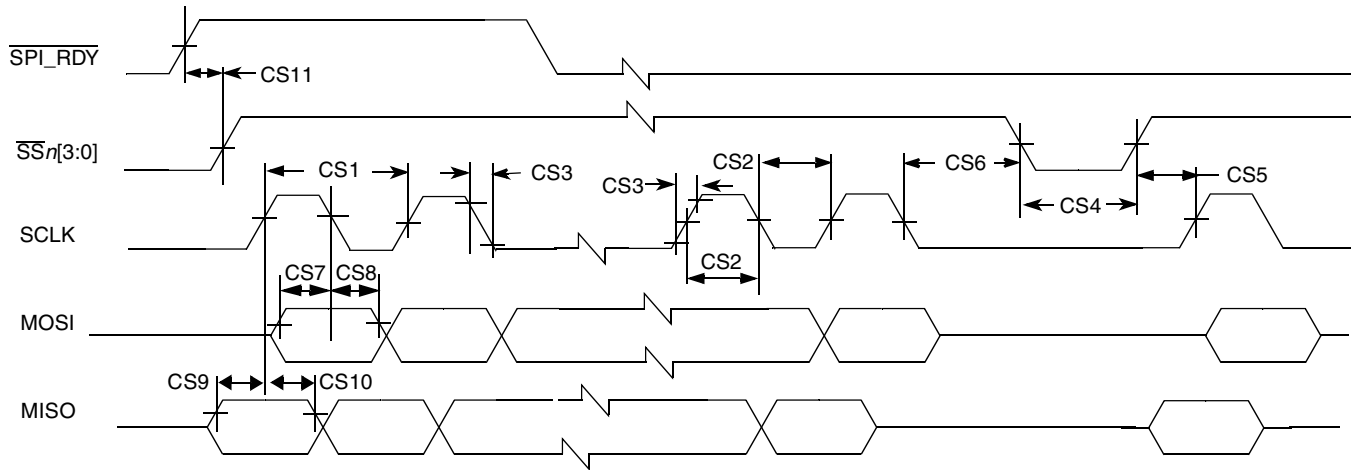


Figure 7. CSPI Master Mode Timing Diagram

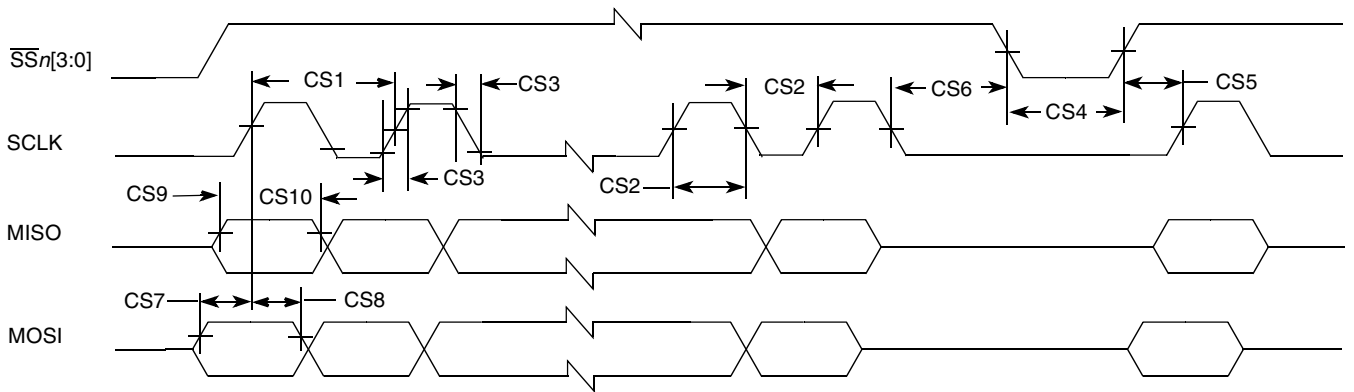


Figure 8. CSPI Slave Mode Timing Diagram

Table 25. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
CS1	SCLK cycle time	t_{clk}	60	—	ns
CS2	SCLK high or low time	t_{sw}	30	—	ns
CS3	SCLK rise or fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	$\overline{SSn[3:0]}$ pulse width	t_{CSLH}	30	—	ns
CS5	$\overline{SSn[3:0]}$ lead time (CS setup time)	t_{SCS}	30	—	ns
CS6	$\overline{SSn[3:0]}$ lag time (CS hold time)	t_{HCS}	30	—	ns
CS7	MOSI setup time	t_{Smosi}	5	—	ns
CS8	MOSI hold time	t_{Hmosi}	5	—	ns
CS9	MISO setup time	t_{Smiso}	5	—	ns

Table 25. CSPI Interface Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
CS10	MISO hold time	t_{Hmiso}	5	—	ns
CS11	$\overline{SPI_RDY}$ setup time	t_{SDRY}	5	—	ns

4.9.3 DPLL Electrical Specifications

There are three PLLs inside the i.MX35, all based on the same PLL design. The reference clock for these PLLs is normally generated from an external 24-MHz crystal connected to an internal oscillator via EXTAL24M and XTAL24 pins. It is also possible to connect an external 24-MHz clock directly to EXTAL24M, bypassing the internal oscillator.

DPLL specifications are listed in [Table 26](#).

Table 26. DPLL Specifications

Parameter	Min.	Typ.	Max.	Unit	Comments
Reference clock frequency	10	24	100	MHz	
Max. allowed reference clock phase noise	—	—	0.03 0.01 0.15	$2 T_{dck}^1$	Fmodulation < 50 kHz 50 kHz < Fmodulation 300 Hz Fmodulation > 300 KHz
Frequency lock time (FOL mode or non-integer MF)	—	—	80	μs	—
Phase lock time	—	—	100	μs	—
Max. allowed PL voltage ripple	—	—	150 100 150	mV	Fmodulation < 50 kHz 50 kHz < Fmodulation 300 Hz Fmodulation > 300 KHz

¹ There are two PLL are used in the i.MX35, MPLL and PPLL. Both are based on same DPLL design.

4.9.4 Embedded Trace Macrocell (ETM) Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a test point access (TPA) that supports TRACECLK frequencies up to 133 MHz.

[Figure 9](#) depicts the TRACECLK timings of ETM, and [Table 27](#) lists the timing parameters.

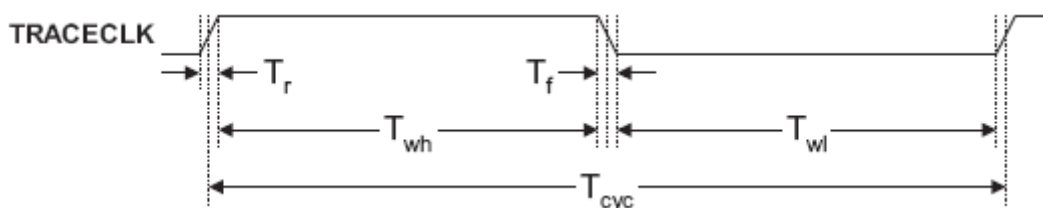


Figure 9. ETM TRACECLK Timing Diagram

Table 27. ETM TRACECLK Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 10 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 28 lists the timing parameters.

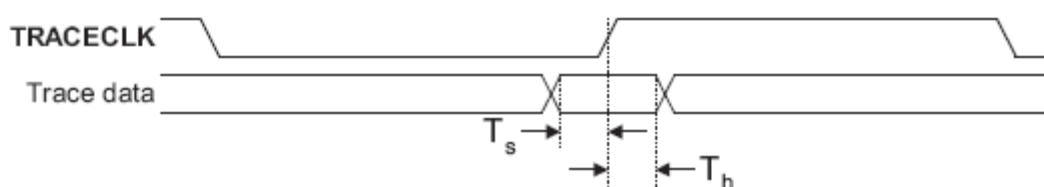


Figure 10. Trace Data Timing Diagram

Table 28. ETM Trace Data Timing Parameters

ID	Parameter	Min.	Max.	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.9.4.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 10. The same T_s and T_h parameters from Table 28 still apply with respect to the falling edge of the TRACECLK signal.

4.9.5 EMI Electrical Specifications

This section provides electrical parametrics and timing for the EMI module.

4.9.5.1 NAND Flash Controller Interface (NFC)

The i.MX35 NFC supports normal timing mode, using two flash clock cycles for one access of \overline{RE} and \overline{WE} . AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 11, Figure 12,

Figure 13, and Figure 14 depict the relative timing requirements among different signals of the NFC at module level for normal mode. Table 29 lists the timing parameters.

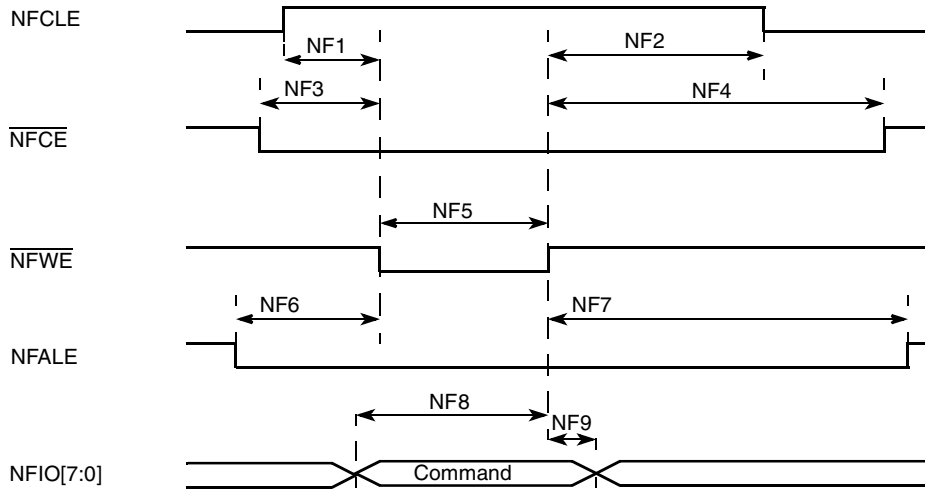


Figure 11. Command Latch Cycle Timing Diagram

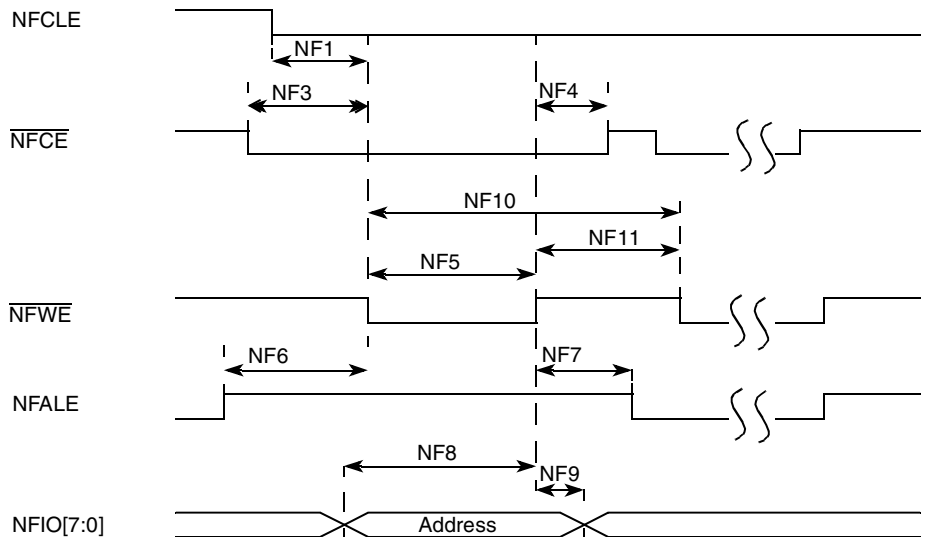


Figure 12. Address Latch Cycle Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

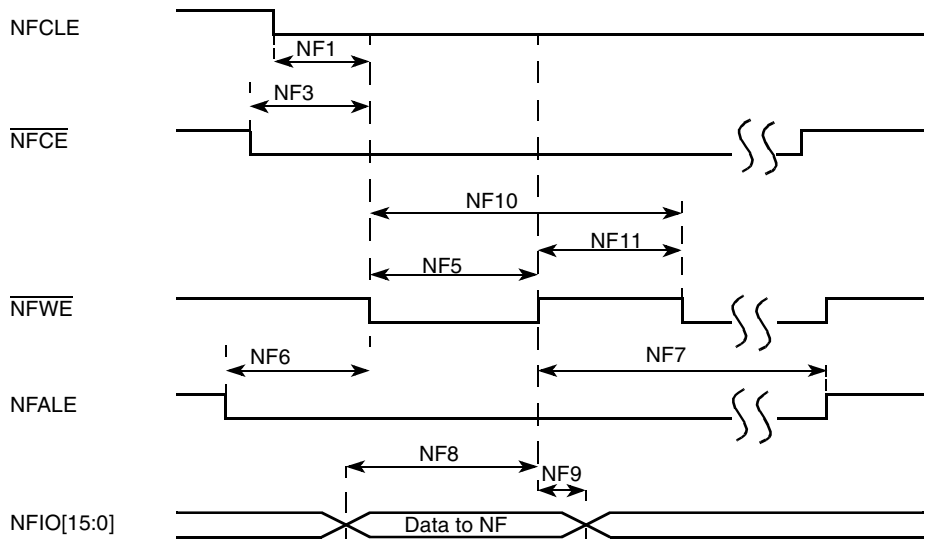


Figure 13. Write Data Latch Cycle Timing Diagram

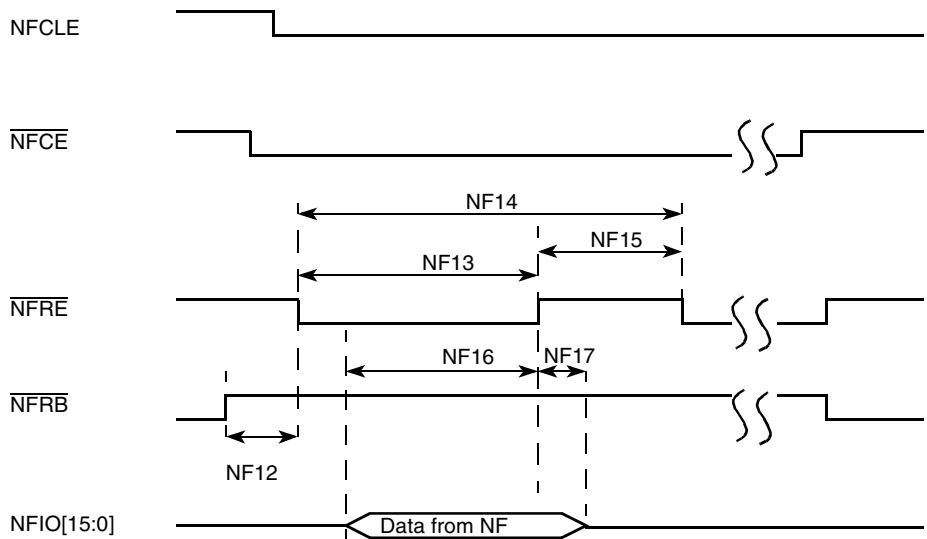


Figure 14. Read Data Latch Cycle Timing Diagram

Table 29. NFC Timing Parameters¹

ID	Parameter	Symbol	Timing T = NFC Clock Cycle ²		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T - 1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T - 2.0 ns	—	25	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	T - 1.0 ns	—	29	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	T - 2.0 ns	—	209	—	ns

Table 29. NFC Timing Parameters¹ (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle ²		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{\text{NF_WP}}$ pulse width	tWP	T – 1.5 ns		29.5		ns
NF6	NFALE setup time	tALS	T	—	30	—	ns
NF7	NFALE hold time	tALH	T – 3.0 ns	—	27.5	—	ns
NF8	Data setup time	tDS	T	—	30	—	ns
NF9	Data hold time	tDH	T – 5.0 ns	—	106	—	ns
NF10	Write cycle time	tWC	2T		59		ns
NF11	$\overline{\text{NFW\!E}}$ hold time	tWH	T – 2.5 ns		27		ns
NF12	Ready to $\overline{\text{NFRE}}$ low	tRR	6T	—	8400	—	ns
NF13	$\overline{\text{NFRE}}$ pulse width	tRP	1.5T	—	44.5	—	ns
NF14	READ cycle time	tRC	2T	—	58	—	ns
NF15	$\overline{\text{NFRE}}$ high hold time	tREH	0.5T – 2.5 ns		11	—	ns
NF16	Data setup on READ	tDSR	N/A		9	—	ns
NF17	Data hold on READ	tDHR	N/A		52	—	ns

¹ The flash clock maximum frequency is 50 MHz.

² Subject to DPLL jitter specification listed in [Table 26, "DPLL Specifications,"](#) on page 30.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

4.9.5.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clocks related to the BCLK rising edge or falling edge according to the corresponding assertion or negation control fields. The address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration.

Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 15 depicts the timing of the WEIM module, and Table 30 lists the timing parameters.

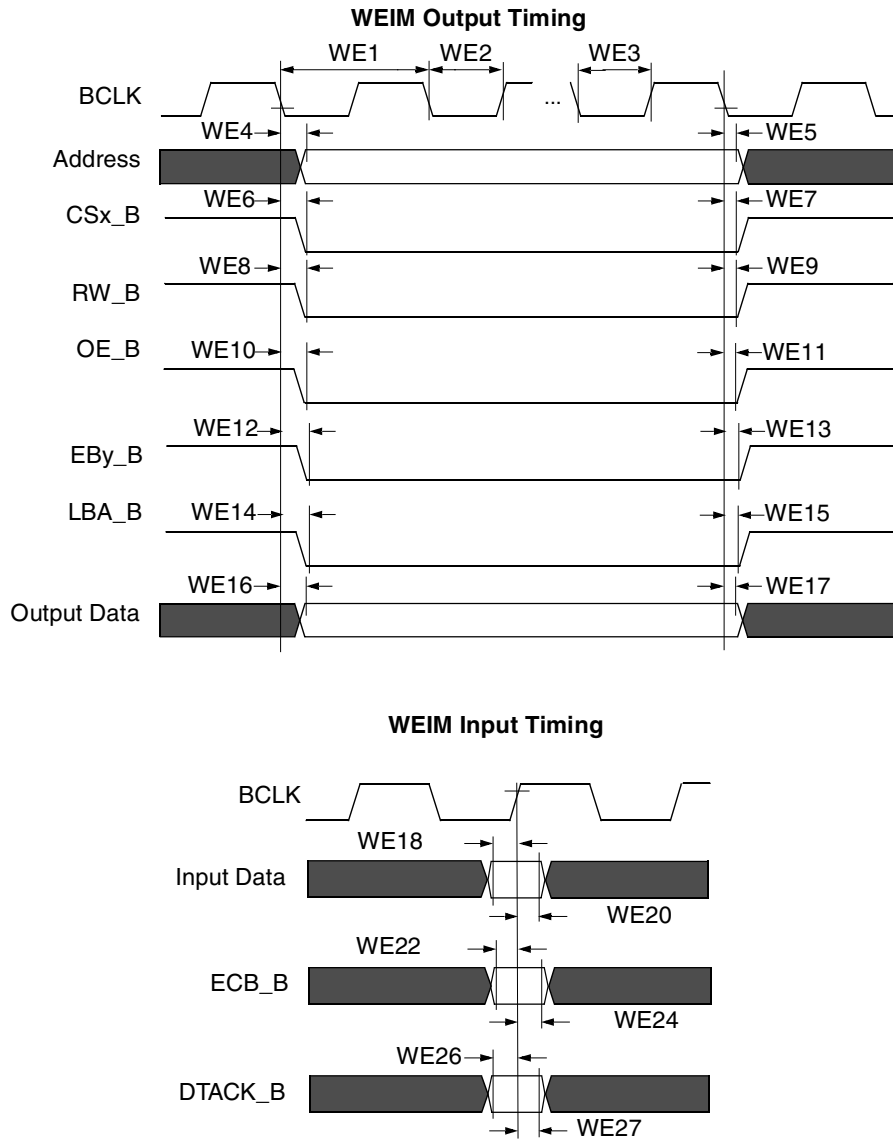


Figure 15. WEIM Bus Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

Table 30. WEIM Bus Timing Parameters¹

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time ²	14.5	—	ns
WE2	BCLK low-level width ²	7	—	ns
WE3	BCLK high-level width ²	7	—	ns
WE4	Clock fall to address valid	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to CSx_B valid	15	19	ns
WE7	Clock rise/fall to CSx_B invalid	3.6	5	ns
WE8	Clock rise/fall to RW_B valid	8	12	ns
WE9	Clock rise/fall to RW_B invalid	3	8	ns
WE10	Clock rise/fall to OE_B valid	7	12	ns
WE11	Clock rise/fall to OE_B invalid	3.8	5.5	ns
WE12	Clock rise/fall to EBy_B valid	6	11.5	ns
WE13	Clock rise/fall to EBy_B invalid	6	10	ns
WE14	Clock rise/fall to LBA_B valid	17.5	20	ns
WE15	Clock rise/fall to LBA_B invalid	0	1	ns
WE16	Clock rise/fall to Output Data valid	5	10	ns
WE17	Clock rise to Output Data invalid	0	2.5	ns
WE18	Input Data Valid to Clock rise ³	1	—	ns
WE20	Clock rise to Input Data invalid ³	1	—	ns
WE22	ECB_B setup time ³	5	—	ns
WE24	ECB_B hold time ³	0	—	ns
WE26	DTACK_B setup time	5.4	—	ns
WE27	DTACK_B hold time	-3.2	—	ns

¹ “High” is defined as 80% of signal value, and “low” is defined as 20% of signal value.

² BCLK parameters are measured from the 50% point. For example, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

³ Parameters W18, W20, W22, and W24 are tested when FCE=1. i.MX35 does not support FCE=0.

NOTE

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is set to maximum drive.

Recommended drive strength for all controls, address and BCLK is set to maximum drive.

Figure 16 through Figure 21 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 30 for specific control parameter settings.

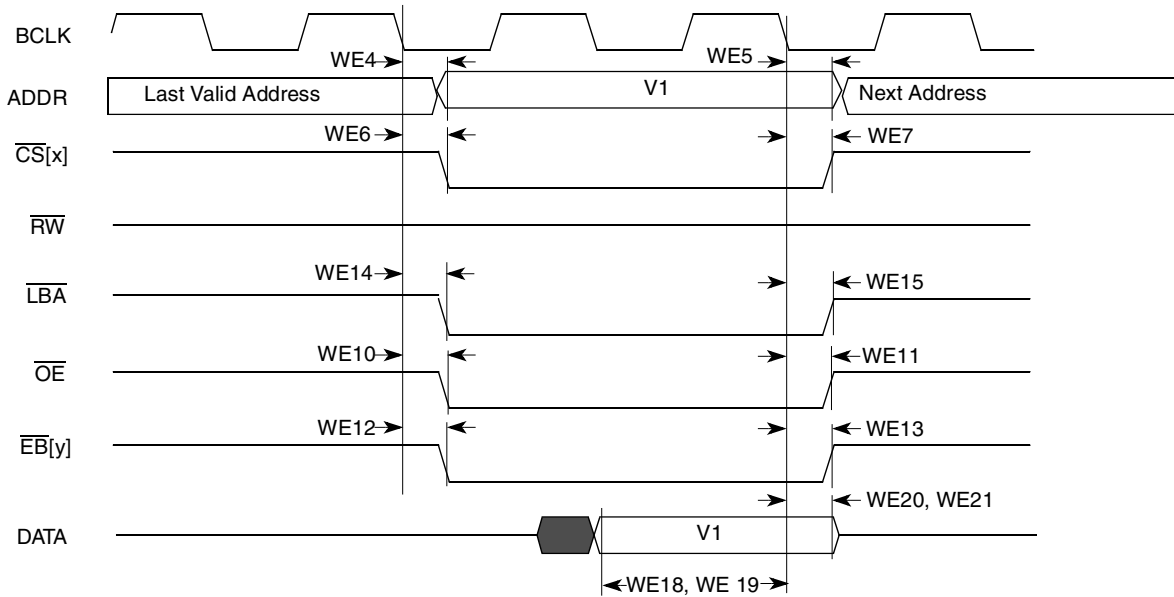


Figure 16. Synchronous Memory Timing Diagram for Read Access—WSC = 1

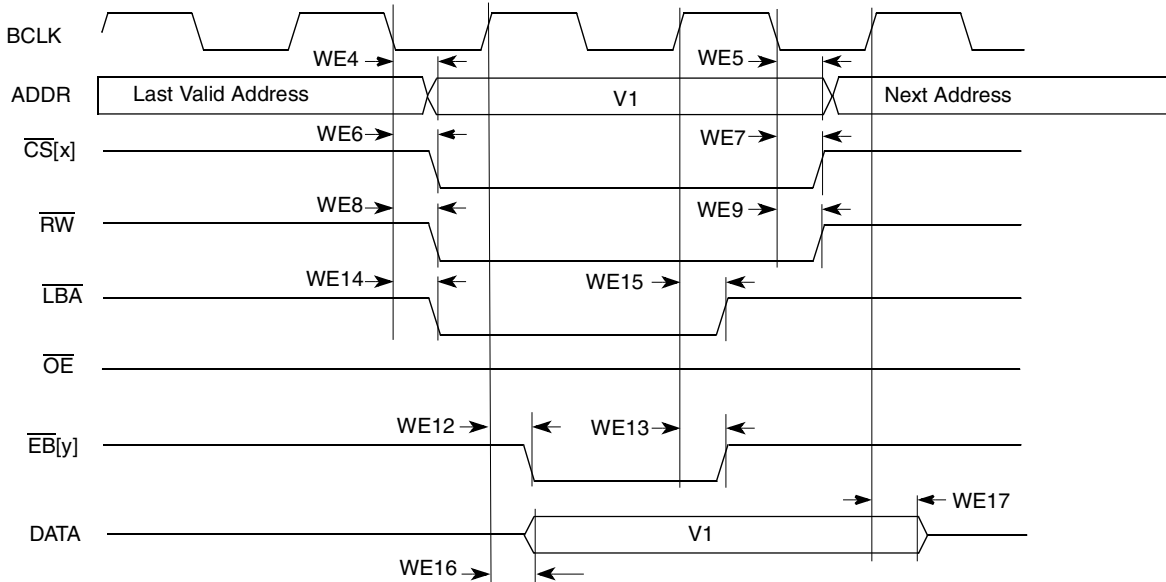
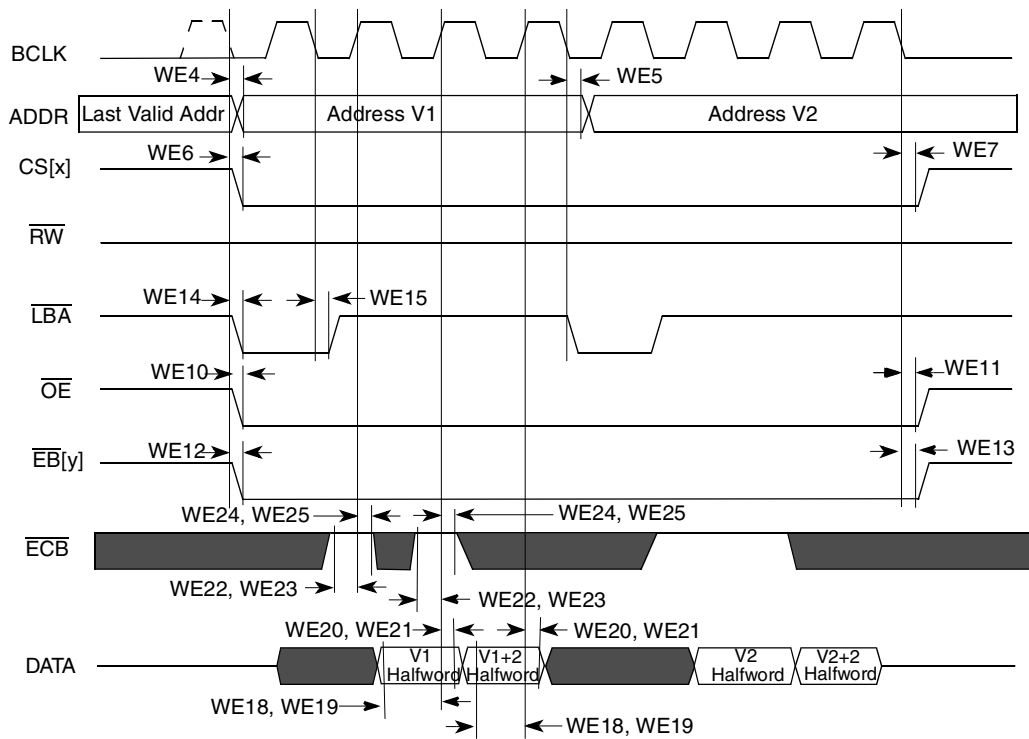
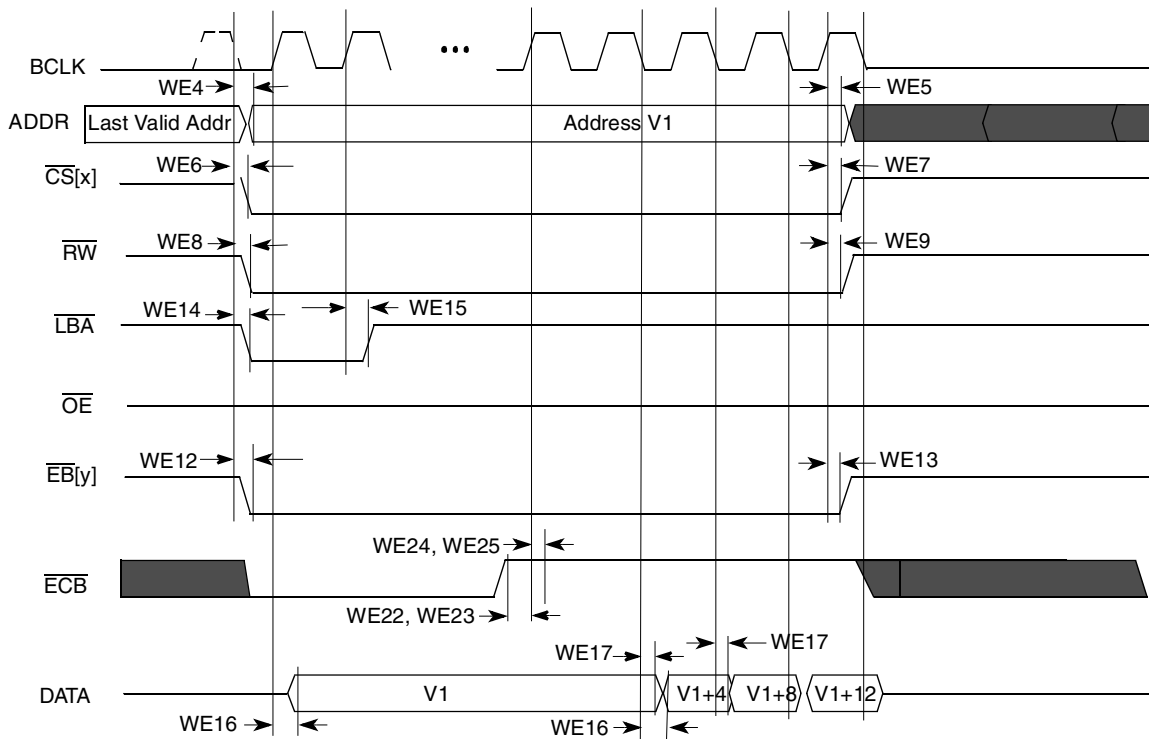


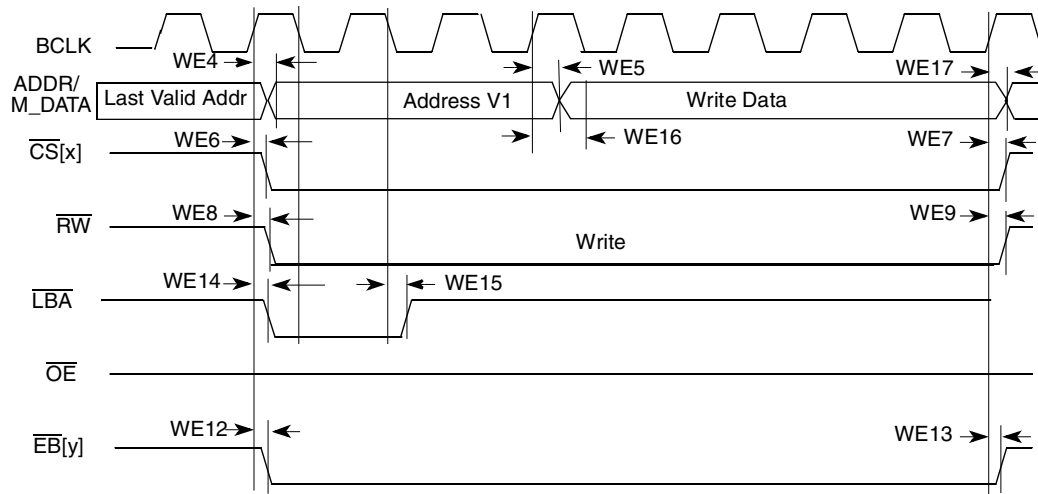
Figure 17. Synchronous Memory Timing Diagram for Write Access—WSC = 1, EBWA = 1, EBWN = 1, LBN = 1



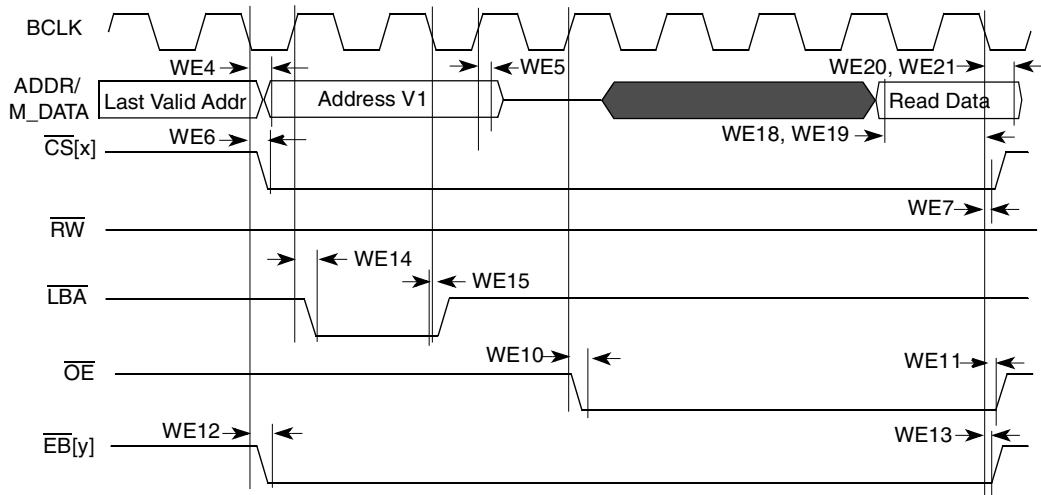
**Figure 18. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—
WSC = 2, SYNC = 1, DOL = 0**



**Figure 19. Synchronous Memory Timing Diagram for Burst Write Access—
BCS = 1, WSC = 4, SYNC = 1, DOL = 0, PSR = 1**



**Figure 20. Muxed A/D Mode Timing Diagram for Synchronous Write Access—
WSC = 7, LBA = 1, LBN = 1, LAH = 1**



**Figure 21. Muxed A/D Mode Timing Diagram for Synchronous Read Access—
WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7**

Figure 22 through Figure 26, and Table 31 help to determine timing parameters relative chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

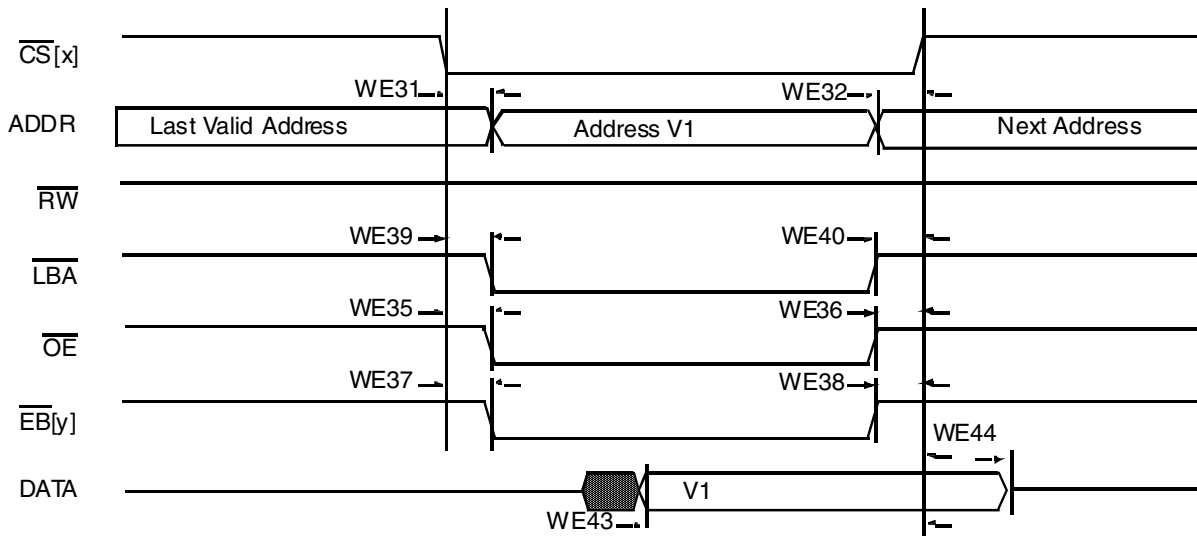


Figure 22. Asynchronous Memory Read Access

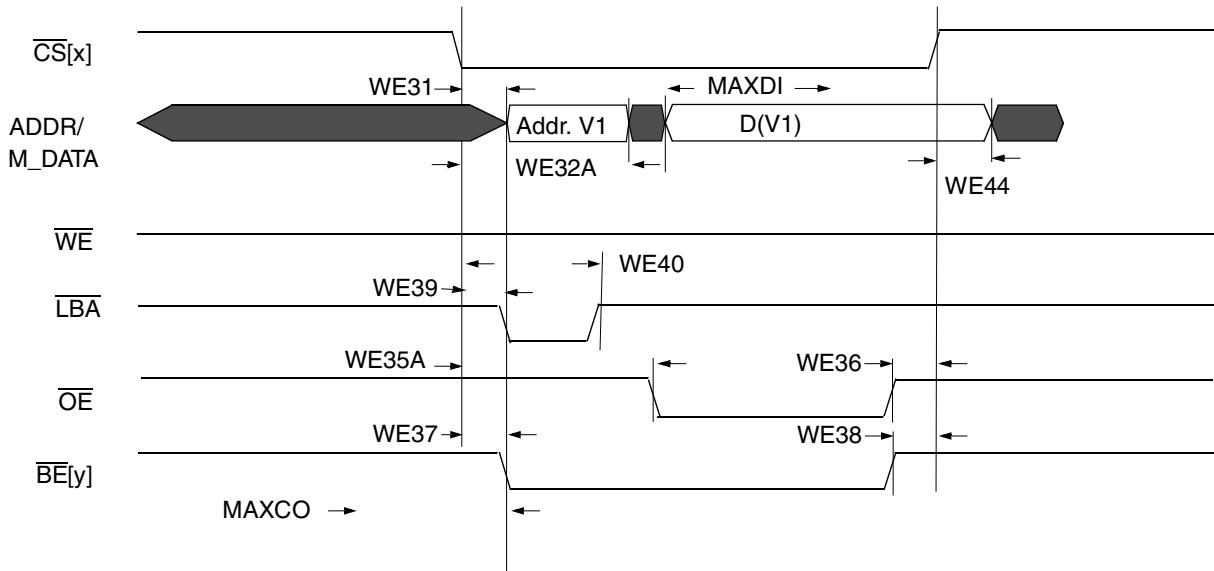


Figure 23. Asynchronous A/D muxed Read Access (RWSC = 5)

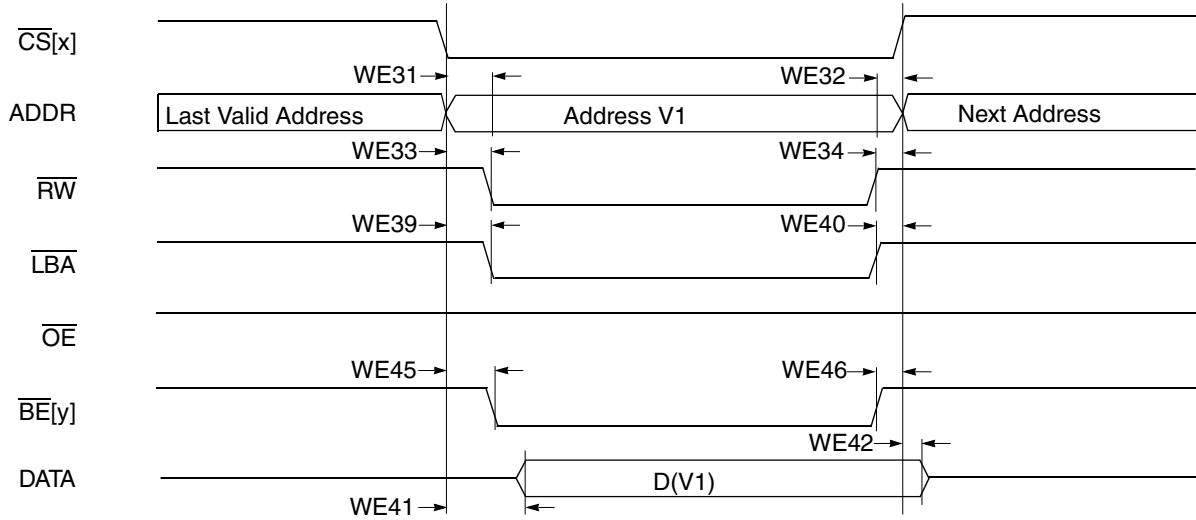


Figure 24. Asynchronous Memory Write Access

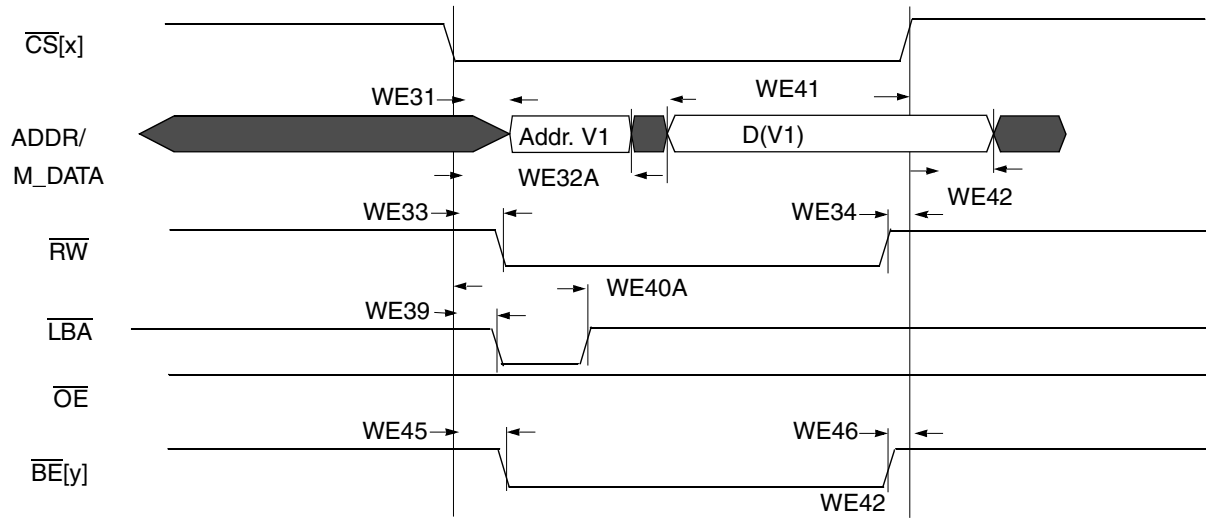


Figure 25. Asynchronous A/D Mux Write Access

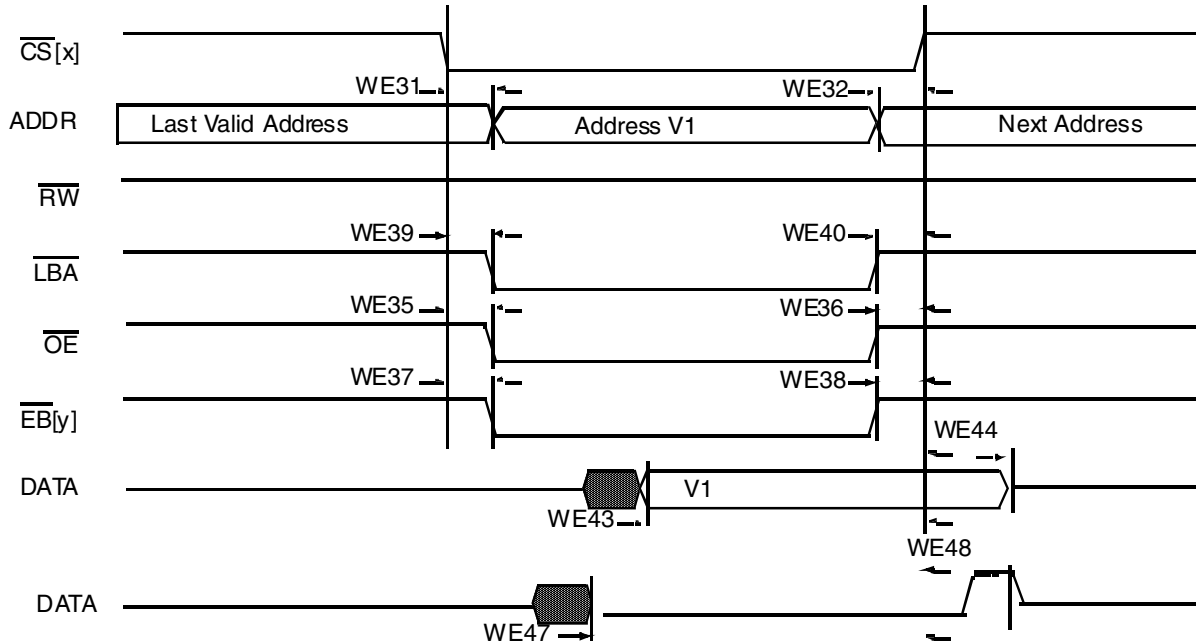


Figure 26. DTACK Read Access

Table 31. WEIM Asynchronous Timing Parameters Relative Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters ¹	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}[x]$ valid to Address valid	$WE4 - WE6 - CSA^2$	—	$3 - CSA$	ns
WE32	Address invalid to $\overline{CS}[x]$ invalid	$WE7 - WE5 - CSN^3$	—	$3 - CSN$	ns
WE32A (muxed A/D)	$\overline{CS}[x]$ valid to address invalid	$WE4 - WE7 + (LBN + LBA + 1 - CSA^2)$	$-3 + (LBN + LBA + 1 - CSA)$	—	ns
WE33	$\overline{CS}[x]$ valid to \overline{WE} valid	$WE8 - WE6 + (WEA - CSA)$	—	$3 + (WEA - CSA)$	ns
WE34	\overline{WE} invalid to $\overline{CS}[x]$ invalid	$WE7 - WE9 + (WEN - CSN)$	—	$3 - (WEN - CSN)$	ns
WE35	$\overline{CS}[x]$ valid to \overline{OE} valid	$WE10 - WE6 + (OEA - CSA)$	—	$3 + (OEA - CSA)$	ns
WE35A (muxed A/D)	$\overline{CS}[x]$ valid to \overline{OE} valid	$WE10 - WE6 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$	$-3 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$	$3 + (OEA + RLBN + RLBA + ADH + 1 - CSA)$	ns
WE36	\overline{OE} invalid to $\overline{CS}[x]$ invalid	$WE7 - WE11 + (OEN - CSN)$	—	$3 - (OEN - CSN)$	ns
WE37	$\overline{CS}[x]$ valid to $\overline{BE}[y]$ valid (read access)	$WE12 - WE6 + (RBEA - CSA)$	—	$3 + (RBEA^4 - CSA)$	ns
WE38	$\overline{BE}[y]$ invalid to $\overline{CS}[x]$ invalid (read access)	$WE7 - WE13 + (RBEN - CSN)$	—	$3 - (RBEN^5 - CSN)$	ns
WE39	$\overline{CS}[x]$ valid to \overline{LBA} valid	$WE14 - WE6 + (LBA - CSA)$	—	$3 + (LBA - CSA)$	ns
WE40	\overline{LBA} invalid to $\overline{CS}[x]$ invalid	$WE7 - WE15 - CSN$	—	$3 - CSN$	ns

Table 31. WEIM Asynchronous Timing Parameters Relative Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters ¹	Min	Max (If 133 MHz is supported by SoC)	Unit
WE40A (muxed A/D)	$\overline{CS}[x]$ valid to \overline{LBA} invalid	$WE14 - WE6 + (LBN + LBA + 1 - CSA)$	$-3 + (LBN + LBA + 1 - CSA)$	$3 + (LBN + LBA + 1 - CSA)$	ns
WE41	$\overline{CS}[x]$ valid to Output Data valid	$WE16 - WE6 - WCSA$	—	$3 - WCSA$	ns
WE41A (muxed A/D)	$\overline{CS}[x]$ valid to Output Data valid	$WE16 - WE6 + (WLBN + WLBA + ADH + 1 - WCSA)$	—	$3 + (WLBN + WLBA + ADH + 1 - WCSA)$	ns
WE42	Output Data invalid to $\overline{CS}[x]$ Invalid	$WE17 - WE7 - CSN$	—	$3 - CSN$	ns
WE43	Input Data valid to $\overline{CS}[x]$ invalid	$MAXCO - MAXCSO + MAXDI$	$MAXCO^6 - MAXCSO^7 + MAXDI^8$	—	ns
WE44	$\overline{CS}[x]$ invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}[x]$ valid to $\overline{BE}[y]$ valid (write access)	$WE12 - WE6 + (WBEA - CSA)$	—	$3 + (WBEA - CSA)$	ns
WE46	$\overline{BE}[y]$ invalid to $\overline{CS}[x]$ invalid (write access)	$WE7 - WE13 + (WBEN - CSN)$	—	$-3 + (WBEN - CSN)$	ns
WE47	\overline{DTACK} valid to $\overline{CS}[x]$ invalid	$MAXCO - MAXCSO + MAXDTI$	$MAXCO^6 - MAXCSO^7 + MAXDTI^9$	—	ns
WE48	$\overline{CS}[x]$ Invalid to \overline{DTACK} invalid	0	0	—	ns

¹ For the value of parameters WE4–WE21, see column BCD = 0 in Table 30.

² \overline{CS} Assertion. This bit field determines when the \overline{CS} signal is asserted during read/write cycles.

³ \overline{CS} Negation. This bit field determines when the \overline{CS} signal is negated during read/write cycles.

⁴ \overline{BE} Assertion. This bit field determines when the \overline{BE} signal is asserted during read cycles.

⁵ \overline{BE} Negation. This bit field determines when the \overline{BE} signal is negated during read cycles.

⁶ Output maximum delay from internal driving ADDR/control FFs to chip outputs.

⁷ Output maximum delay from $\overline{CS}[x]$ internal driving FFs to $\overline{CS}[x]$ out.

⁸ DATA maximum delay from chip input data to its internal FF.

⁹ DTACK maximum delay from chip dtack input to its internal FF.

Note: All configuration parameters (CSA, CSN, WBEA, WBEN, LBA, LBN, OEN, OEA, RBEA, and RBEN) are in cycle units.

4.9.5.3 ESDCTL Electrical Specifications

Figure 27 through Figure 36 depict the timings pertaining to the ESDCTL module, which interfaces with mobile DDR or SDR SDRAM. Table 32 through Table 41 list the timing parameters.

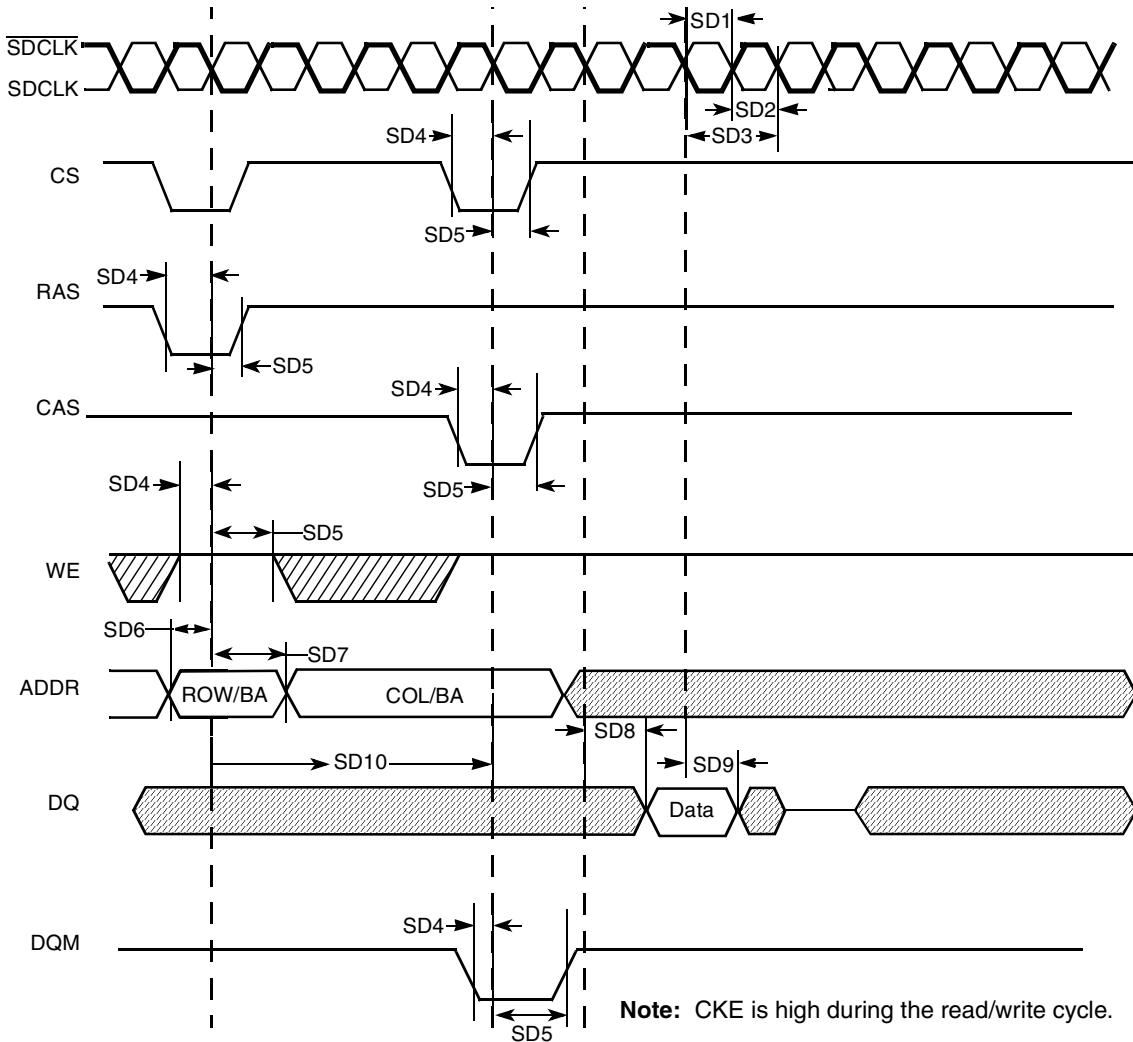


Figure 27. SDRAM Read Cycle Timing Diagram

Table 32. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns

Table 32. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns
SD9	Data out hold time ¹	tOH	1.2	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

¹ Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see [Table 40](#) and [Table 41](#).

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, [Table 32](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

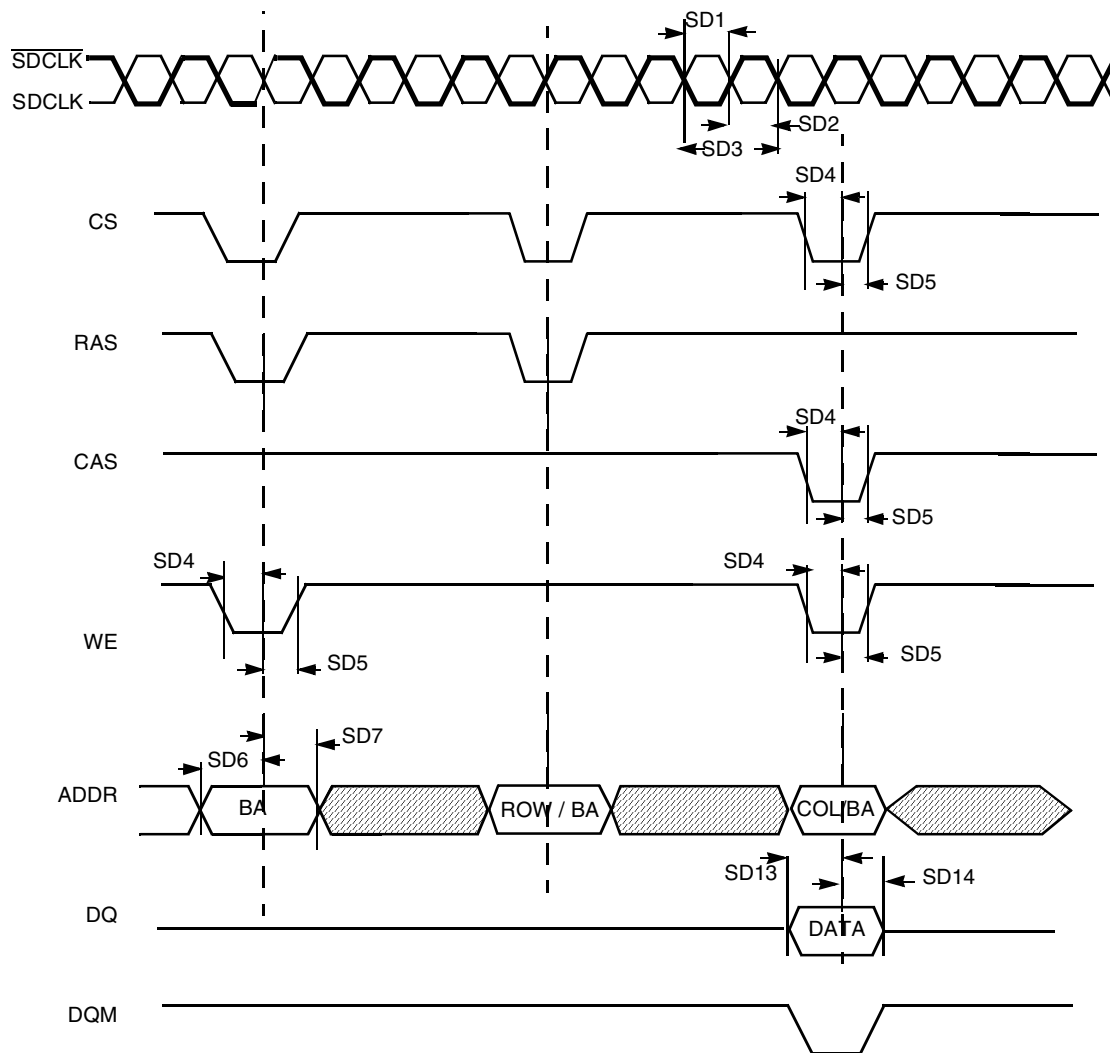


Figure 28. SDR SDRAM Write Cycle Timing Diagram

Table 33. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	t _{CH}	0.45	0.55	ns
SD2	SDRAM clock low-level width	t _{CL}	0.45	0.55	ns
SD3	SDRAM clock cycle time	t _{CK}	7.0	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	t _{CMS}	2.4	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	t _{CMH}	1.4	—	ns
SD6	Address setup time	t _{AS}	2.4	—	ns
SD7	Address hold time	t _{AH}	1.4	—	ns
SD13	Data setup time	t _{DS}	2.4	—	ns
SD14	Data hold time	t _{DH}	1.4	—	ns

NOTE

Test conditions are: pin voltage 1.7 V–1.95 V, capacitance 15 pF for all pins (both DDR and non-DDR pins), drive strength is high (7.2 mA). “High” is defined as 80% of signal value and “low” is defined as 20% of signal value.

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value. $t_{CH} + t_{CL}$ will not exceed 7.5 ns for 133 MHz. DDR SDRAM CLK parameters are measured at the crossing point of \overline{SDCLK} and \overline{SDCLK} (inverted clock).

The timing parameters are similar to the ones used in SDRAM data sheets. [Table 33](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of \overline{SDCLK} , and the parameters are measured at maximum memory frequency.

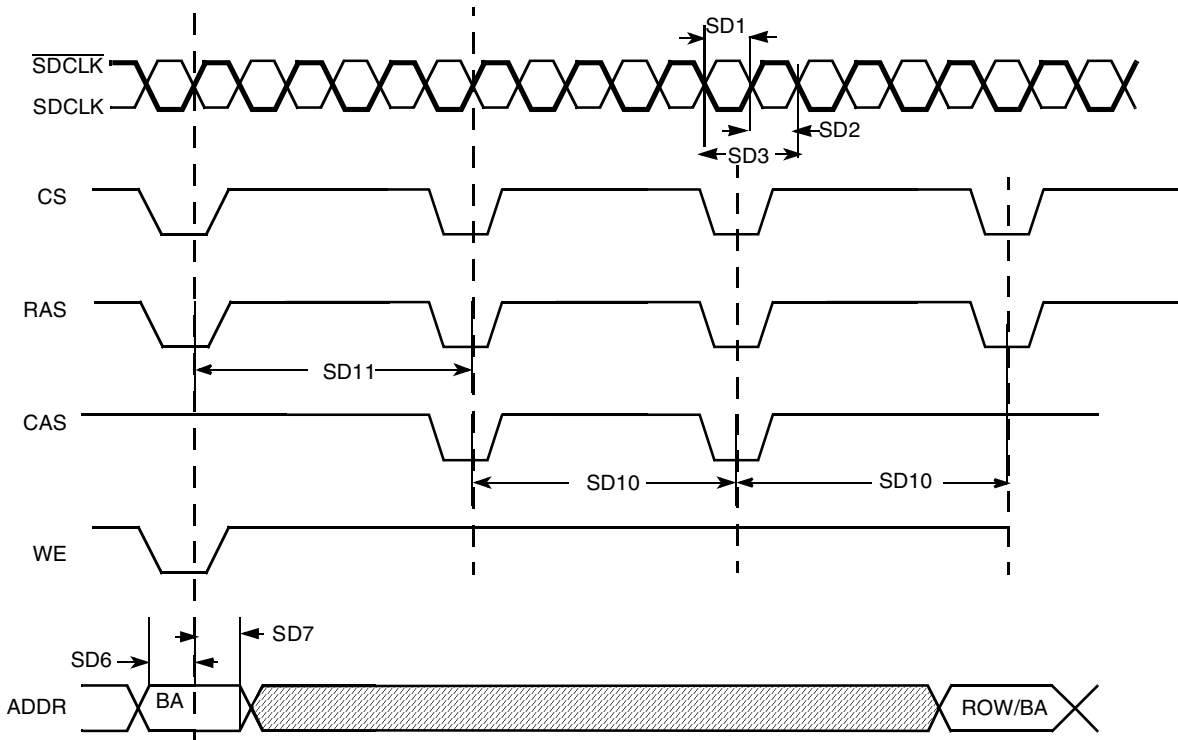


Figure 29. SDRAM Refresh Timing Diagram

Table 34. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	t_{CH}	3.4	4.1	ns
SD2	SDRAM clock low-level width	t_{CL}	3.4	4.1	ns
SD3	SDRAM clock cycle time	t_{CK}	7.5	—	ns
SD6	Address setup time	t_{AS}	1.8	—	ns

Table 34. SDRAM Refresh Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Unit
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period ¹	tRP	1	4	clock
SD11	Auto precharge command period ¹	tRC	2	20	clock

¹ SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. [Table 34](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

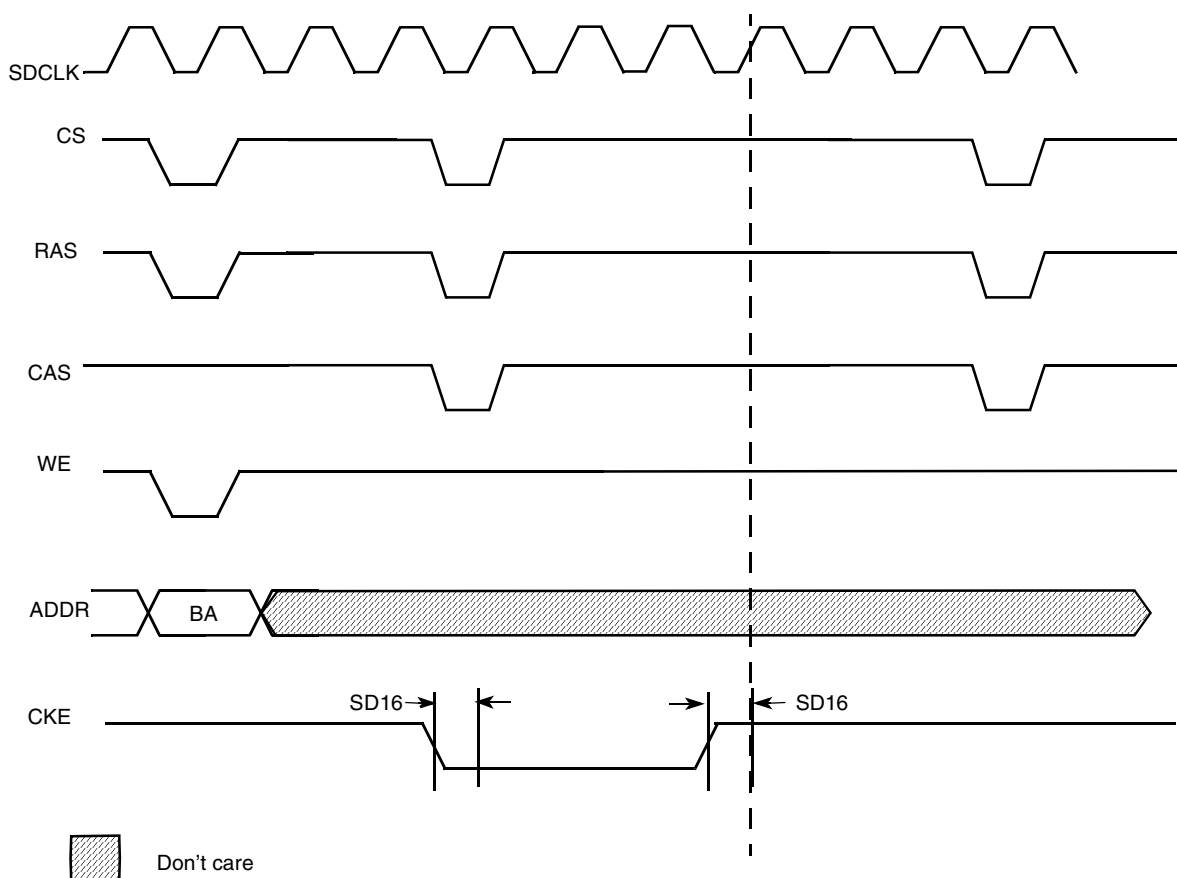


Figure 30. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

Table 35. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

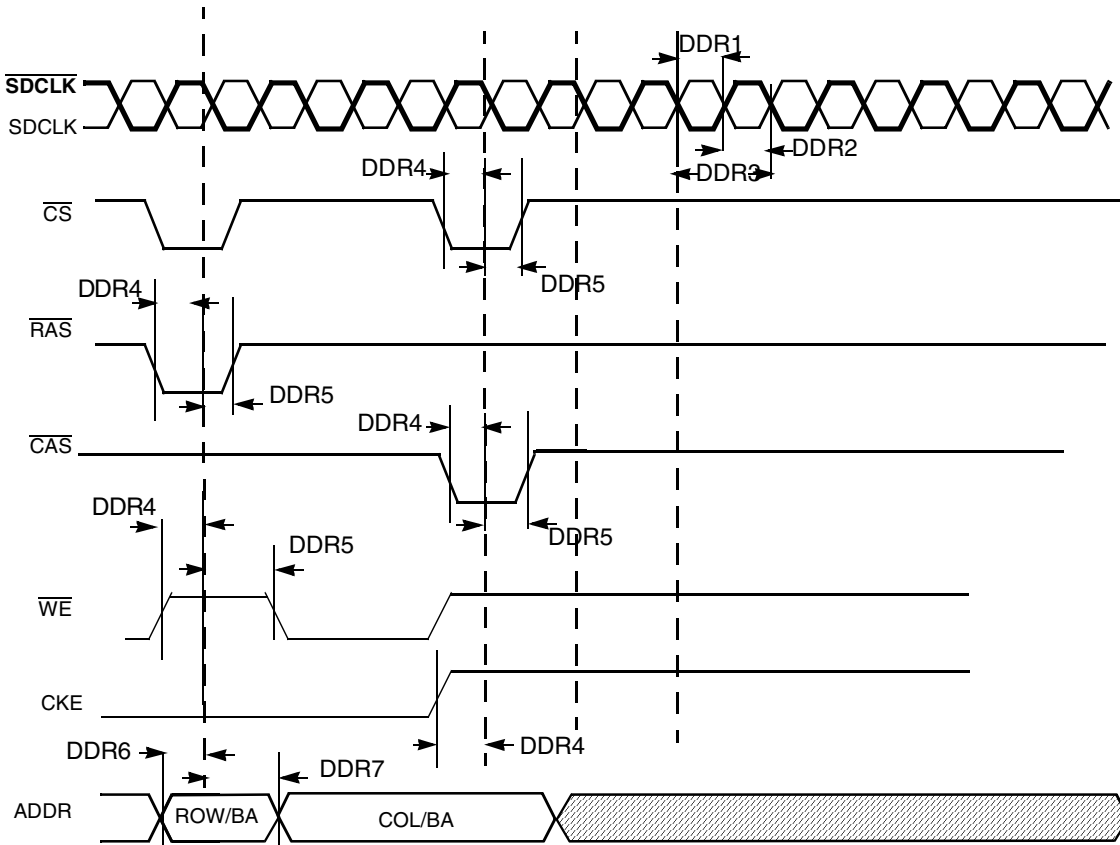


Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 36. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	tCH	0.45	0.55	tck
DDR2	SDRAM clock low-level width	tCL	0.45	0.55	tck
DDR3	SDRAM clock cycle time	tck	7.0	8.0	ns
DDR4	CS, RAS, CAS, CKE, WE setup time	tis ¹	0.35	—	ns

Table 36. DDR2 SDRAM Timing Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{tH}^1	0.475	—	ns
DDR6	Address output setup time	t_{tS}^1	0.35	—	ns
DDR7	Address output hold time	t_{tH}^1	0.475	—	ns

NOTE

These values are for command/address slew rate of 1 V/ns and SDCLK, SDCLK_B differential slew rate of 2 V/ns. For different values, use the derating table.

Table 37. Derating Values for DDR2-400, DDR2-533

t _{tS} , t _{tH} Derating Values for DDR2-400, DDR2-533									
CK,CK Differential Slew Rate									
2.0 V/ns									
1.5 V/ns									
1.0 V/ns									
	Δt_{tS}	Δt_{tH}	Δt_{tS}	Δt_{tH}	Δt_{tS}	Δt_{tH}	Units	Notes	
Com- mand/Ad- dress Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
0.15	-800	-708	-770	-678	-740	-648	ps	1	
0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1	

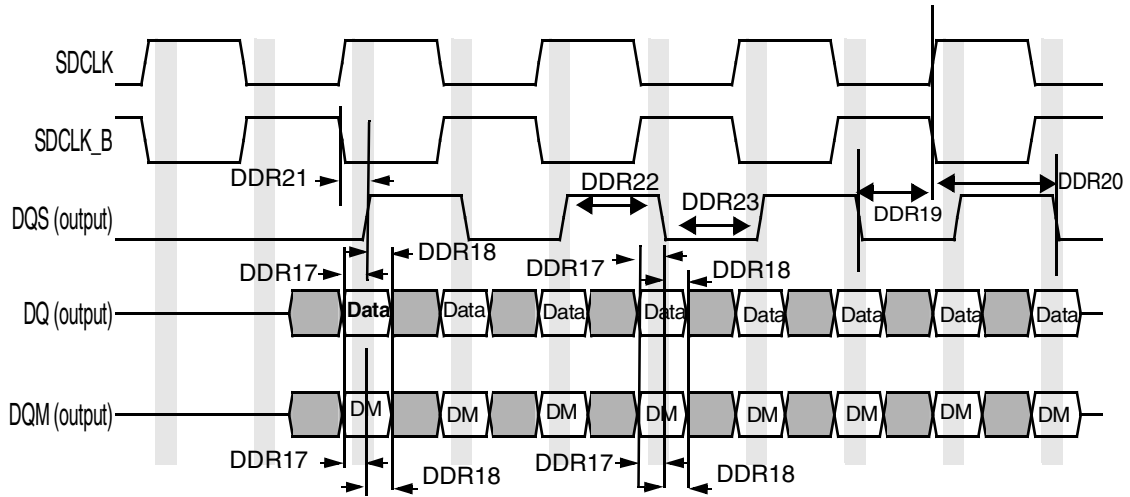


Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Figure 33. DDR2 SDRAM Write Cycle Parameters

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (single-ended strobe)	tDS1(base)	0.025	—	ns
DDR18	DQ and DQM hold time to DQS (single-ended strobe)	tDH1(base)	0.025	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time.	tDSS	0.2	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	0.2	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	tCK
DDR22	DQS high level width	tDQSH	0.35	—	tCK
DDR23	DQS low level width	tDQSL	0.35	—	tCK

NOTE

These values are for DQ/DM slew rate of 1 V/ns and DQS slew rate of 1 V/ns. For different values use the derating table.

Table 38. DDR Single-ended Slew Rate

Δt_{DS1} , Δt_{DH1} derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$	$\Delta t_{D S1}$	$\Delta t_{D H1}$		
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	

NOTE

SDR SDRAM CLK parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of $SDCLK$ and \overline{SDCLK} (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for $SDCLK$ and High for Address and controls.

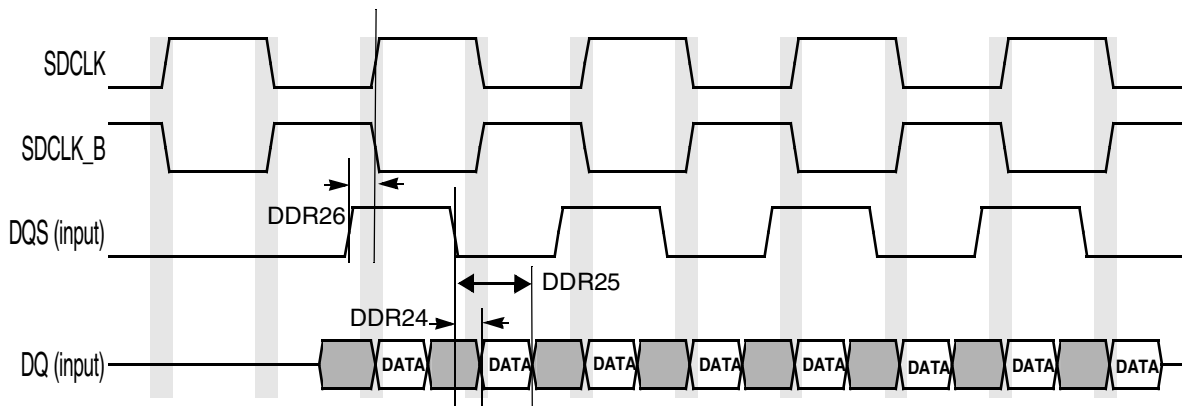


Figure 34. DDR2 SDRAM DQ vs. DQS and $SDCLK$ READ Cycle Timing Diagram

Table 39. DDR2 SDRAM Read Cycle Parameter Table

ID	PARAMETER	Symbol	DDR2-400		Unit
			Min	Max	
DDR24	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.35	ns
DDR25	DQS DQ in HOLD time from DQS ¹	tQH	2.925	—	ns
DDR26	DQS output access time from SDCLK posedge	tDQSK	-0.5	0.5	ns

¹The value was calculated for an SDCLK frequency of 133 MHz by the formula $t_{QH} = t_{HP} - t_{QHS} = \min(t_{CL}, t_{CH}) - t_{QHS} = 0.45 \times t_{CK} - t_{QHS} = 0.45 \times 7.5 - 0.45 = 2.925$ ns.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and \overline{SDCLK} (inverted clock).

Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strength is Medium for SDCLK and High for Address and controls.

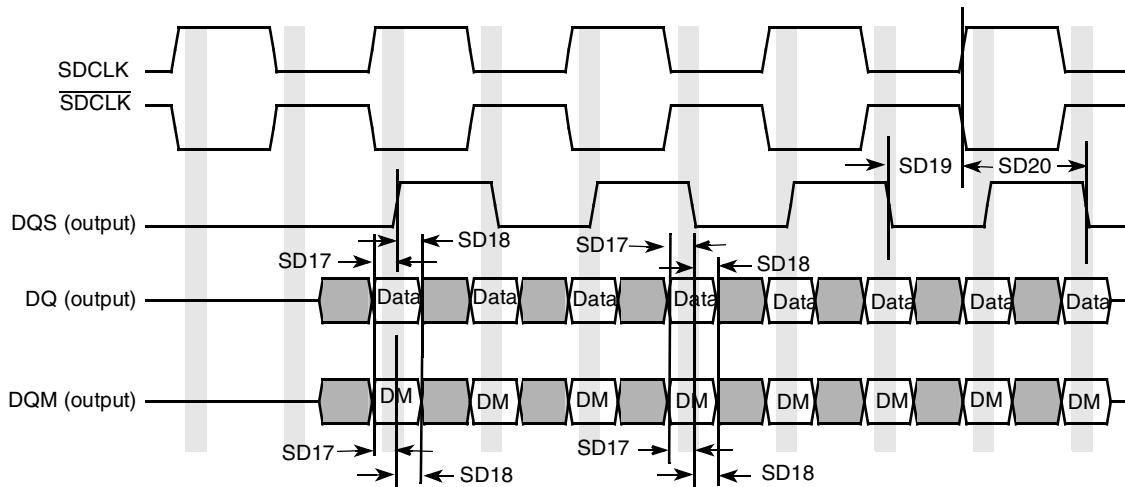


Figure 35. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 40. Mobile DDR SDRAM Write Cycle Timing Parameters¹

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

¹ Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. [Table 40](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

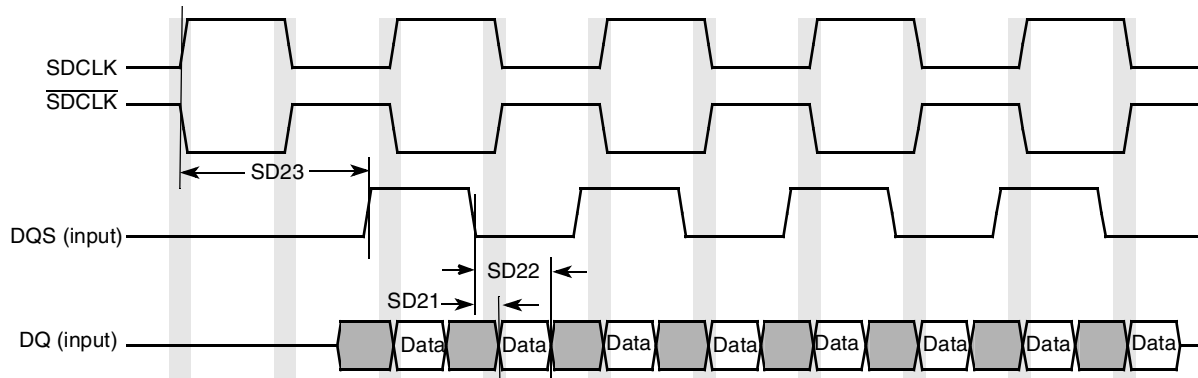


Figure 36. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 41. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS-related parameters are measured from the 50% point—that is, “high” is defined as 50% of signal value, and “low” is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets. [Table 41](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK, and the parameters are measured at maximum memory frequency.

4.9.6 Enhanced Serial Audio Interface (ESAI) Timing Specifications

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 42 shows the interface timing values. The number field in the table refers to timing signals found in Figure 37 and Figure 38.

Table 42. Enhanced Serial Audio Interface Timing

No.	Characteristics ^{1,2}	Symbol	Expression ²	Min.	Max.	Condition ³	Unit
62	Clock cycle ⁴	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period	—	$2 \times T_C - 9.0$	6	—	—	ns
	• For internal clock	—	$2 \times T_C$	15	—	—	
	• For external clock	—	$2 \times T_C$	15	—	—	
64	Clock low period	—	$2 \times T_C - 9.0$	6	—	—	ns
	• For internal clock	—	$2 \times T_C$	15	—	—	
	• For external clock	—	$2 \times T_C$	15	—	—	
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge ⁵	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 42. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics ^{1,2}	Symbol	Expression ²	Min.	Max.	Condition ³	Unit
80	SCKT rising edge to FST out (wr) high ⁵	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low ⁵	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance ^{6,7}	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge ⁵	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns

¹ i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

² bl = bit length
wl = word length
wr = word length relative

³ SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

⁴ For the internal clock, the external clock cycle is defined by l_{cy}c and the ESAI control register.

⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

⁶ Periodically sampled and not 100% tested.

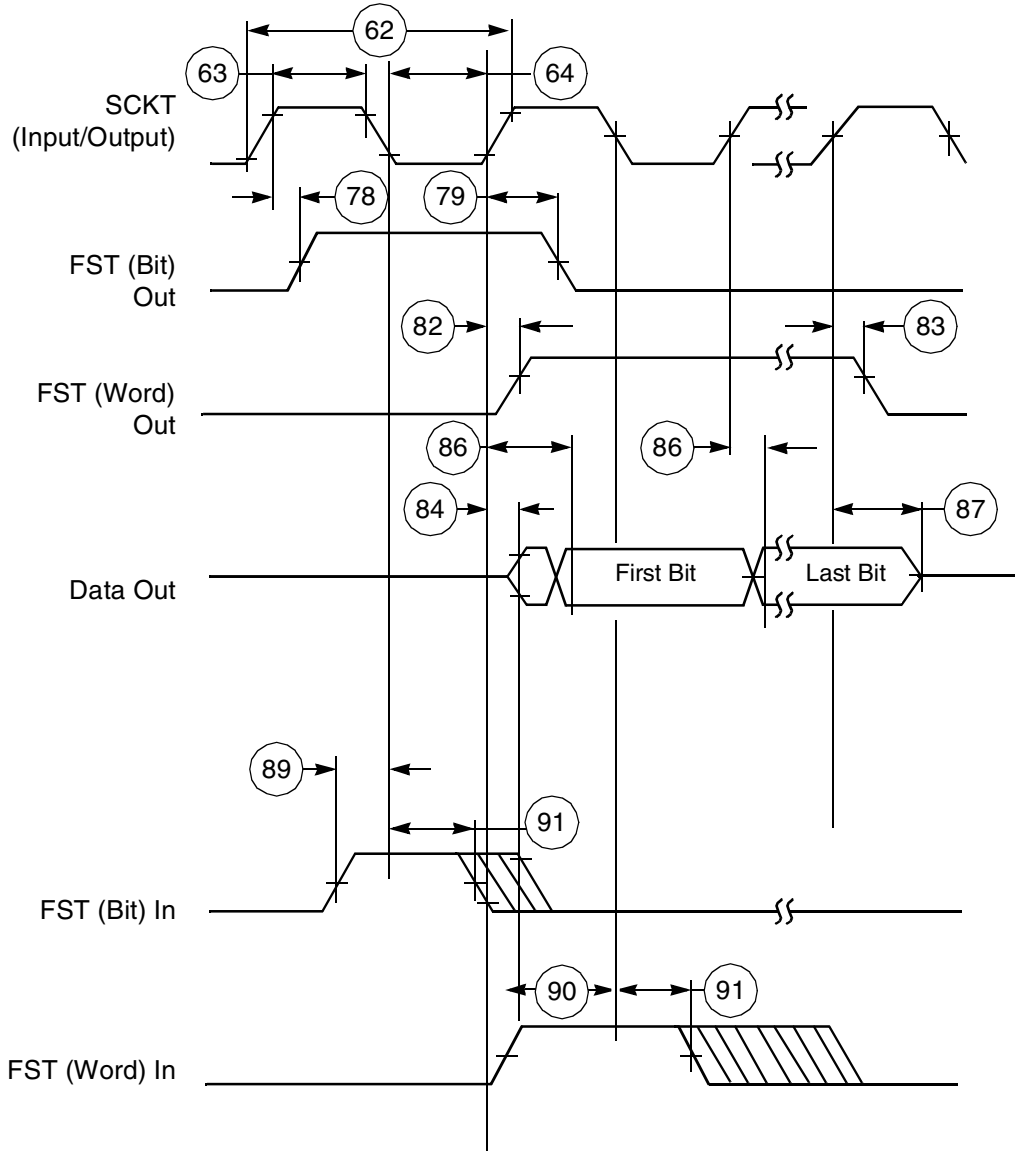


Figure 37. ESAI Transmitter Timing

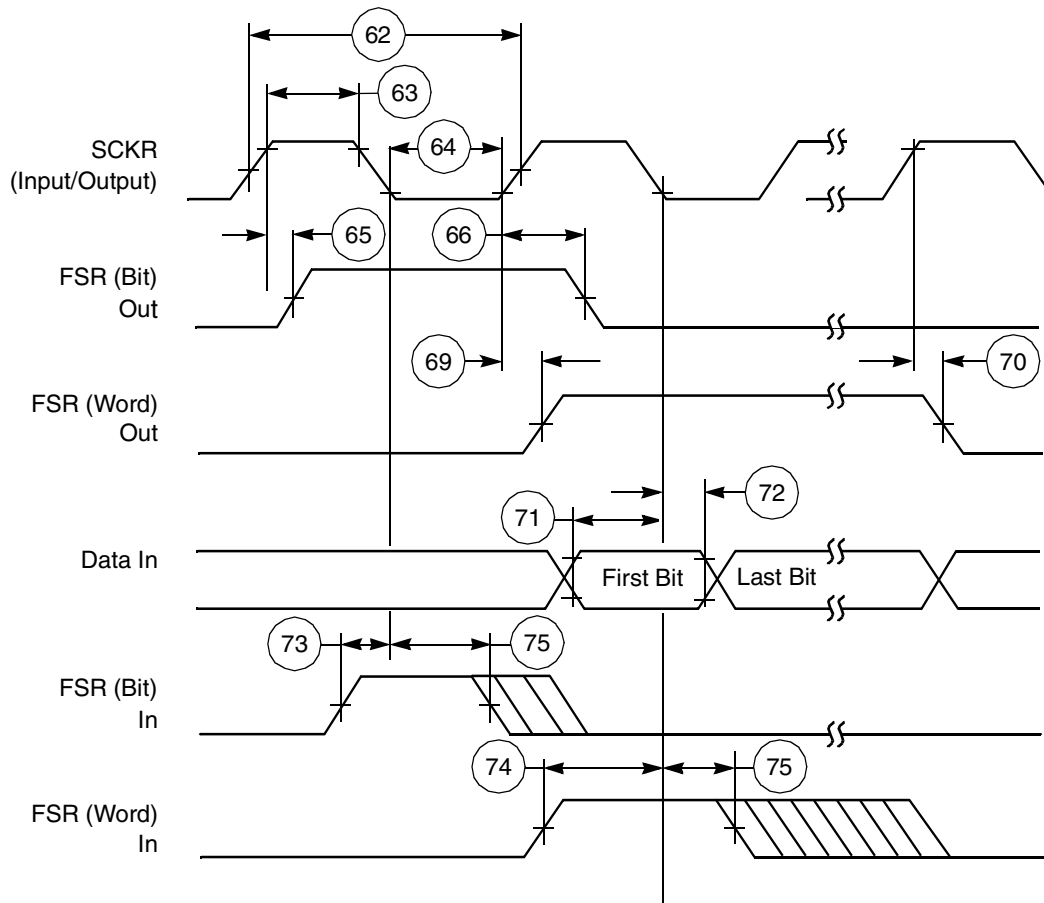


Figure 38. ESAI Receiver Timing

4.9.7 eSDHCv2 AC Electrical Specifications

Figure 39 depicts the timing of eSDHCv2, and Table 43 lists the eSDHCv2 timing characteristics. The following definitions apply to values and signals described in Table 43:

- LS: low-speed mode. Low-speed card can tolerate a clock up to 400 kHz.
- FS: full-speed mode. For a full-speed MMC card, the card clock can reach 20 MHz; a full-speed SD/SDIO card can reach 25 MHz.
- HS: high-speed mode. For a high-speed MMC card, the card clock can reach 52 MHz; SD/SDIO can reach 50 MHz.

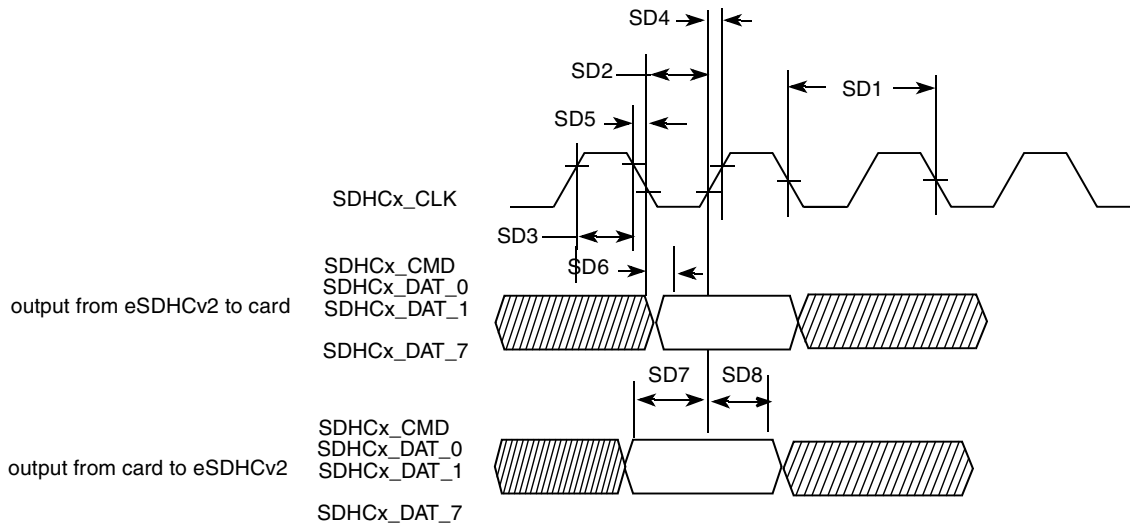


Figure 39. eSDHCv2 Timing

Table 43. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (Low Speed)	f_{PP}^1	0	400	kHz
	Clock frequency (SD/SDIO Full Speed/High Speed)	f_{PP}^2	0	25/50	MHz
	Clock frequency (MMC Full Speed/High Speed)	f_{PP}^3	0	20/52	MHz
	Clock frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	-3	3	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	5	—	ns
SD8	eSDHC input hold time	t_{IH}^4	2.5	—	ns

¹ In low-speed mode, the card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal-speed mode for the SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal-speed mode for MMC card, clock frequency can be any value between 0 and 20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.8 Fast Ethernet Controller (FEC) AC Electrical Specifications

This section describes the electrical information of the FEC module. The FEC is designed to support both 10- and 100-Mbps Ethernet networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps Media Independent Interface (MII) using a total of 18 pins. The 10-Mbps 7-wire interface that is restricted to a 10-Mbps data rate uses seven of the MII pins for connection to an external Ethernet transceiver.

4.9.8.1 FEC AC Timing

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.9.8.2 MII Receive Signal Timing

The MII receive timing signals consist of FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 44 lists MII receive channel timings.

Table 44. MII Receive Signal Timing

Num.	Characteristic ¹	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

¹ FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 40 shows the MII receive signal timings listed in Table 44.

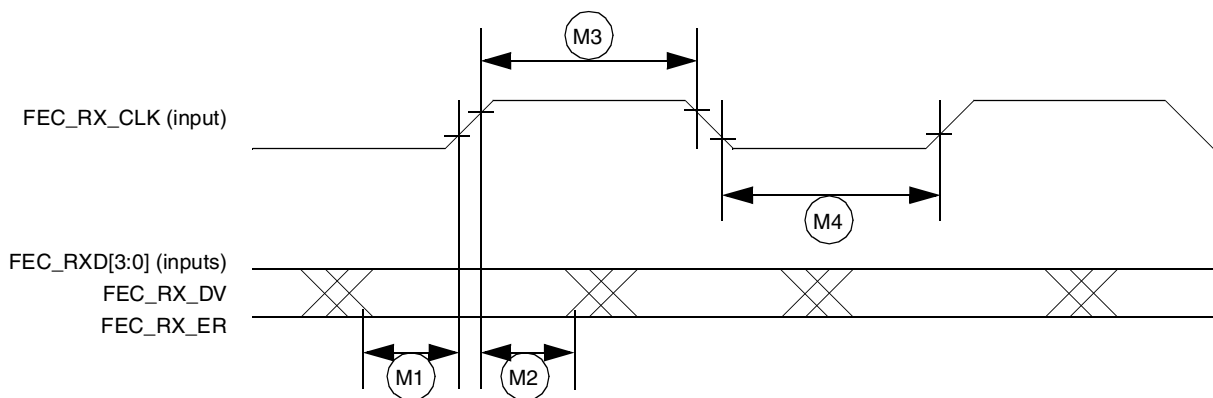


Figure 40. MII Receive Signal Timing Diagram

4.9.8.3 MII Transmit Signal Timing

The transmitter timing signals consist of FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 45 lists MII transmit channel timings.

Table 45. MII Transmit Signal Timing

Num	Characteristic ¹	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

¹ FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing when in 10 Mbps 7-wire interface mode.

Figure 41 shows the MII transmit signal timings listed in Table 45.

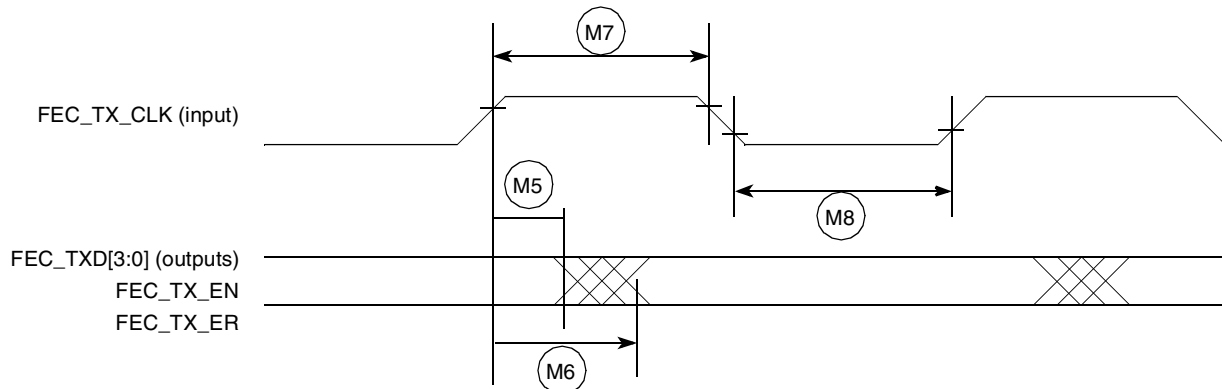


Figure 41. MII Transmit Signal Timing Diagram

4.9.8.4 MII Asynchronous Inputs Signal Timing

The MII asynchronous timing signals are FEC_CR_S and FEC_CO_L. Table 46 lists MII asynchronous inputs signal timing.

Table 46. MII Asynch Inputs Signal Timing

Num	Characteristic	Min.	Max.	Unit
M9 ¹	FEC_CR_S to FEC_CO_L minimum pulse width	1.5	—	FEC_TX_CLK period

¹ FEC_CO_L has the same timing in 10 Mbit 7-wire interface mode.

Figure 42 shows MII asynchronous input timings listed in Table 46.

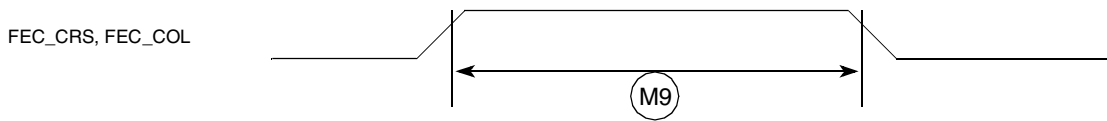


Figure 42. MII Asynch Inputs Timing Diagram

4.9.8.5 MII Serial Management Channel Timing

Serial management channel timing is accomplished using FEC_MDIO and FEC_MDC. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. Table 47 lists MII serial management channel timings.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 47. MII Transmit Signal Timing

Num	Characteristic	Min.	Max.	Units
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 43 shows MII serial management channel timings listed in Table 47.

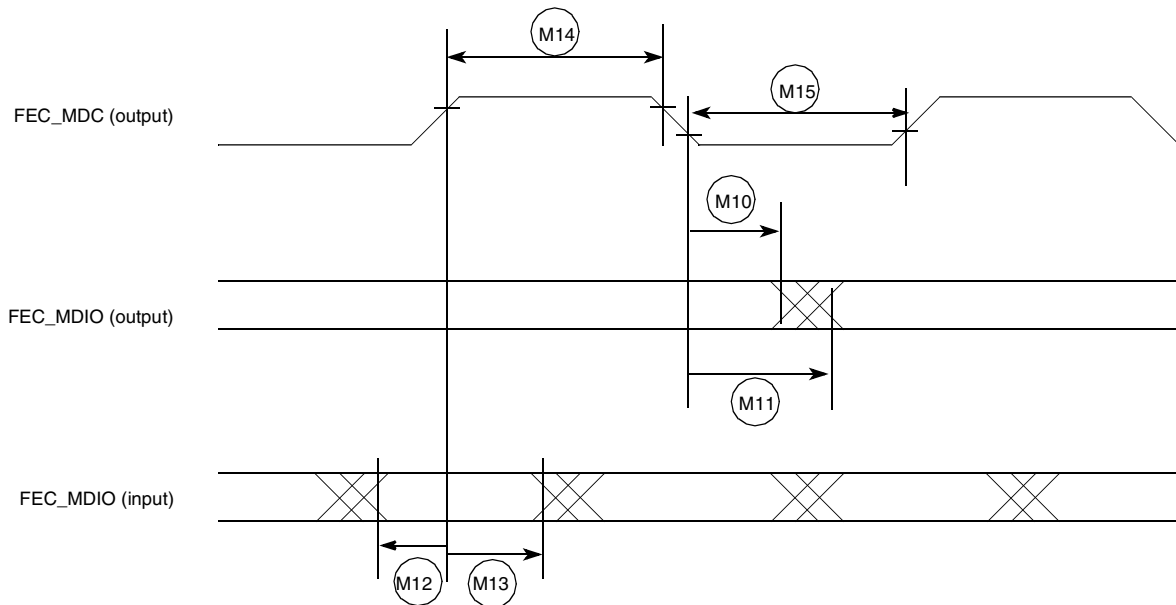


Figure 43. MII Serial Management Channel Timing Diagram

4.9.9 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) defined by IrDA[®] (Infrared Data Association). Refer to the IrDA[®] website for details on FIR and MIR protocols.

4.9.10 FlexCAN Module AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver outside the chip. The i.MX35 has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. Refer to the IOMUX chapter of the *MCIMX35 Multimedia Applications Processor Reference Manual* to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.9.11 I²C AC Electrical Specifications

This section describes the electrical characteristics of the I²C module.

4.9.11.1 I²C Module Timing

Figure 44 depicts the timing of the I²C module. Table 48 lists the I²C module timing parameters.

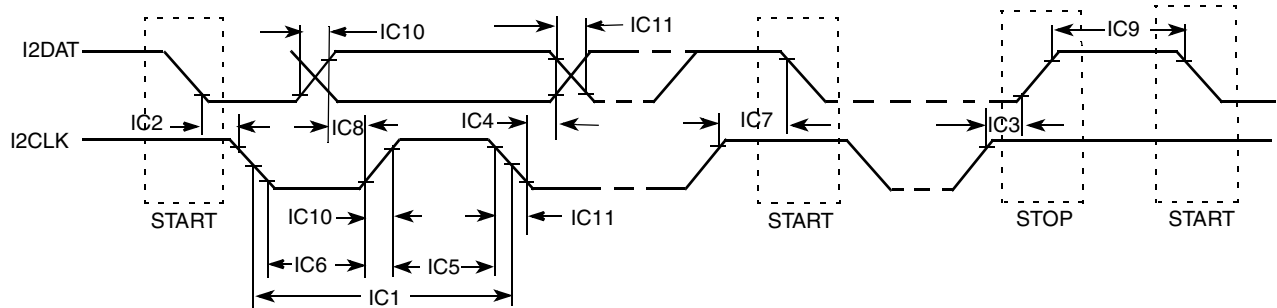


Figure 44. I²C Bus Timing Diagram

Table 48. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
IC8	Data set-up time	250	—	100 ³	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	—	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	—	300	ns
IC12	Capacitive load for each bus line (C _b)	—	400	—	400	pF

¹ A device must internally provide a hold time of at least 300 ns for the I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

² The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

³ A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line $\text{max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns}$ (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4.9.12 IPU—Sensor Interfaces

This section contains a list of supported camera sensors, a functional description, and the electrical characteristics.

4.9.12.1 Supported Camera Sensors

Table 49 lists the known supported camera sensors at the time of publication.

Table 49. Supported Camera Sensors¹

Vendor	Model
Conexant	CX11646, CX20490 ² , CX20450 ²
Agilent	HDCCP-2010, ADCS-1021 ² , ADCS-1021 ²
Toshiba	TC90A70
ICMedia	ICM202A, ICM102 ²
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC-0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501 ² , W6600 ² , W6552 ² , STV0974 ²
OmniVision	OV7620, OV6630, OV2640
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python) ² , SCM20014 ² , SCM20114 ² , SCM22114 ² , SCM20027 ²
National Semiconductor	LM9618 ²

¹ Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

² These sensors have not been validated at the time of publication.

4.9.12.2 Functional Description

There are three timing modes supported by the IPU.

4.9.12.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which typically include image processing capability, support video mode transfer operations. They use an embedded timing syntax to replace the SENS_B_VSYNC and SENS_B_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of the ITU BT.656 specifications. The only control signal used is SENS_B_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with an EAV code. In some cases, digital blanking is

inserted in between EAV and SAV code. The CSI decodes and filters out the timing coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

4.9.12.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See [Figure 45](#).

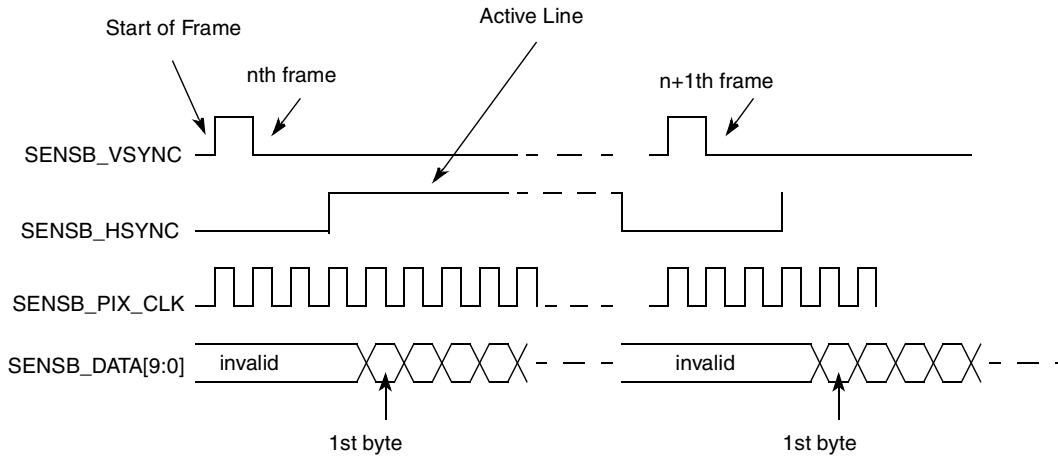


Figure 45. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timing corresponds to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. The pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of the line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the SENSB_HSYNC timing repeats. For the next frame, the SENSB_VSYNC timing repeats.

4.9.12.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in [Section 4.9.12.2.2, “Gated Clock Mode”](#)), except for the SENSB_HSYNC signal, which is not used. See [Figure 46](#). All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

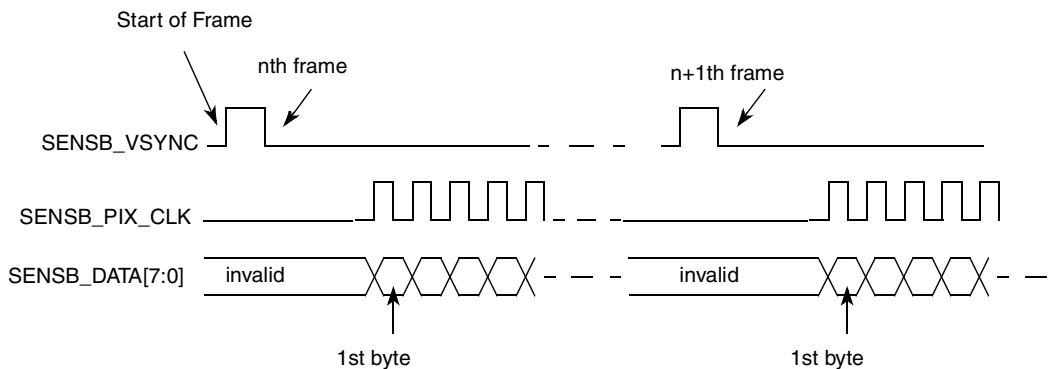


Figure 46. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 46 is that of a Motorola sensor. Some other sensors may have slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENS_B_VSYNC; active-high/low SENS_B_HSYNC; and rising/falling-edge triggered SENS_B_PIX_CLK.

4.9.12.3 Electrical Characteristics

Figure 47 depicts the sensor interface timing, and Table 50 lists the timing parameters.

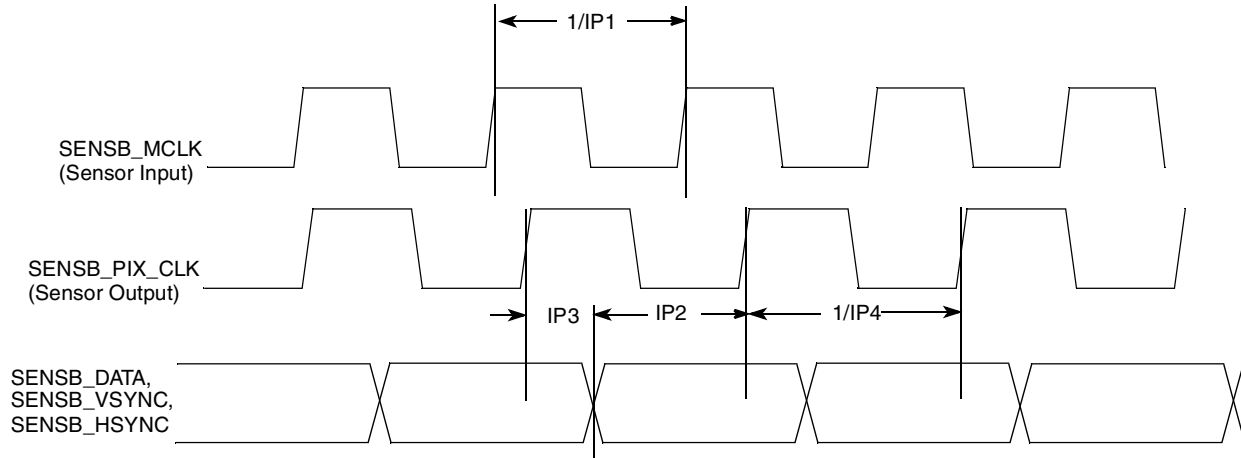


Figure 47. Sensor Interface Timing Diagram

Table 50. Sensor Interface Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

4.9.13 IPU—Display Interfaces

This section describes the following types of display interfaces:

- [Section 4.9.13.1, “Synchronous Interfaces”](#)
- [Section 4.9.13.2, “Interface to Sharp HR-TFT Panels”](#)
- [Section 4.9.13.3, “Synchronous Interface to Dual-Port Smart Displays”](#)
- [Section 4.9.13.4, “Asynchronous Interfaces”](#)
- [Section 4.9.13.5, “Serial Interfaces, Functional Description”](#)

4.9.13.1 Synchronous Interfaces

This section discusses the interfaces to active matrix TFT LCD panels, Sharp HR-TFT, and dual-port smart displays.

4.9.13.1.4 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 48 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is as follows:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted to the display. When disabled, the data is invalid and the trace is off.

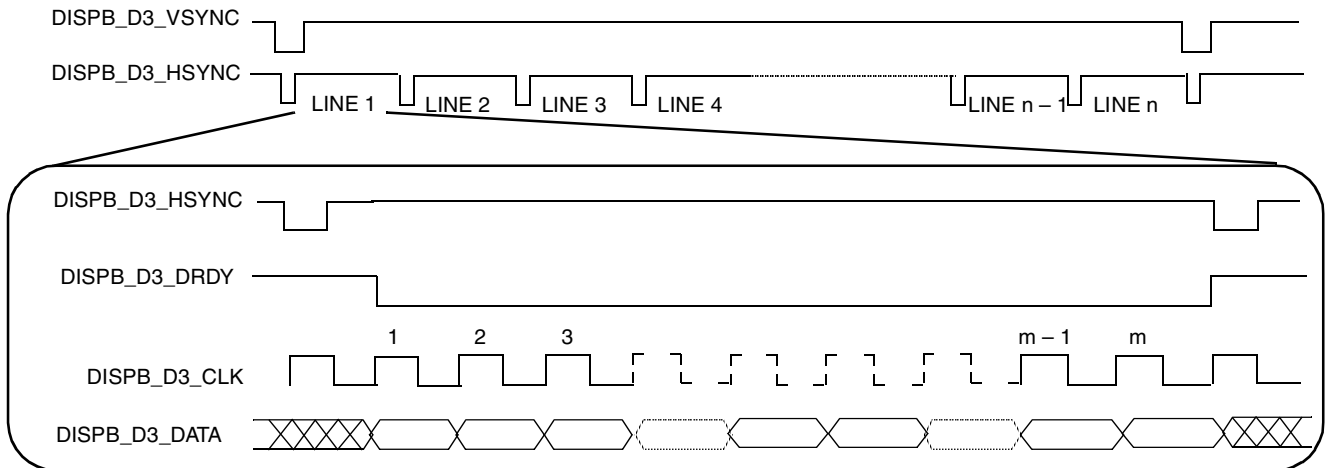


Figure 48. Interface Timing Diagram for TFT (Active Matrix) Panels

4.9.13.1.5 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 49 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity

of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

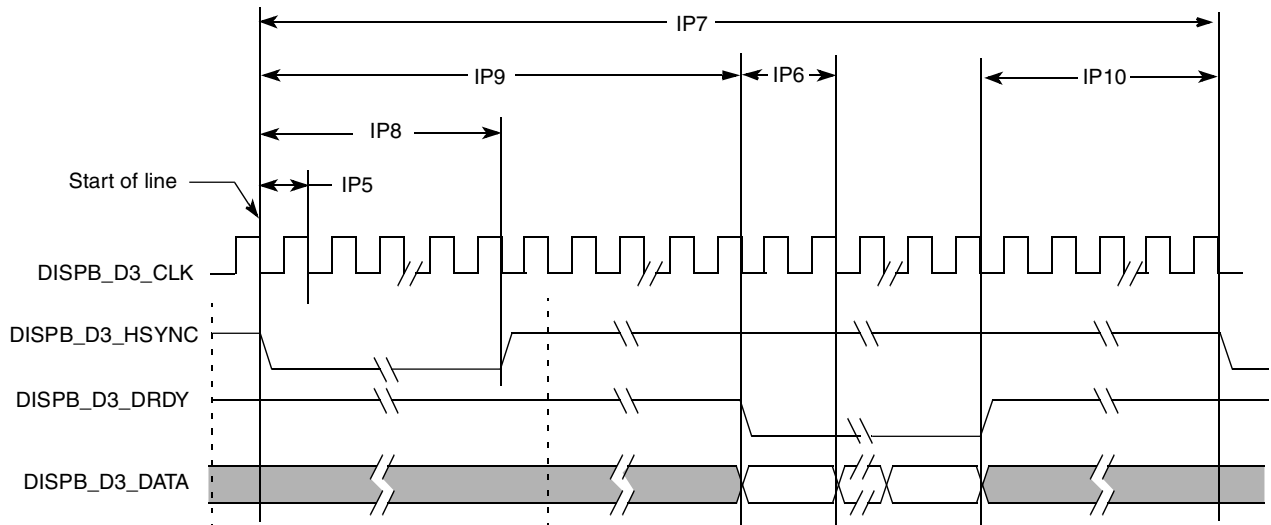


Figure 49. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 50 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

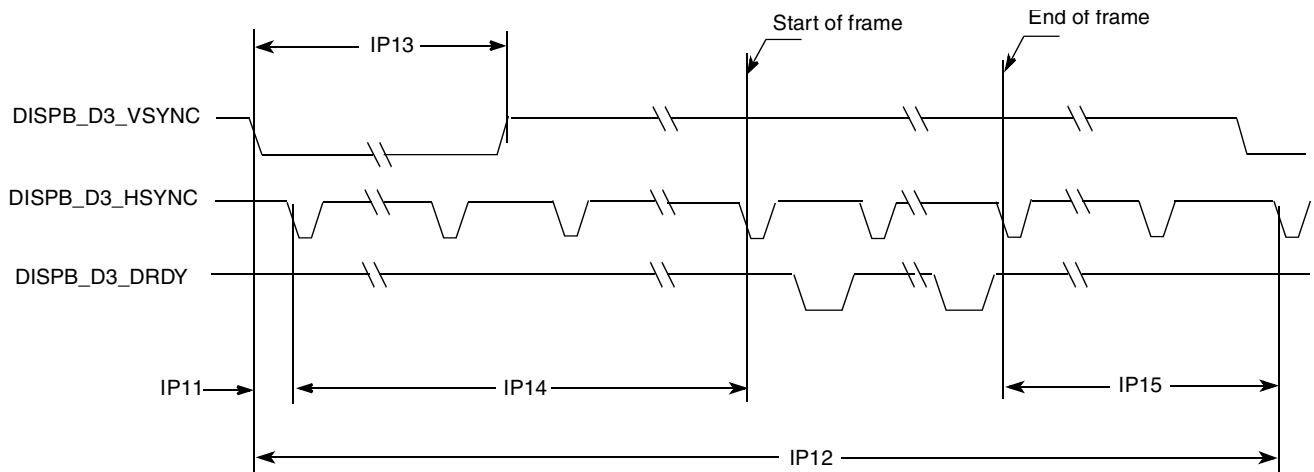


Figure 50. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 51 shows timing parameters of signals presented in Figure 49 and Figure 50.

Table 51. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp ¹	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D + 1) × Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH + 1) × Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH + 1) × Tdpcp	ns

Table 51. Synchronous Display Interface Timing Parameters—Pixel Level (continued)

ID	Parameter	Symbol	Value	Units
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdpcp	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdpcp	ns
IP11	HSYNC delay	Thsd	H_SYNC_DELAY × Tdpcp	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT + 1) × Tsw	ns
IP13	VSYNC width	Tvsw	if V_SYNC_WIDTH_L = 0 than (V_SYNC_WIDTH + 1) × Tdpcp else (V_SYNC_WIDTH + 1) × Tsw	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	ns

¹ Display interface clock period immediate value

Display interface clock period average value.

$$\bar{T}_{dicp} = T_{HSP_CLK} \cdot \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD}$$

Figure 51 depicts the synchronous display interface timing for access level, and Table 52 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

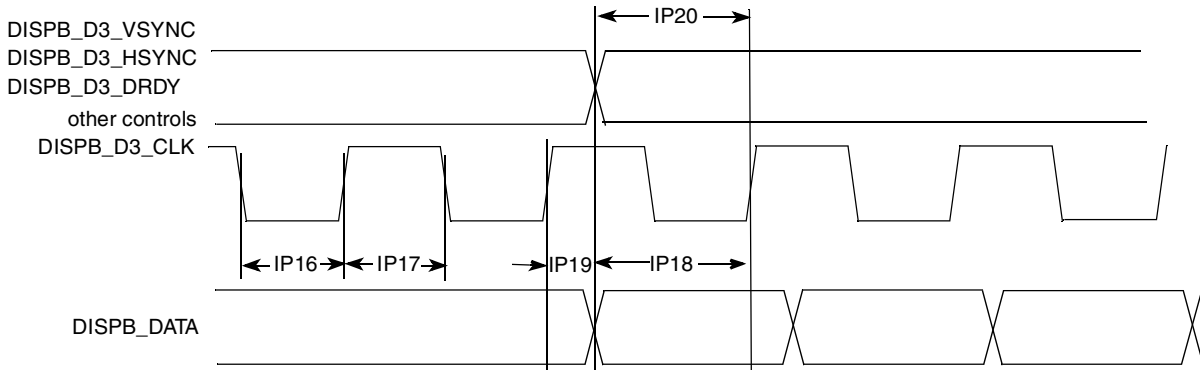


Figure 51. Synchronous Display Interface Timing Diagram—Access Level

Table 52. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP16	Display interface clock low time	Tckl	Tdicd – Tdicu – 1.5	Tdicd ² – Tdicu ³	Tdicd – Tdicu + 1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp – Tdicd + Tdicu – 1.5	Tdicp – Tdicd + Tdicu	Tdicp – Tdicd + Tdicu + 1.5	ns
IP18	Data setup time	Tdsu	Tdicd – 3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp – Tdicd – 3.5	Tdicp – Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd – 3.5	Tdicu	—	ns

¹ The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

² Display interface clock down time

$$T_{dicd} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot \text{DISP3_IF_CLK_DOWN_WR}}{HSP_CLK_PERIOD} \right]$$

³ Display interface clock up time

$$T_{dicu} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot \text{DISP3_IF_CLK_UP_WR}}{HSP_CLK_PERIOD} \right]$$

where CEIL(X) rounds the elements of X to the nearest integers toward infinity.

4.9.13.2 Interface to Sharp HR-TFT Panels

Figure 52 depicts the Sharp HR-TFT panel interface timing, and Table 53 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to

Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.” The timing images correspond to straight polarity of the Sharp signals.

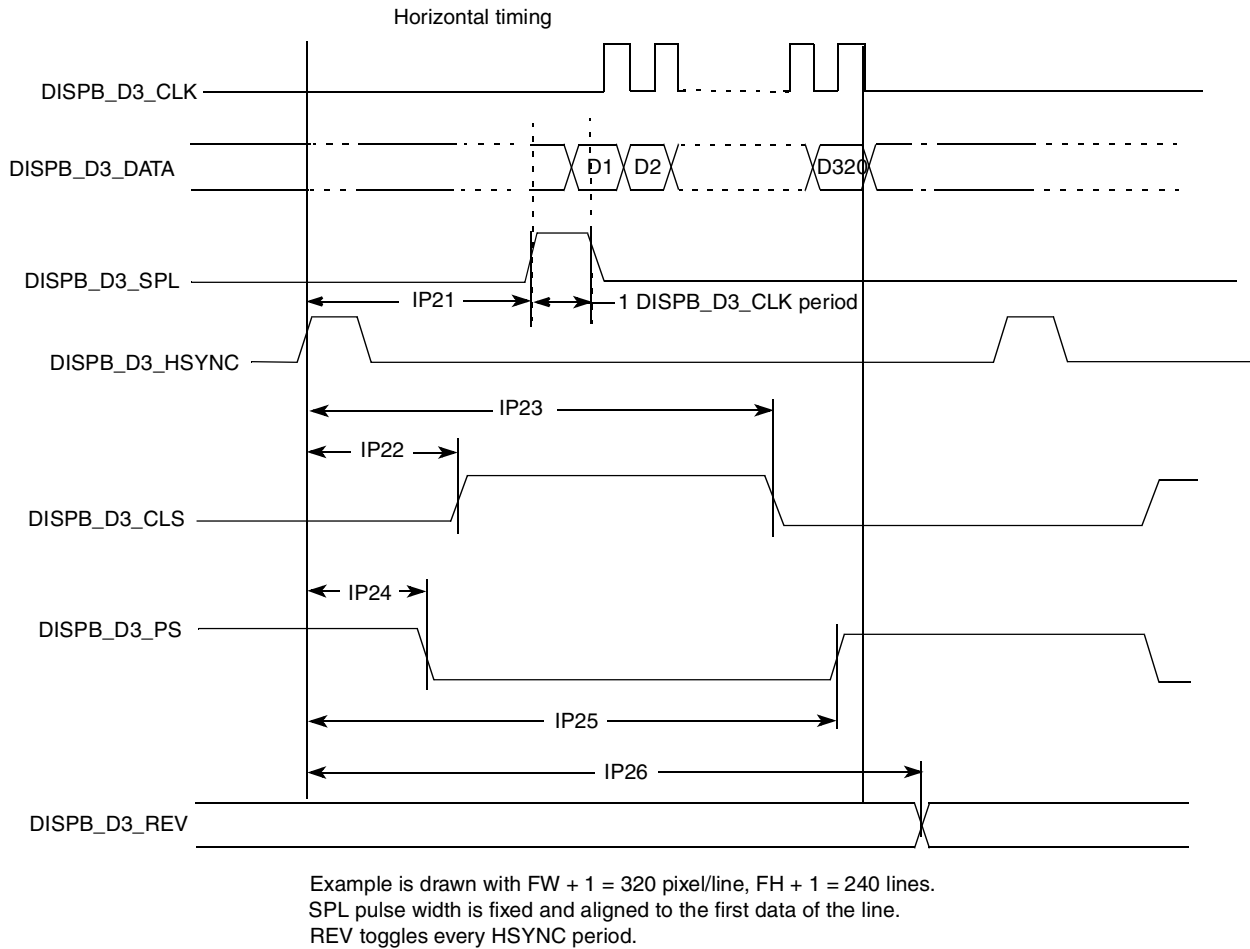


Figure 52. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level

Table 53. Sharp Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP21	SPL rise time	Tsplr	$(BGXP - 1) \times Tdpcp$	ns
IP22	CLS rise time	Tclsr	$CLS_RISE_DELAY \times Tdpcp$	ns
IP23	CLS fall time	Tclsf	$CLS_FALL_DELAY \times Tdpcp$	ns
IP24	CLS rise and PS fall time	Tpsf	$PS_FALL_DELAY \times Tdpcp$	ns
IP25	PS rise time	Tpsr	$PS_RISE_DELAY \times Tdpcp$	ns
IP26	REV toggle time	Trev	$REV_TOGGLE_DELAY \times Tdpcp$	ns

4.9.13.3 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See [Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”](#)

4.9.13.3.6 Interface to a TV Encoder—Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. [Figure 53](#) depicts the interface timing.

- The frequency of the clock DISPB_D3_CLK is 27 MHz.
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
 - At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
 - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

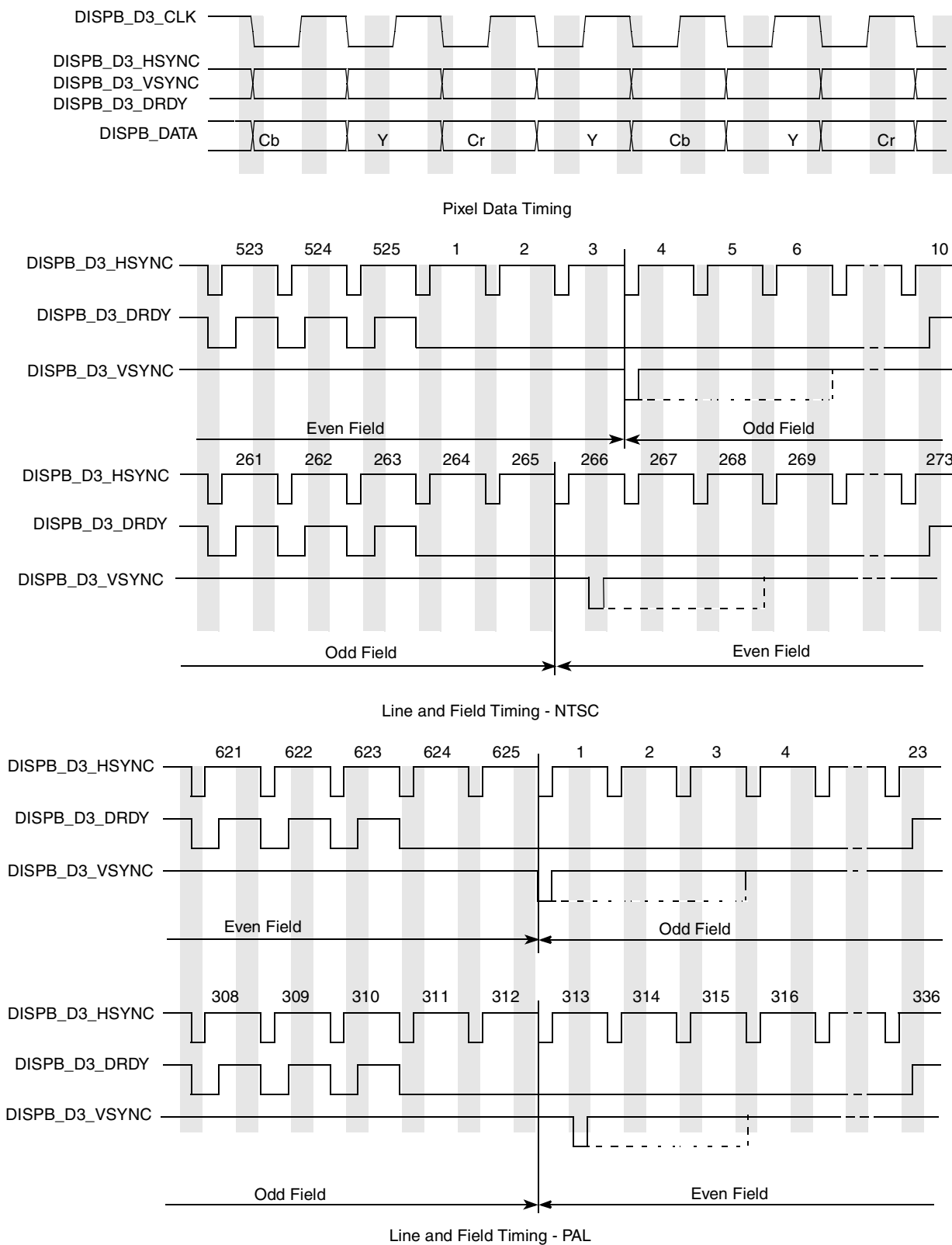


Figure 53. TV Encoder Interface Timing Diagram

4.9.13.3.7 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See [Section 4.9.13.1.5, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”](#)

4.9.13.4 Asynchronous Interfaces

This section discusses the asynchronous parallel and serial interfaces.

4.9.13.4.8 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
 - Type 1 (sampling with the chip select signal) with and without byte enable signals.
 - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
 - Type 1 (sampling with the chip select signal) with or without byte enable signals.
 - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock—The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) or by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals change only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k), and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK—In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode—In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according to the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in [Figure 54](#), [Figure 55](#), [Figure 56](#), and [Figure 57](#). These timing images correspond to active-low DISPB_Dn_CS, DISPB_Dn_WR and DISPB_Dn_RD signals.

Additionally, the IPU allows a programmable pause between two bursts. The pause is defined in the HSP_CLK cycles. It allows the prevention of timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

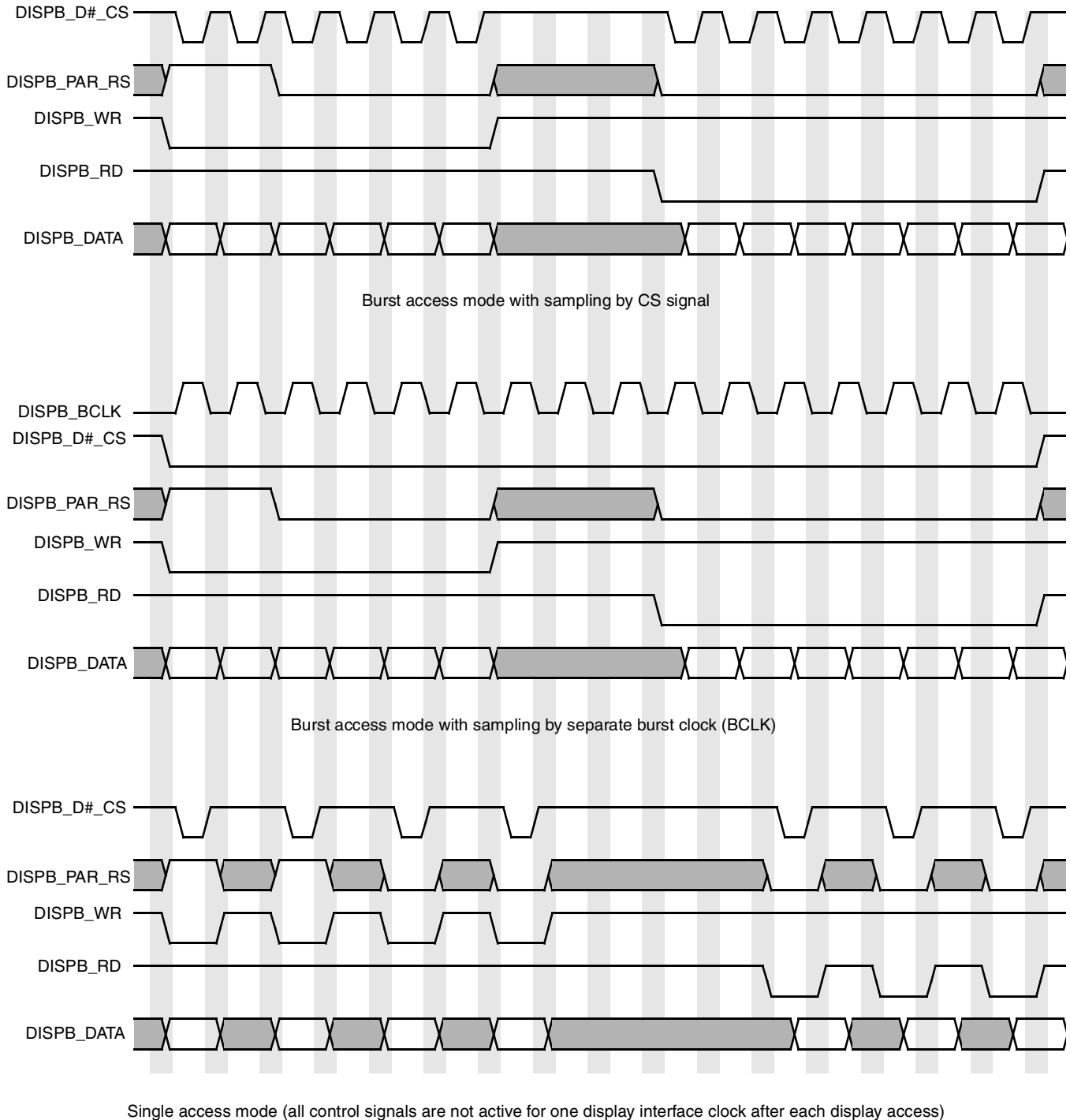


Figure 54. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram

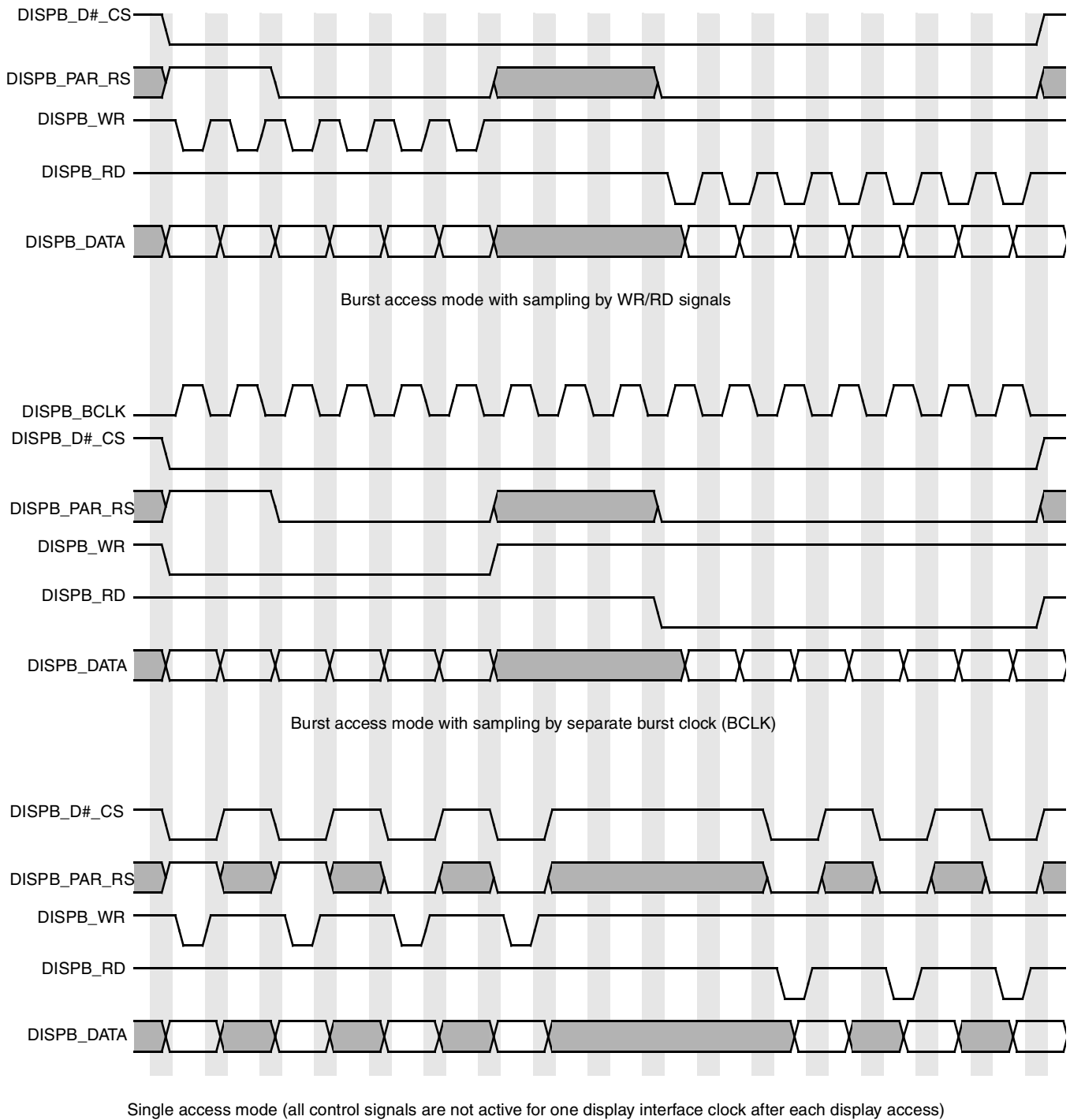
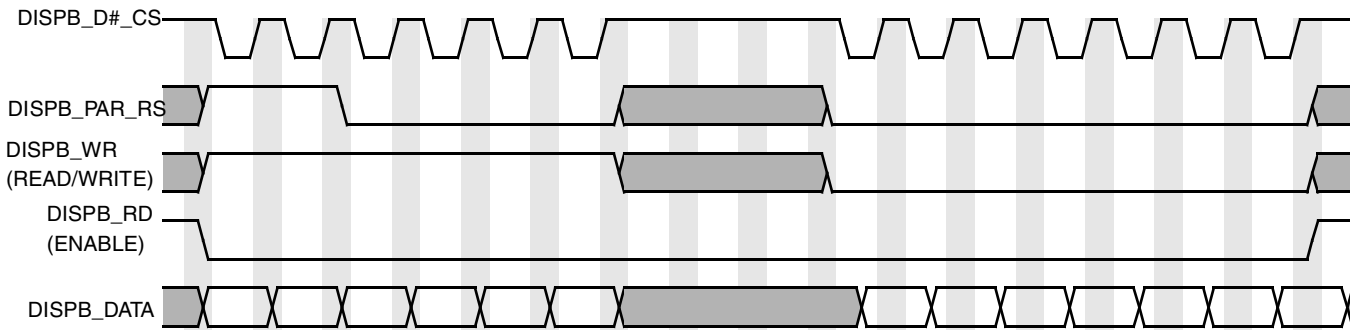
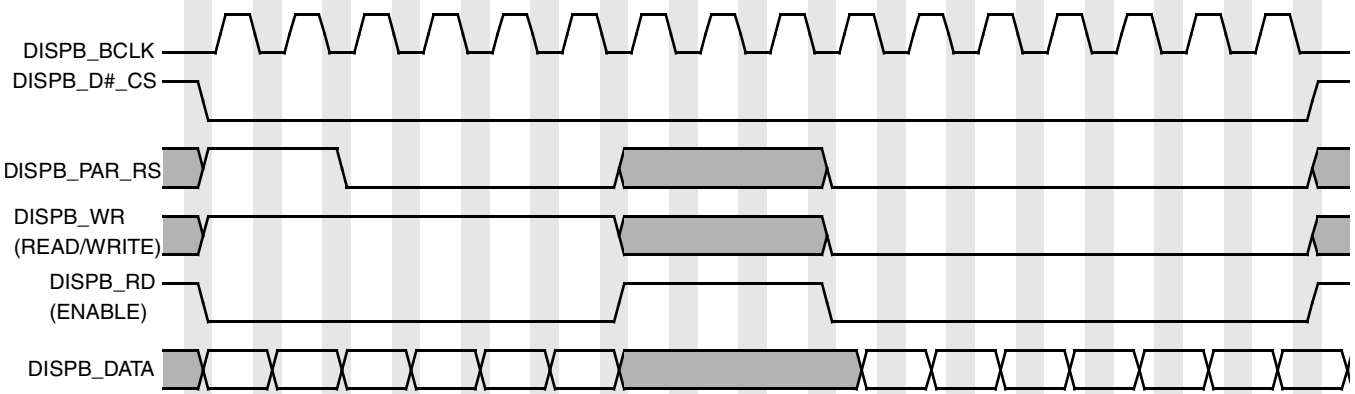


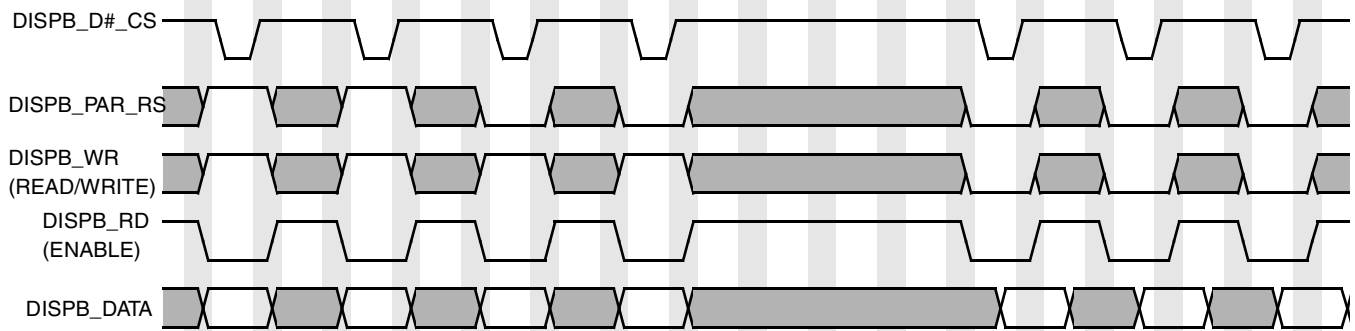
Figure 55. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram



Burst access mode with sampling by CS signal



Burst access mode with sampling by separate burst clock (BCLK)



Single access mode (all control signals are not active for one display interface clock after each display access)

Figure 56. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

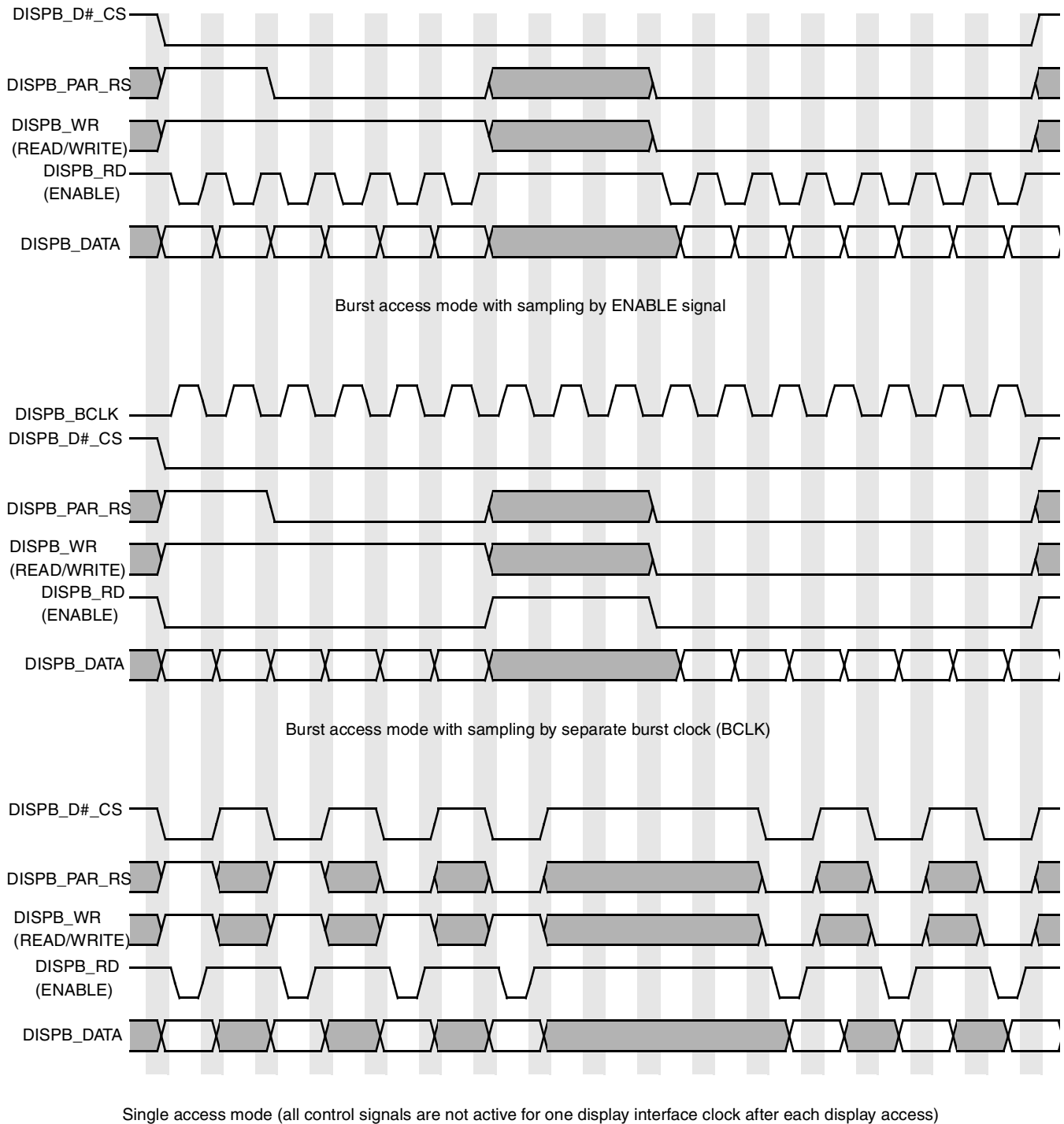


Figure 57. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode Timing Diagram

Display read operation can be performed with wait states when each read access takes up to 4 display interface clock cycles according to the DISPO_RD_WAIT_ST parameter in the

DI_DISP n _TIME_CONF_3 registers ($n = 0,1,2$). Figure 58 shows the timing of the parallel interface with read wait states.

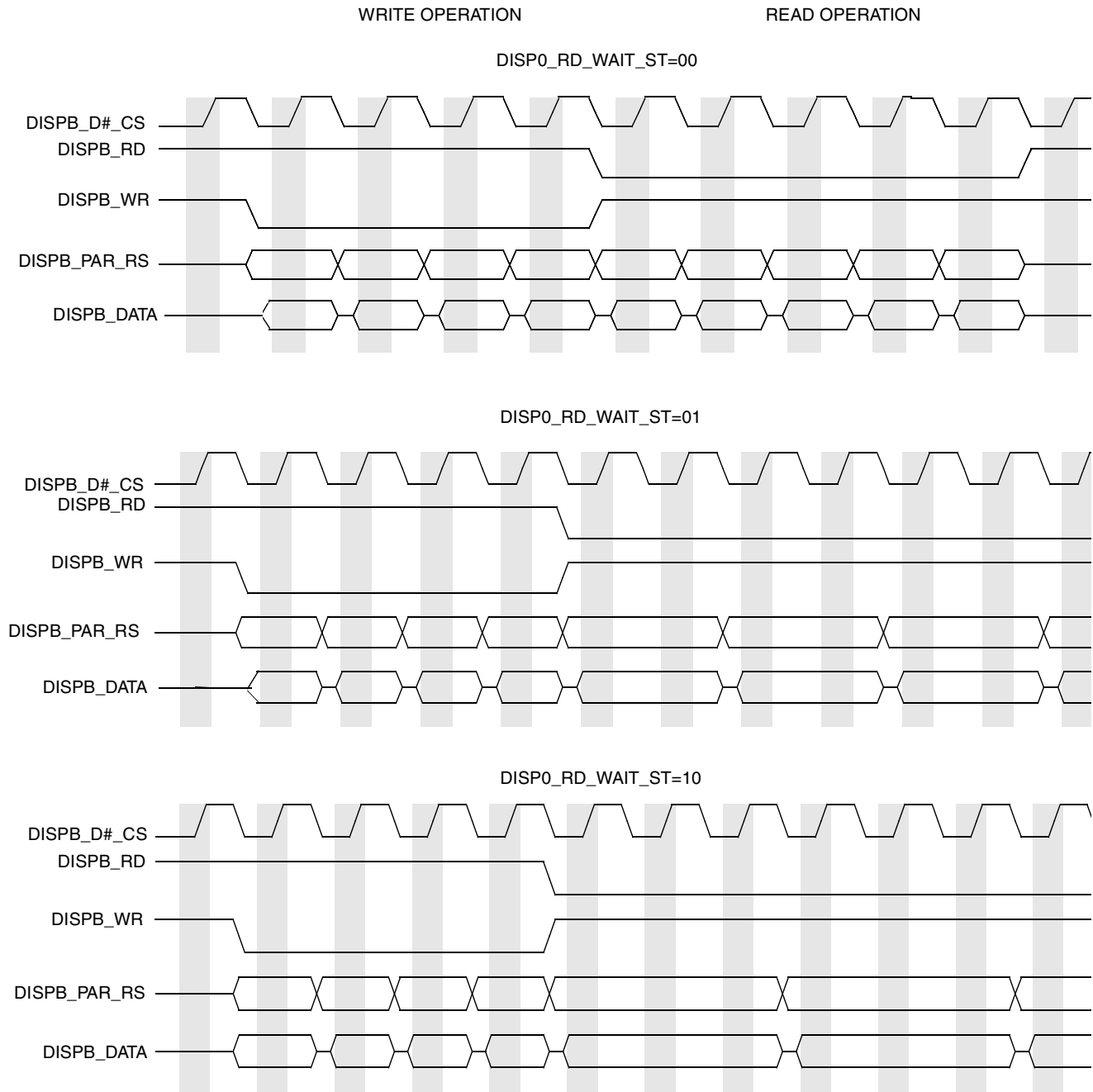


Figure 58. Parallel Interface Timing Diagram—Read Wait States

4.9.13.4.9 Parallel Interfaces, Electrical Characteristics

Figure 59, Figure 61, Figure 60, and Figure 62 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 54 lists the timing parameters at display access level. All

timing images are based on active low control signals (signal polarity is controlled via the DI_DISP_SIG_POL register).

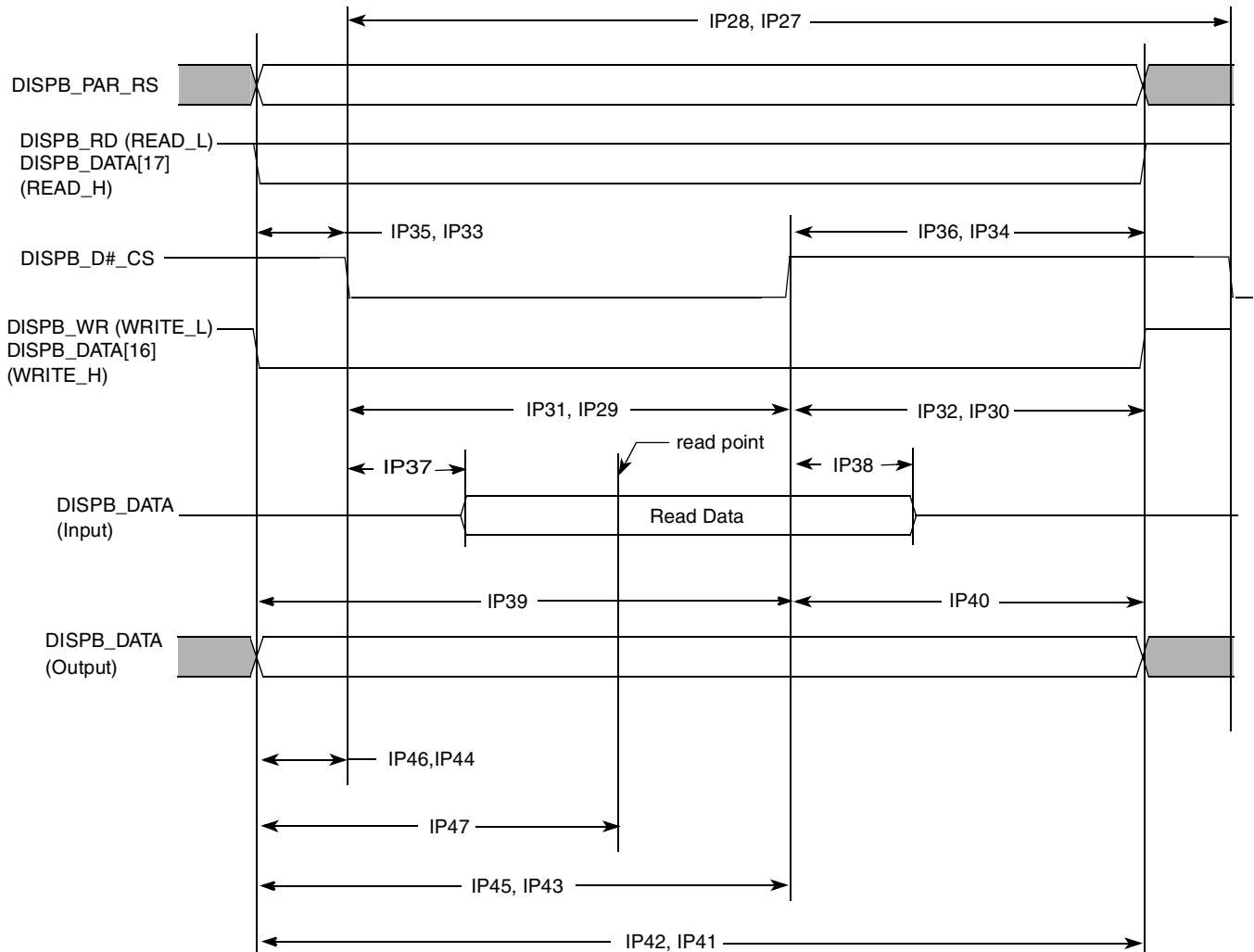


Figure 59. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

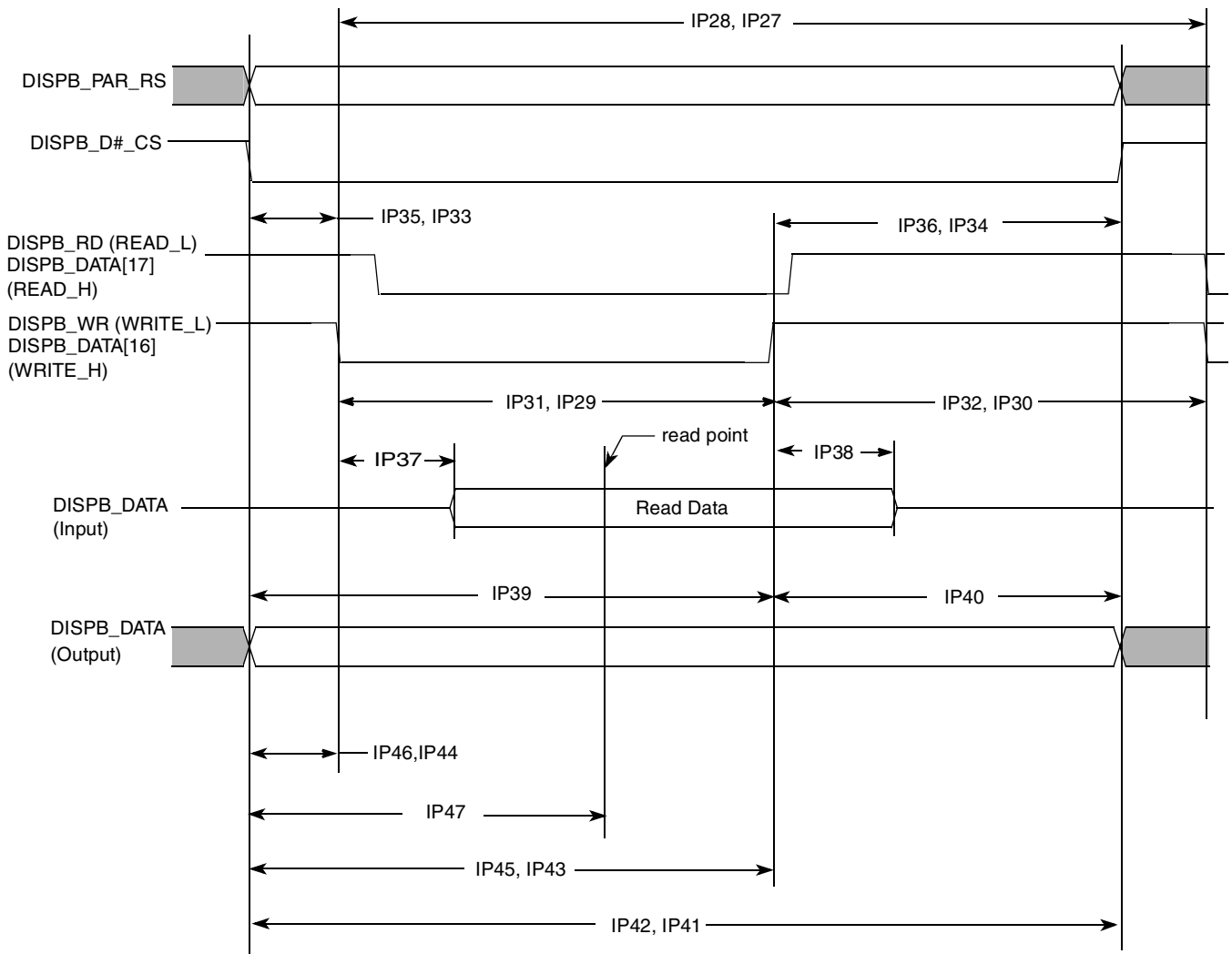


Figure 60. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

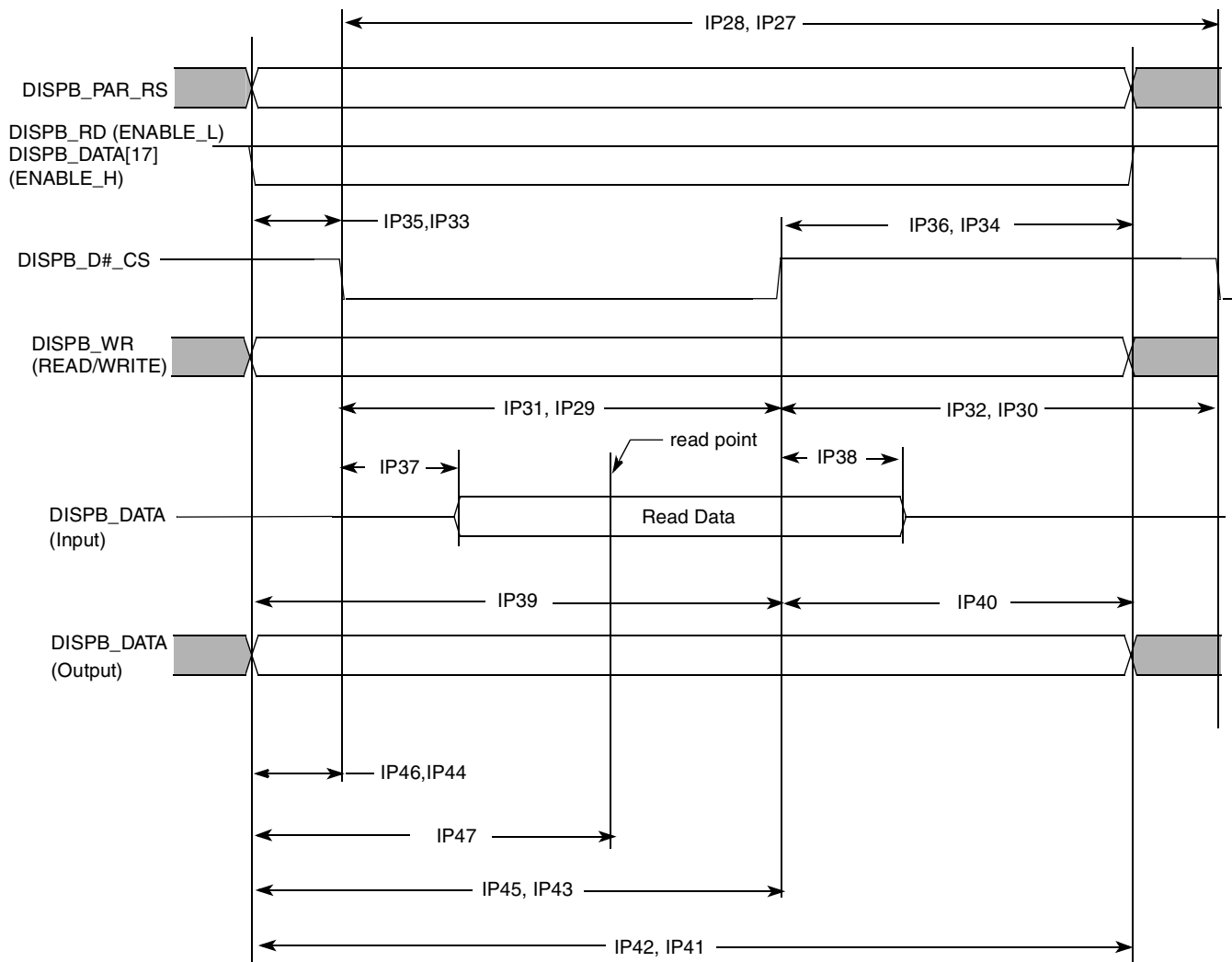


Figure 61. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

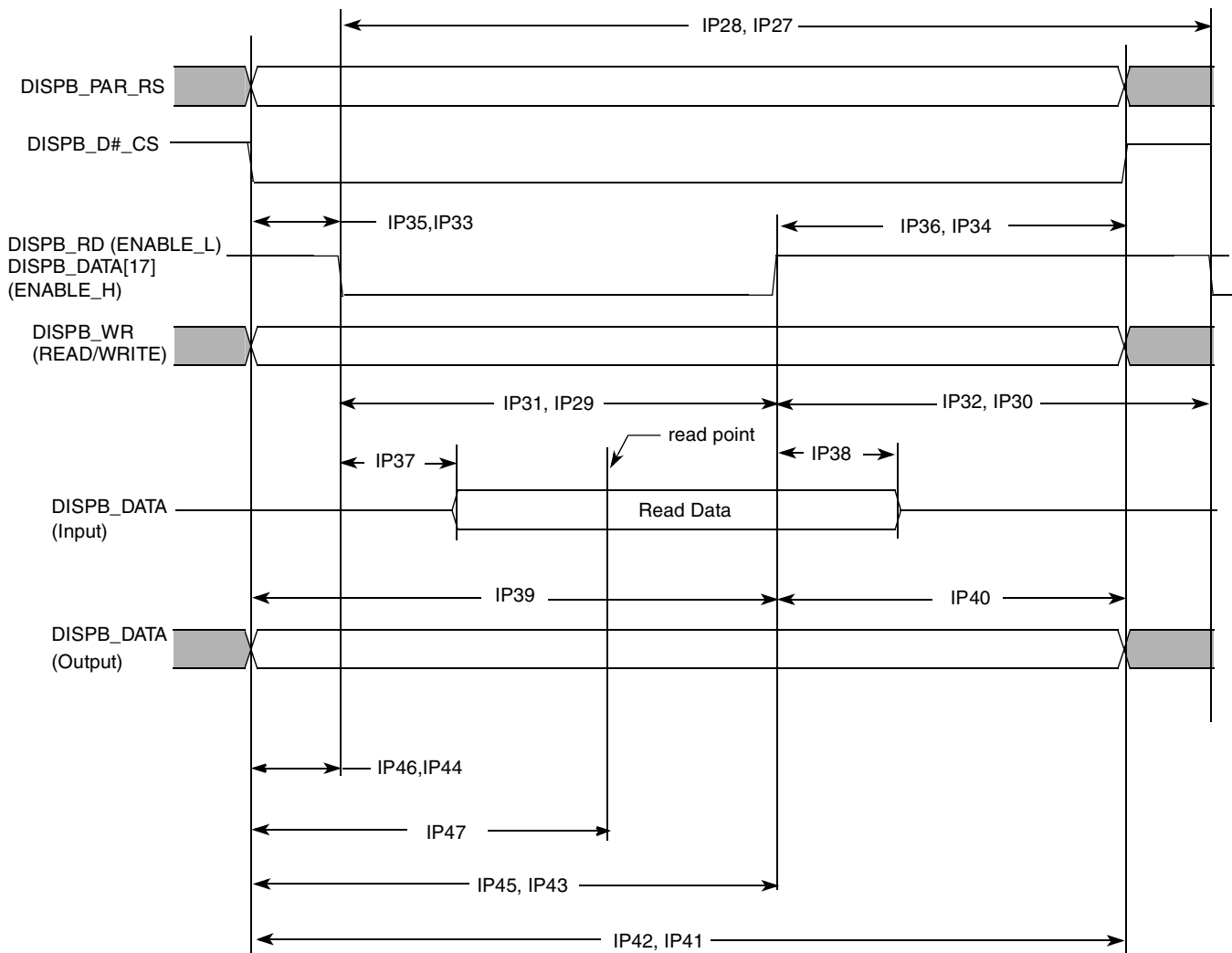


Figure 62. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 54. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr ²	Tdicpr + 1.5	ns
IP28	Write system cycle time	Tcyw	Tdicpw – 1.5	Tdicpw ³	Tdicpw + 1.5	ns
IP29	Read low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr ⁴ – Tdicur ⁵	Tdicdr – Tdicur + 1.5	ns
IP30	Read high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP31	Write low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw ⁶ – Tdicuw ⁷	Tdicdw – Tdicuw + 1.5	ns
IP32	Write high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns

Table 54. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP35	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP36	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP37	Slave device data delay ⁸	Tracc	0	—	Tdrp ⁹ – Tlbd ¹⁰ – Tdicur – 1.5	ns
IP38	Slave device data hold time ⁸	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP39	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP40	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP41	Read period ²	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP42	Write period ³	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP43	Read down time ⁴	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP44	Read up time ⁵	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP45	Write down time ⁶	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP46	Write up time ⁷	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP47	Read time point ⁹	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device-specific.

² Display interface clock period value for read:

$$T_{dicpr} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_IF_CLK_PER_RD}{HSP_CLK_PERIOD} \right]$$

³ Display interface clock period value for write:

$$T_{dicpw} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_IF_CLK_PER_WR}{HSP_CLK_PERIOD} \right]$$

⁴ Display interface clock down time for read:

$$T_{dicdr} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_RD}{HSP_CLK_PERIOD} \right]$$

⁵ Display interface clock up time for read:

$$T_{dicur} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_UP_RD}{HSP_CLK_PERIOD} \right]$$

⁶ Display interface clock down time for write:

$$T_{dicdw} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_WR}{HSP_CLK_PERIOD} \right]$$

⁷ Display interface clock up time for write:

$$T_{dicuw} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_UP_WR}{HSP_CLK_PERIOD} \right]$$

⁸ This parameter is a requirement to the display connected to the IPU

⁹ Data read point

$$T_{drp} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_READ_EN}{HSP_CLK_PERIOD} \right]$$

¹⁰ Loopback delay T_{lbd} is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device – level output delay, board delays, a device – level input delay, an IPU input delay. This value is device specific.

The following parameters are programmed via the `DI_DISP#_TIME_CONF_1`, `DI_DISP#_TIME_CONF_2`, and `DI_HSP_CLK_PER` registers:

- `DISP#_IF_CLK_PER_WR`, `DISP#_IF_CLK_PER_RD`
- `HSP_CLK_PERIOD`
- `DISP#_IF_CLK_DOWN_WR`
- `DISP#_IF_CLK_UP_WR`
- `DISP#_IF_CLK_DOWN_RD`
- `DISP#_IF_CLK_UP_RD`
- `DISP#_READ_EN`

4.9.13.5 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 63 depicts timing of the 3-wire serial interface. The timing images correspond to active-low `DISPB_D#_CS` signal and the straight polarity of the `DISPB_SD_D_CLK` signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (`IPP_IND_DISP_B_SD_D` and `IPP_DO_DISP_B_SD_D`). The I/O mux connects the internal data lines to the bidirectional external line according to the `IPP_OBE_DISP_B_SD_D` signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the `DI_SER_DISPn_CONF` registers ($n = 1, 2$).

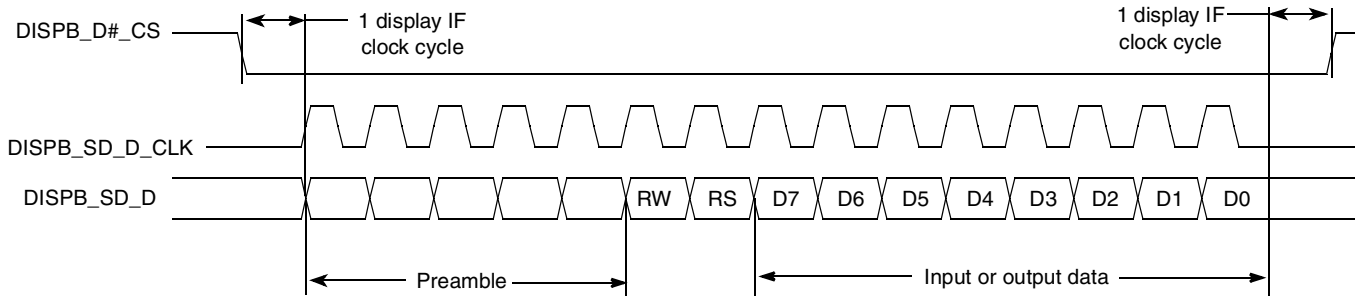


Figure 63. 3-Wire Serial Interface Timing Diagram

Figure 64 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

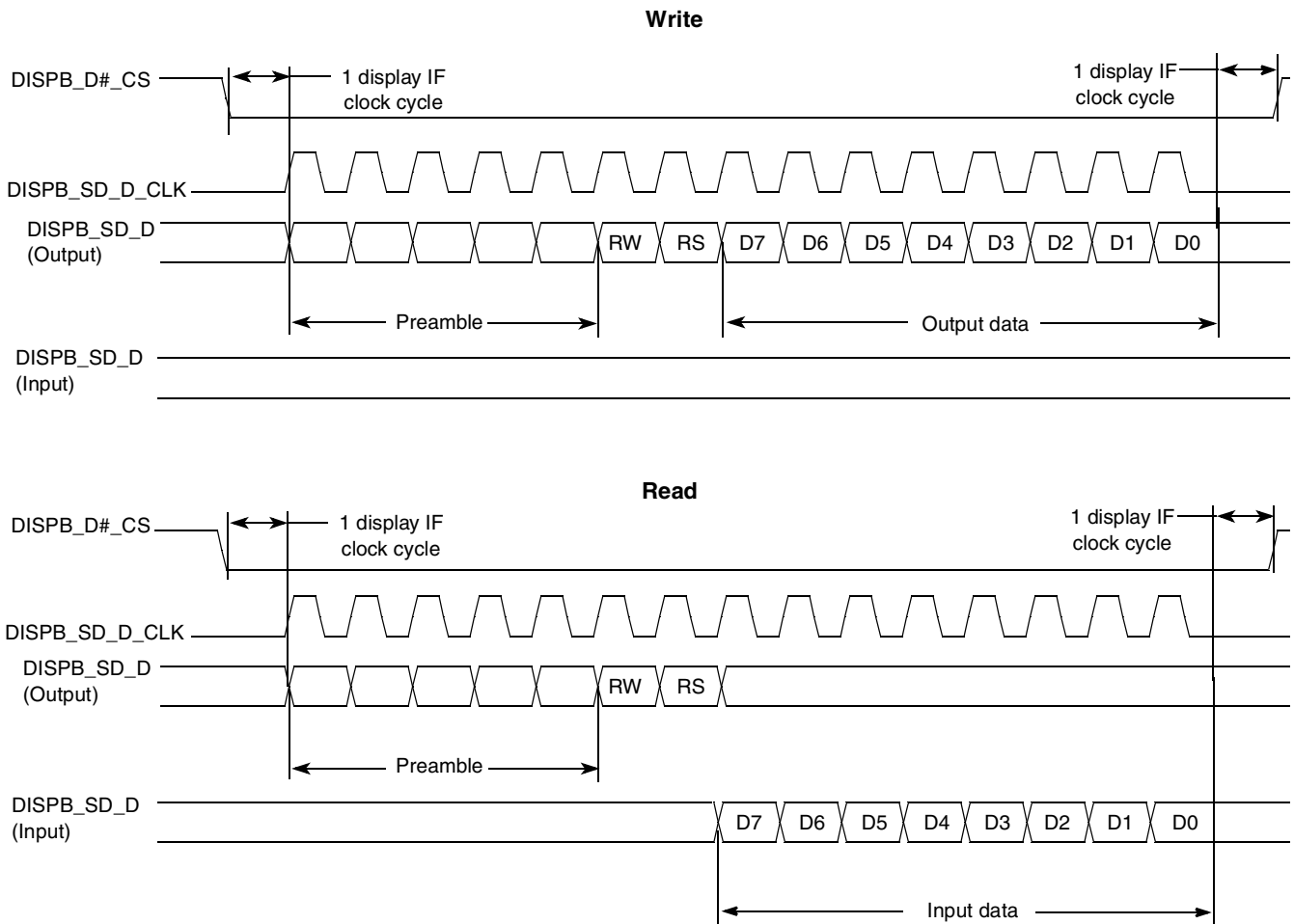


Figure 64. 4-Wire Serial Interface Timing Diagram

Figure 65 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

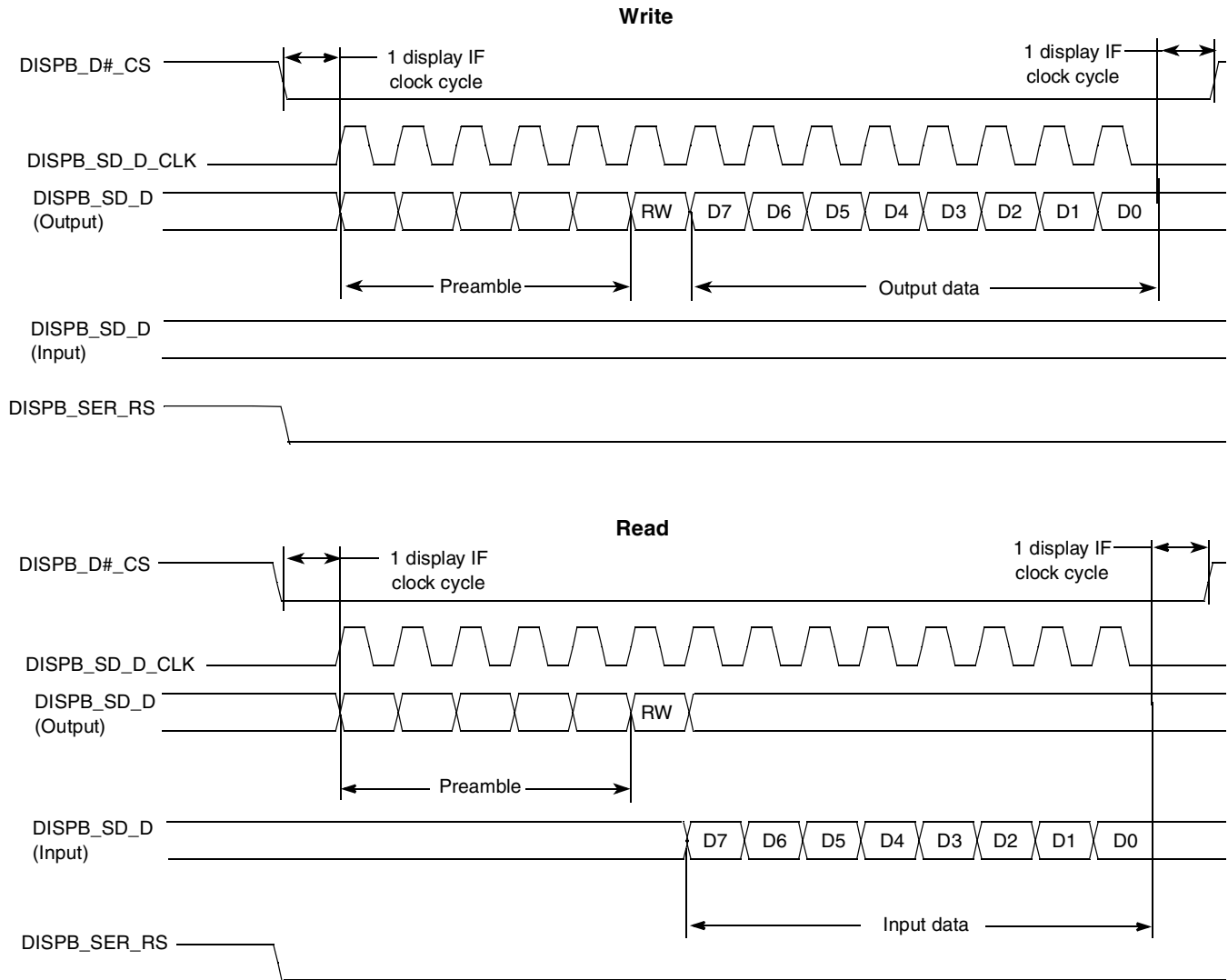


Figure 65. 5-Wire Serial Interface (Type 1) Timing Diagram

Figure 66 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within a single active chip select interval, the RS can be changed at boundaries of words.

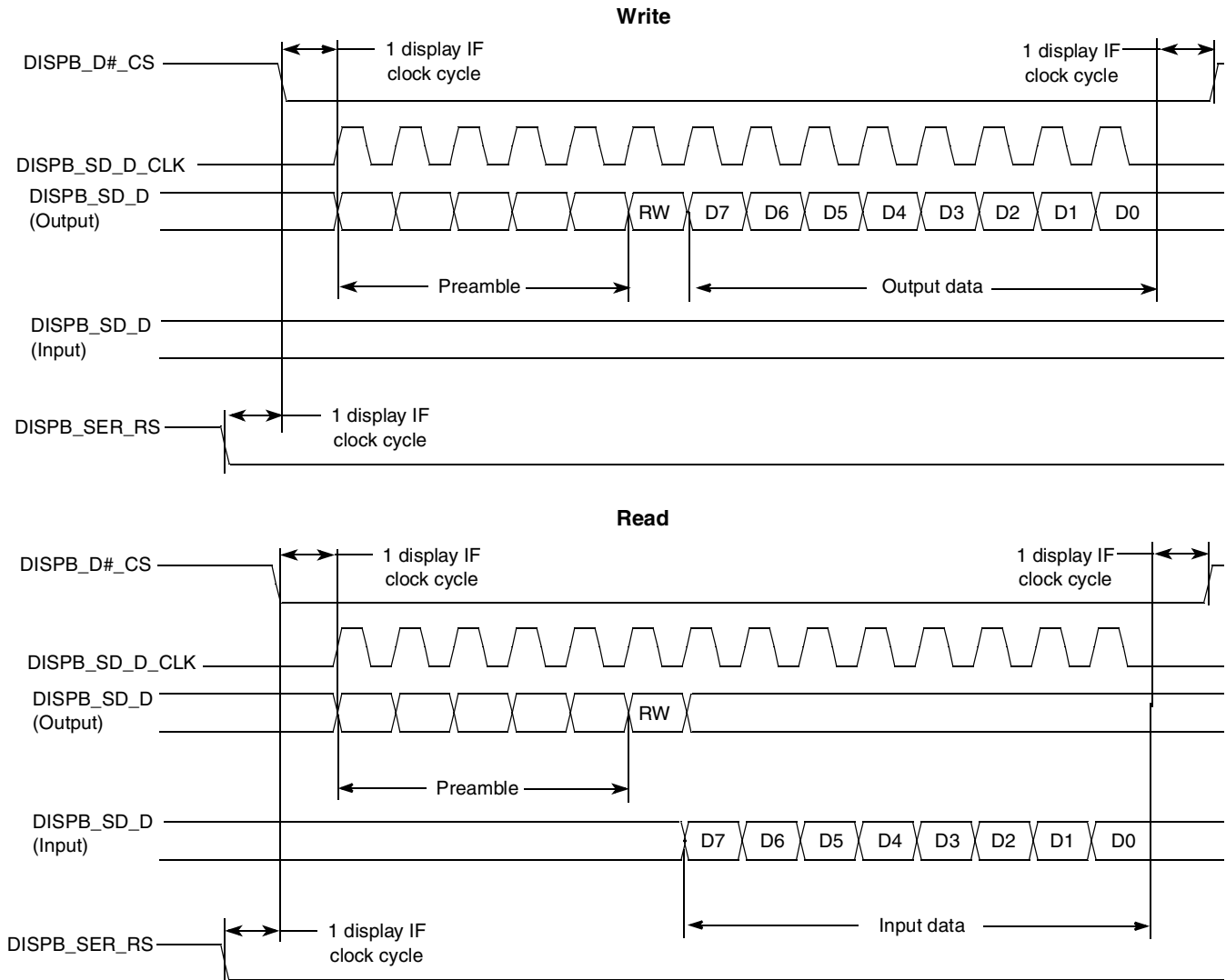


Figure 66. 5-Wire Serial Interface (Type 2) Timing Diagram

4.9.13.5.10 Serial Interfaces, Electrical Characteristics

Figure 67 depicts timing of the serial interface. Table 55 lists the timing parameters at display access level.

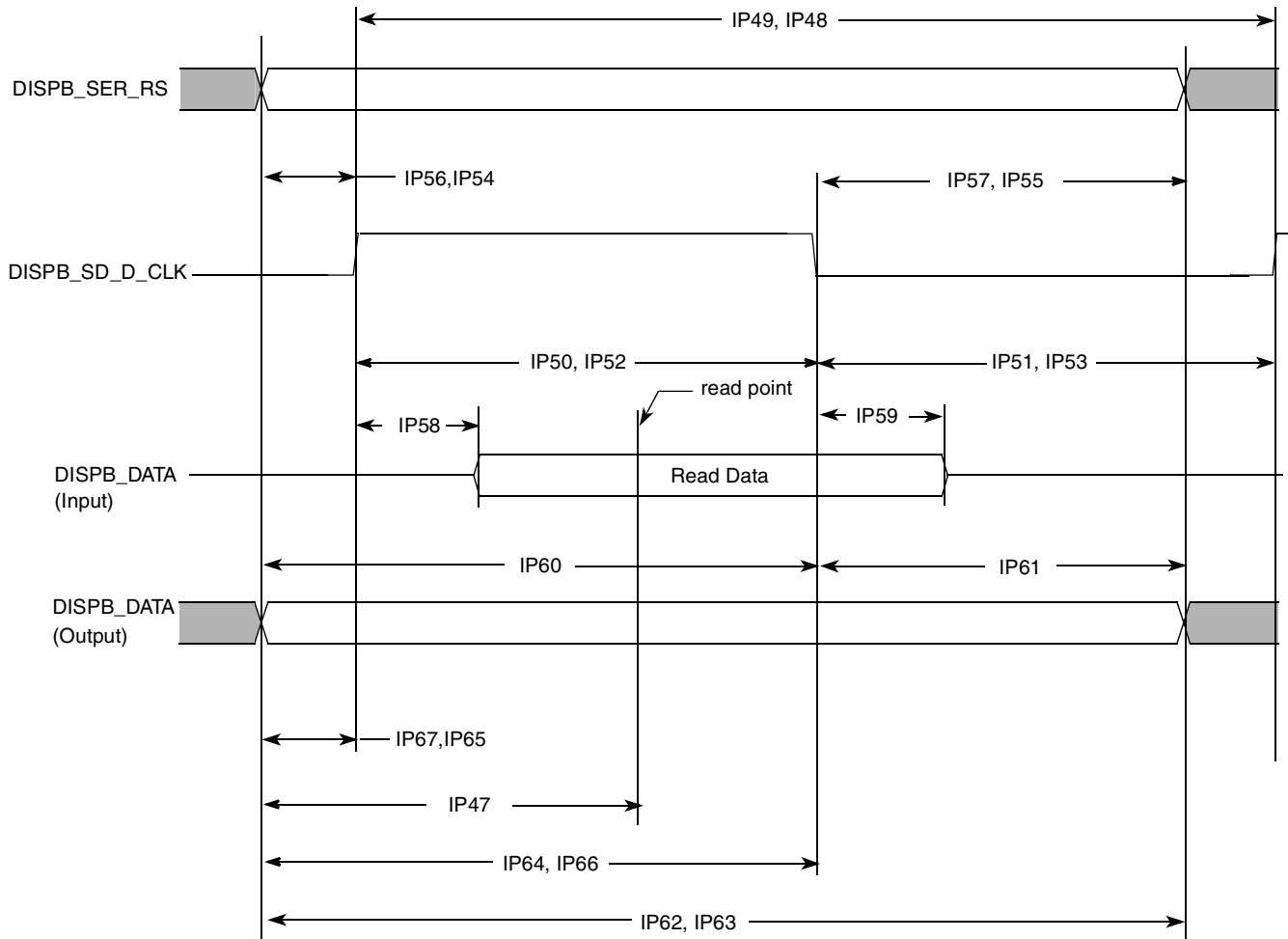


Figure 67. Asynchronous Serial Interface Timing Diagram

Table 55. Asynchronous Serial Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP48	Read system cycle time	Tcycr	Tdicpr – 1.5	Tdicpr ²	Tdicpr + 1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw – 1.5	Tdicpw ³	Tdicpw + 1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr – Tdicur – 1.5	Tdicdr ⁴ – Tdicur ⁵	Tdicdr – Tdicur + 1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr – Tdicdr + Tdicur – 1.5	Tdicpr – Tdicdr + Tdicur	Tdicpr – Tdicdr + Tdicur + 1.5	ns
IP52	Write clock low pulse width	Twl	Tdicdw – Tdicuw – 1.5	Tdicdw ⁶ – Tdicuw ⁷	Tdicdw – Tdicuw + 1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw – Tdicdw + Tdicuw – 1.5	Tdicpw – Tdicdw + Tdicuw	Tdicpw – Tdicdw + Tdicuw + 1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur – 1.5	Tdicur	—	ns

Table 55. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP55	Controls hold time for read	Tdchr	Tdicpr – Tdicdr – 1.5	Tdicpr – Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw – 1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP58	Slave device data delay ⁸	Tracc	0	—	Tdrp ⁹ – Tlbd ¹⁰ – Tdicur – 1.5	ns
IP59	Slave device data hold time ⁸	Troh	Tdrp – Tlbd – Tdicdr + 1.5	—	Tdicpr – Tdicdr – 1.5	ns
IP60	Write data setup time	Tds	Tdicdw – 1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw – Tdicdw – 1.5	Tdicpw – Tdicdw	—	ns
IP62	Read period ²	Tdicpr	Tdicpr – 1.5	Tdicpr	Tdicpr + 1.5	ns
IP63	Write period ³	Tdicpw	Tdicpw – 1.5	Tdicpw	Tdicpw + 1.5	ns
IP64	Read down time ⁴	Tdicdr	Tdicdr – 1.5	Tdicdr	Tdicdr + 1.5	ns
IP65	Read up time ⁵	Tdicur	Tdicur – 1.5	Tdicur	Tdicur + 1.5	ns
IP66	Write down time ⁶	Tdicdw	Tdicdw – 1.5	Tdicdw	Tdicdw + 1.5	ns
IP67	Write up time ⁷	Tdicuw	Tdicuw – 1.5	Tdicuw	Tdicuw + 1.5	ns
IP68	Read time point ⁹	Tdrp	Tdrp – 1.5	Tdrp	Tdrp + 1.5	ns

¹ The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

² Display interface clock period value for read:

$$T_{dicpr} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_IF_CLK_PER_RD}{HSP_CLK_PERIOD} \right]$$

³ Display interface clock period value for write:

$$T_{dicpw} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_IF_CLK_PER_WR}{HSP_CLK_PERIOD} \right]$$

⁴ Display interface clock down time for read:

$$T_{dicdr} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_RD}{HSP_CLK_PERIOD} \right]$$

⁵ Display interface clock up time for read:

$$T_{dicur} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_UP_RD}{HSP_CLK_PERIOD} \right]$$

⁶ Display interface clock down time for write:

$$T_{dicdw} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_WR}{HSP_CLK_PERIOD} \right]$$

⁷ Display interface clock up time for write:

$$T_{dicuw} = \frac{1}{2} T_{HSP_CLK} \cdot \text{ceil} \left[\frac{2 \cdot DISP\#_IF_CLK_UP_WR}{HSP_CLK_PERIOD} \right]$$

⁸ This parameter is a requirement to the display connected to the IPU.

⁹ Data read point:

$$T_{drp} = T_{HSP_CLK} \cdot \text{ceil} \left[\frac{DISP\#_READ_EN}{HSP_CLK_PERIOD} \right]$$

¹⁰ Loopback delay T_{lbd} is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, and an IPU input delay. This value is device specific.

The following parameters are programmed via the `DI_DISP#_TIME_CONF_1`, `DI_DISP#_TIME_CONF_2`, and `DI_HSP_CLK_PER` registers:

- `DISP#_IF_CLK_PER_WR`
- `DISP#_IF_CLK_PER_RD`
- `HSP_CLK_PERIOD`
- `DISP#_IF_CLK_DOWN_WR`
- `DISP#_IF_CLK_UP_WR`
- `DISP#_IF_CLK_DOWN_RD`
- `DISP#_IF_CLK_UP_RD`
- `DISP#_READ_EN`

4.9.14 Memory Stick Host Controller (MSHC)

Figure 68, Figure 69, and Figure 70 depict the MSHC timings, and Table 56 and Table 57 list the timing parameters.

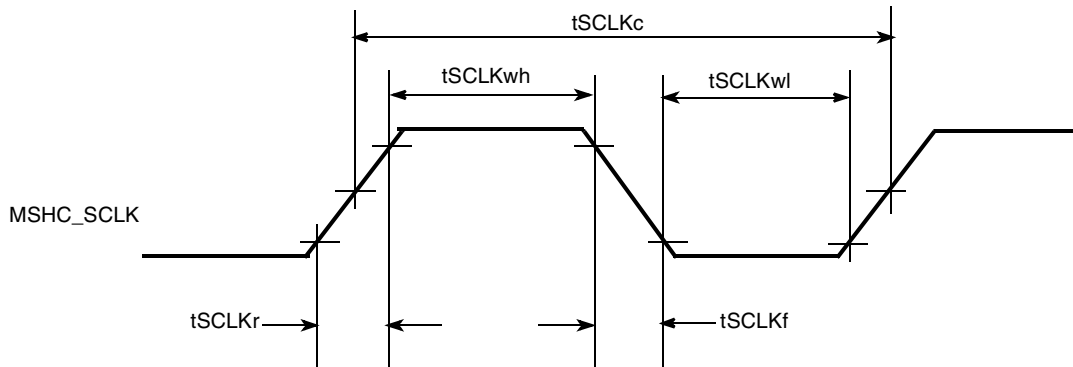


Figure 68. MSHC_CLK Timing Diagram

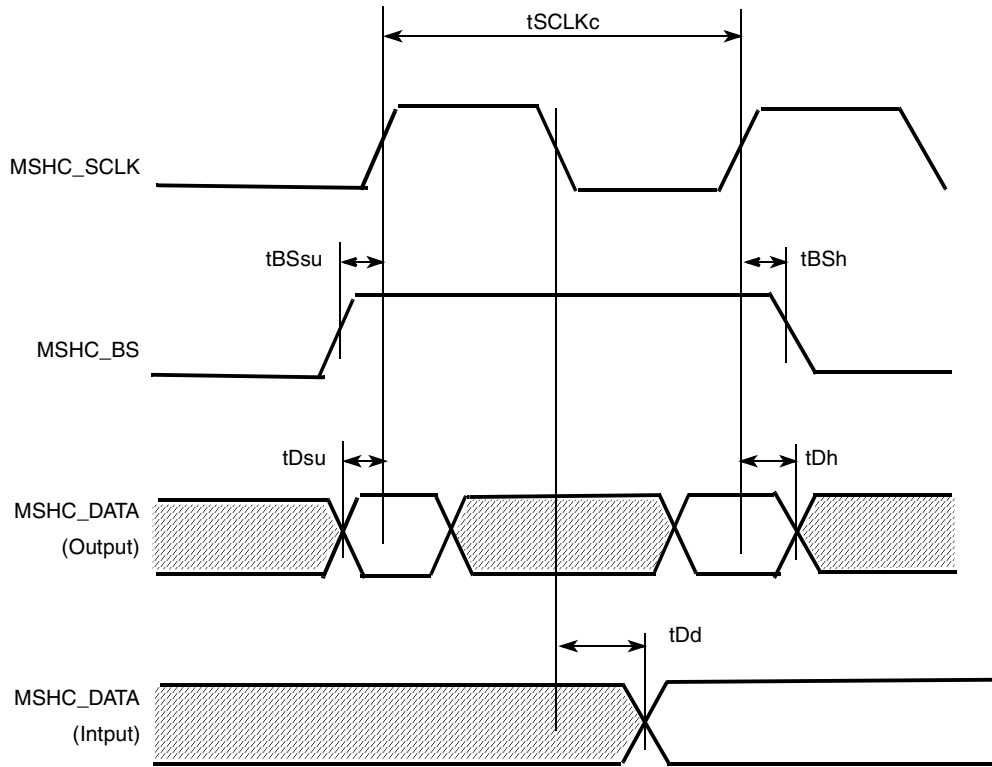


Figure 69. Transfer Operation Timing Diagram (Serial)

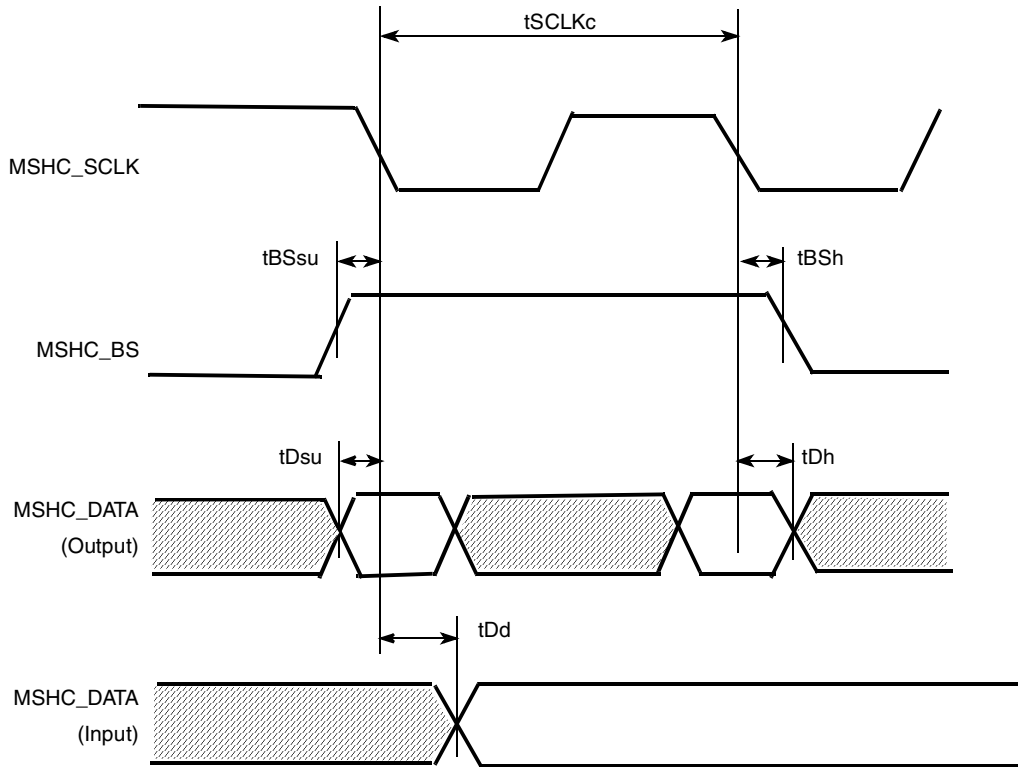


Figure 70. Transfer Operation Timing Diagram (Parallel)

NOTE

The memory stick host controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications*. Tables in this section detail the specifications' requirements for parallel and serial modes, and not the i.MX35 timing.

Table 56. Serial Interface Timing Parameters¹

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns

Table 56. Serial Interface Timing Parameters¹ (continued)

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

¹ Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in [Table 57](#).

Table 57. Parallel Interface Timing Parameters¹

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

¹ Timing is guaranteed for NVCC from 2.7 V through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See the NVCC restrictions described in [Table 7](#).

4.9.15 MediaLB Controller Electrical Specifications

This section describes the electrical information of the MediaLB Controller module.

Table 58. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK operating frequency ¹	f _{mck}	11.264	12.288 24.576	24.6272 25.600	MHz	Min: 256 × Fs at 44.0 kHz Typ: 256 × Fs at 48.0 kHz Typ: 512 × Fs at 48.0 kHz Max: 512 × Fs at 48.1 kHz Max: 512 × Fs PLL unlocked
MLBCLK rise time	t _{mckr}	—	—	3	ns	V _{IL} TO V _{IH}

Table 58. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLB fall time	t_{mckf}	—	—	3	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	— —	81 40	— —	ns	$256 \times F_s$ $512 \times F_s$
MLBCLK low time	t_{mckl}	31.5 30	37 35.5	— —	ns	$256 \times F_s$ $256 \times F_s$ PLL unlocked
		14.5 14	17 16.5	— —	ns	$512 \times F_s$ $512 \times F_s$ PLL unlocked
MLBCLK high time	t_{mckh}	31.5 30	38 36.5	— —	ns	$256 \times F_s$ $256 \times F_s$ PLL unlocked
		14.5 14	17 16.5	— —	ns	$512 \times F_s$ $512 \times F_s$ PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	2	ns pp	Note ²
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	4	—	—	ns	Note ³

¹ The MLB controller can shut off MLBCLK to place MediaLB in a low-power state.

² Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

³ The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; F_s = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below unless otherwise noted.

Table 59. MLB Device 1024Fs Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK Operating Frequency ¹	f_{mck}	45.056	49.152	49.2544 51.200	MHz	Min: $1024 \times F_s$ at 44.0 kHz Typ: $1024 \times F_s$ at 48.0 kHz Max: $1024 \times F_s$ at 48.1 kHz Max: $1024 \times F_s$ PLL unlocked
MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} TO V_{IH}
MLB fall time	t_{mckf}	—	—	1	ns	V_{IH} TO V_{IL}
MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	—
MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	PLL unlocked

Table 59. MLB Device 1024Fs Timing Parameters (continued)

Parameter	Symbol	Min	Typ	Max	Units	Comment
MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	— —	ns	PLL unlocked
MLBCLK pulse width variation	t_{mpwv}	—	—	0.7	ns pp	Note ²
MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
Bus Hold Time	t_{mdzh}	2	—	—	ns	Note ³

¹ The MLB Controller can shut off MLBCLK to place MediaLB in a low-power state.

² Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

³ The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

4.9.16 1-Wire Timing Specifications

Figure 71 depicts the RPP timing, and Table 60 lists the RPP timing parameters.

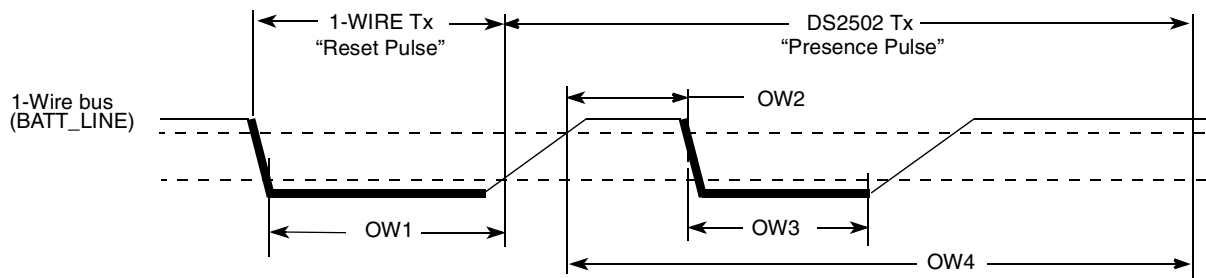


Figure 71. Reset and Presence Pulses (RPP) Timing Diagram

Table 60. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset time low	t_{RSTL}	480	511	—	μ s
OW2	Presence detect high	t_{PDH}	15	—	60	μ s
OW3	Presence detect low	t_{PDL}	60	—	240	μ s
OW4	Reset time high	t_{RSTH}	480	512	—	μ s

Figure 72 depicts write 0 sequence timing, and Table 61 lists the timing parameters.

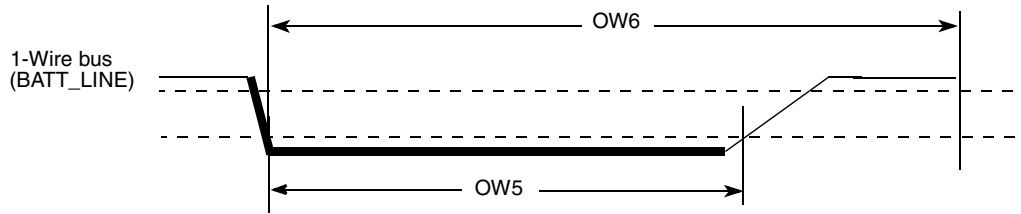


Figure 72. Write 0 Sequence Timing Diagram

Table 61. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 low time	t_{WR0_low}	60	100	120	μs
OW6	Transmission time slot	t_{SLOT}	OW5	117	120	μs

Figure 73 shows write 1 sequence timing, and Figure 74 depicts the read sequence timing. Table 62 lists the timing parameters.

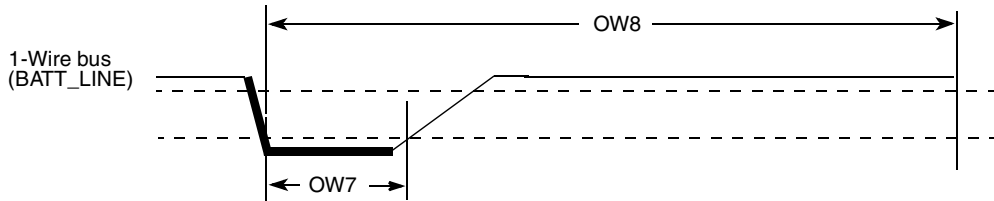


Figure 73. Write 1 Sequence Timing Diagram

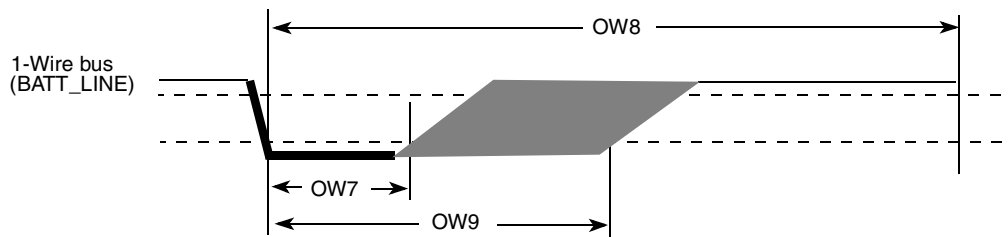


Figure 74. Read Sequence Timing Diagram

Table 62. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1/read low time	t_{LOW1}	1	5	15	μs
OW8	Transmission time slot	t_{SLOT}	60	117	120	μs
OW9	Release time	$t_{RELEASE}$	15	—	45	μs

4.9.17 Parallel ATA Module AC Electrical Specifications

The parallel ATA module can work on PIO/multiword DMA/ultra-DMA transfer modes. Each transfer mode has a different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MBps.

The parallel ATA module interface consists of a total of 29 pins. Some pins have different functions in different transfer modes. There are various requirements for timing relationships among the function pins, in compliance with the ATA/ATAPI-6 specification, and these requirements are configurable by the ATA module registers.

4.9.17.1 General Timing Requirements

Table 63 and Figure 75 define the AC characteristics of the interface signals on all data transfer modes.

Table 63. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	Rising edge slew rate for any signal on the ATA interface ¹	S_{rise}^1	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on the ATA interface ¹	S_{fall}^1	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

¹ SRISE and SFALL meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pF through 40 pF, where all signals have the same capacitive load value.

ATA Interface Signals

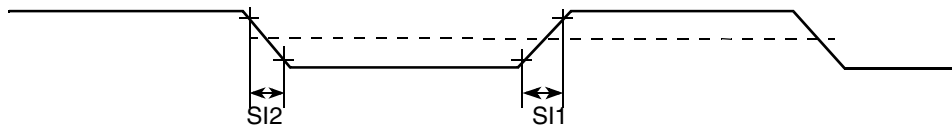


Figure 75. ATA Interface Signals Timing Diagram

4.9.17.2 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA-6 specification.

Level shifters are required for 3.3-V or 5.0-V compatibility on the ATA interface.

The use of bus buffers introduces delays on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. Use of bus buffers is not recommended if fast UDMA mode is required.

The ATA specification imposes a slew rate limit on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Few vendors of bus buffers specify the slew rate of the outgoing signals.

When bus buffers are used the ata_data bus buffer is bidirectional, and uses the direction control signal ata_buffer_en. When ata_buffer_en is asserted, the bus should drive from host to device. When ata_buffer_en is negated, the bus drives from device to host. Steering of the signal is such that contention on the host and device tri-state buses is always avoided.

4.9.17.3 Timing Parameters

Table 64 shows the parameters used in the timing equations. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay, and the cable skew.

Table 64. ATA Timing Parameters

Name	Description	Value/ Contributing Factor ¹
T	Bus clock period (ipg_clk_ata)	Peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Maximum difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Maximum difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Maximum difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver
tbuf	Maximum buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Maximum difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Maximum difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Maximum difference in cable propagation delay without accounting for ground bounce	Cable

¹ Values provided where applicable.

4.9.17.4 PIO Mode Timing

Figure 76 shows timing for PIO read, and Table 65 lists the timing parameters for PIO read.

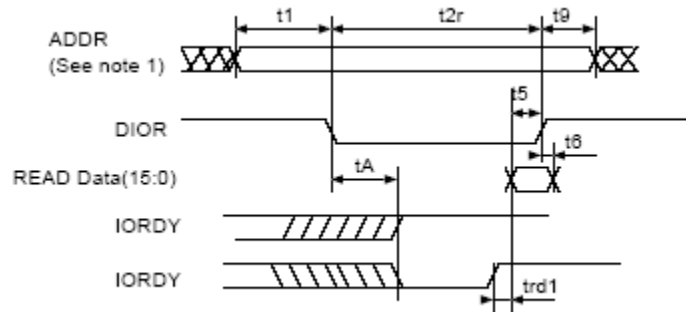


Figure 76. PIO Read Timing Diagram

Table 65. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 76	Value	Controlling Variable
t1	t1	$t1 \text{ (min.)} = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_1
t2	t2r	$t2 \text{ (min.)} = \text{time_2r} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_2r
t9	t9	$t9 \text{ (min.)} = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$	time_3
t5	t5	$t5 \text{ (min.)} = \text{tco} + \text{tsu} + \text{tbuf} + \text{tbuf} + \text{tcable1} + \text{tcable2}$	If not met, increase time_2
t6	t6	0	—
tA	tA	$tA \text{ (min.)} = (1.5 + \text{time_ax}) \times T - (\text{tco} + \text{tsui} + \text{tcable2} + \text{tcable2} + 2 \times \text{tbuf})$	time_ax
trd	trd1	$\text{trd1 (max.)} = (-\text{trd}) + (\text{tskew3} + \text{tskew4})$ $\text{trd1 (min.)} = (\text{time_pio_rdx} - 0.5) \times T - (\text{tsu} + \text{thi})$ $(\text{time_pio_rdx} - 0.5) \times T > \text{tsu} + \text{thi} + \text{tskew3} + \text{tskew4}$	time_pio_rdx
t0	—	$t0 \text{ (min.)} = (\text{time_1} + \text{time_2} + \text{time_9}) \times T$	time_1, time_2r, time_9

Figure 77 shows timing for PIO write, and Table 66 lists the timing parameters for PIO write.

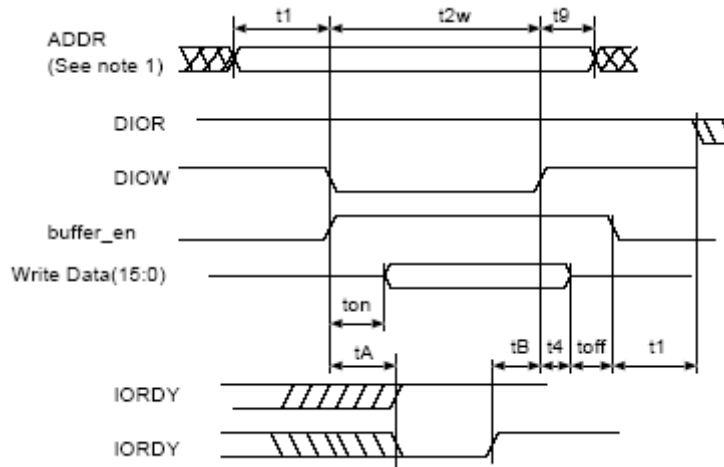


Figure 77. PIO Write Timing Diagram

Table 66. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 77	Value	Controlling Variable
t1	t1	$t1 \text{ (min.)} = \text{time_1} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_1
t2	t2w	$t2 \text{ (min.)} = \text{time_2w} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_2w
t9	t9	$t9 \text{ (min.)} = \text{time_9} \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$	time_9
t3	—	$t3 \text{ (min.)} = (\text{time_2w} - \text{time_on}) \times T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	If not met, increase time_2w
t4	t4	$t4 \text{ (min.)} = \text{time_4} \times T - \text{tskew1}$	time_4
tA	tA	$tA = (1.5 + \text{time_ax}) \times T - (\text{tco} + \text{tsui} + \text{tcable2} + \text{tcable2} + 2 \times \text{tbuf})$	time_ax
t0	—	$t0 \text{ (min.)} = (\text{time_1} + \text{time_2} + \text{time_9}) \times T$	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

Figure 78 shows timing for MDMA read, and Figure 79 shows timing for MDMA write. Table 67 lists the timing parameters for MDMA read and write.

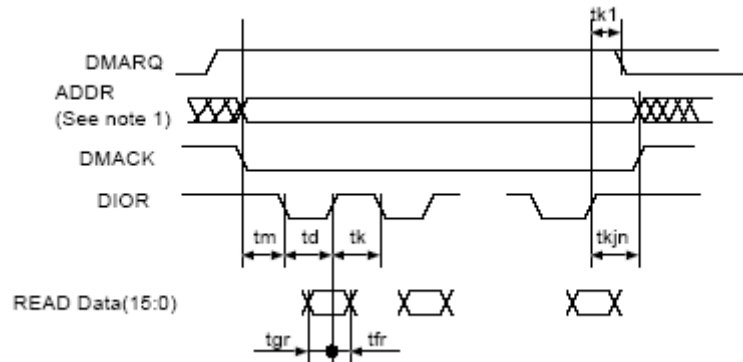


Figure 78. MDMA Read Timing Diagram

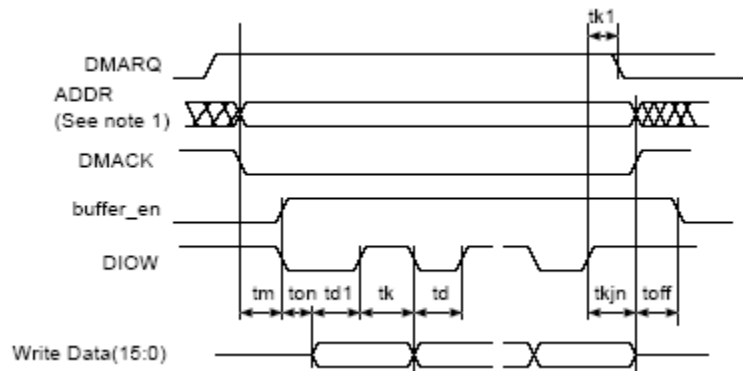


Figure 79. MDMA Write Timing Diagram

Table 67. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79	Value	Controlling Variable
tm, ti	tm	$tm \text{ (min.)} = ti \text{ (min.)} = time_m \times T - (tskew1 + tskew2 + tskew5)$	time_m
td	td, td1	$td1 \text{ (min.)} = td \text{ (min.)} = time_d \times T - (tskew1 + tskew2 + tskew6)$	time_d
tk	tk	$tk \text{ (min.)} = time_k \times T - (tskew1 + tskew2 + tskew6)$	time_k
t0	—	$t0 \text{ (min.)} = (time_d + time_k) \times T$	time_d, time_k
tg(read)	tgr	$tgr \text{ (min. - read)} = tco + tsu + tbuf + tbuf + tcable1 + tcable2$ $tgr \text{ (min. - drive)} = td - te \text{ (drive)}$	time_d
tf(read)	tfr	$tfr \text{ (min. - drive)} = 0$	—
tg(write)	—	$tg \text{ (min. - write)} = time_d \times T - (tskew1 + tskew2 + tskew5)$	time_d
tf(write)	—	$tf \text{ (min. - write)} = time_k \times T - (tskew1 + tskew2 + tskew6)$	time_k
tL	—	$tL \text{ (max.)} = (time_d + time_k - 2) \times T - (tsu + tco + 2 \times tbuf + 2 \times tcable2)$	time_d, time_k

Table 67. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 78, Figure 79	Value	Controlling Variable
tn, tj	tkjn	$tn = tj = tkjn = (\max(\text{time_k}, \text{time_jn}) \times T - (\text{tskew1} + \text{tskew2} + \text{tskew6}))$	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.9.17.5 UDMA-In Timing

Figure 80 shows timing when the UDMA-in transfer starts, Figure 81 shows timing when the UDMA-in host terminates transfer, Figure 82 shows timing when the UDMA-in device terminates transfer, and Table 68 lists the timing parameters for the UDMA-in burst.

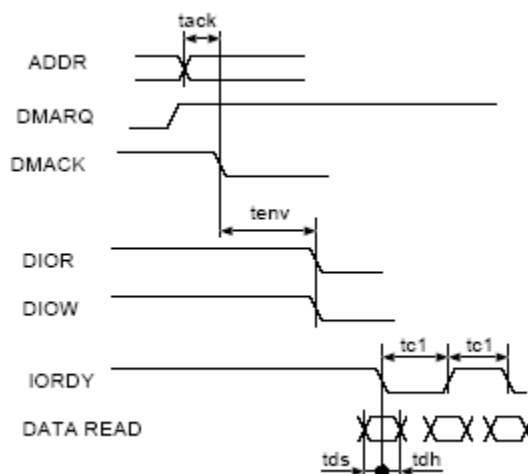


Figure 80. UDMA-In Transfer Starts Timing Diagram

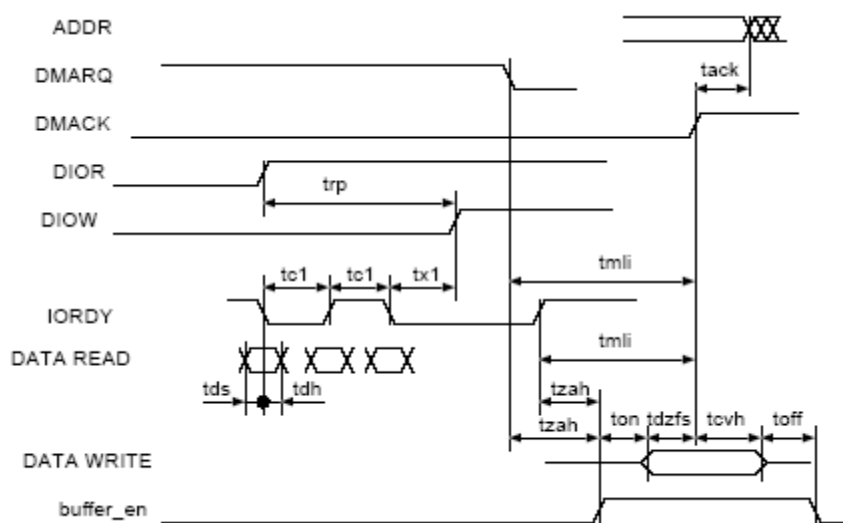


Figure 81. UDMA-In Host Terminates Transfer Timing Diagram

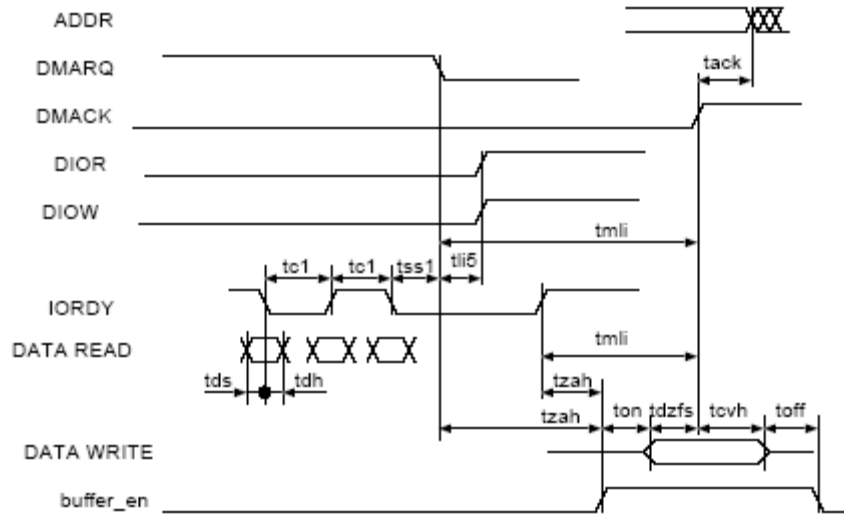


Figure 82. UDMA-In Device Terminates Transfer Timing Diagram

Table 68. UDMA-In Burst Timing Parameters

ATA Parameter	Parameters from Figure 80, Figure 81, Figure 82	Description	Controlling Variable
tack	tack	$tack (min.) = (time_ack \times T) - (tskew1 + tskew2)$	time_ack
tenv	tenv	$tenv (min.) = (time_env \times T) - (tskew1 + tskew2)$ $tenv (max.) = (time_env \times T) + (tskew1 + tskew2)$	time_env
tds	tds1	$tds - (tskew3) - ti_ds > 0$	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	$tdh - (tskew3) - ti_dh > 0$	
tcyc	tc1	$(tcyc - tskew) > T$	T big enough
trp	trp	$trp (min.) = time_rp \times T - (tskew1 + tskew2 + tskew6)$	time_rp
—	tx1 ¹	$(time_rp \times T) - (tco + tsu + 3T + 2 \times tbuf + 2 \times tcable2) > trfs (drive)$	time_rp
tml1	tml1	$tml1 (min.) = (time_mlix + 0.4) \times T$	time_mlix
tzah	tzah	$tzah (min.) = (time_zah + 0.4) \times T$	time_zah
tdzfs	tdzfs	$tdzfs = (time_dzfs \times T) - (tskew1 + tskew2)$	time_dzfs
tcvh	tcvh	$tcvh = (time_cvh \times T) - (tskew1 + tskew2)$	time_cvh
—	ton toff	$ton = time_on \times T - tskew1$ $toff = time_off \times T - tskew1$	—

¹ There is a special timing requirement in the ATA host that requires the internal DIOV to go high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.
2. Make ton and toff large enough to avoid bus contention.

4.9.17.6 UDMA-Out Timing

Figure 83 shows timing when the UDMA-out transfer starts, Figure 84 shows timing when the UDMA-out host terminates transfer, Figure 85 shows timing when the UDMA-out device terminates transfer, and Table 69 lists the timing parameters for the UDMA-out burst.

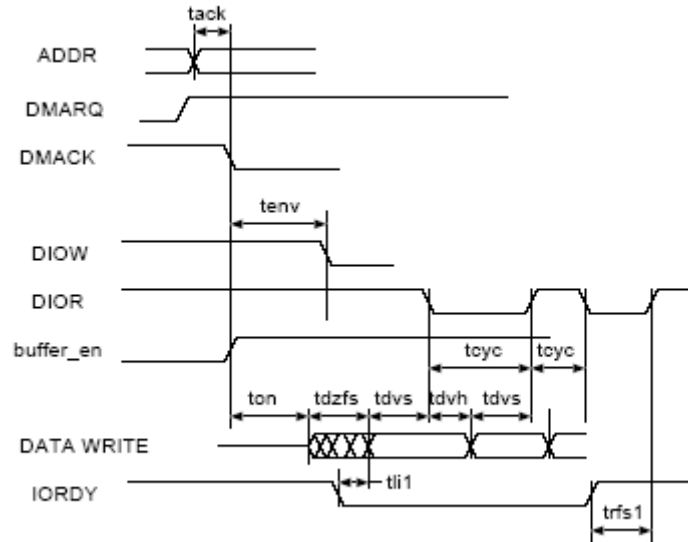


Figure 83. UDMA-Out Transfer Starts Timing Diagram

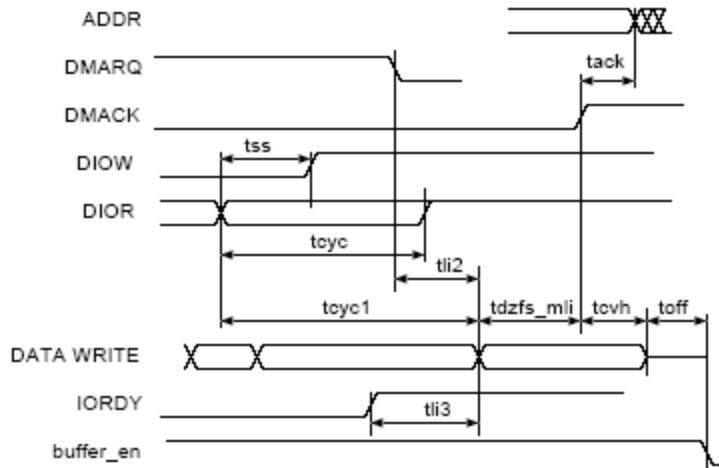


Figure 84. UDMA-Out Host Terminates Transfer Timing Diagram

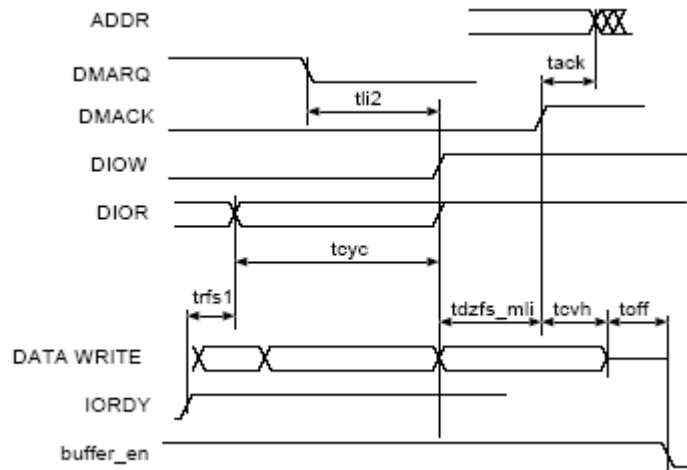


Figure 85. UDMA-Out Device Terminates Transfer Timing Diagram

Table 69. UDMA-Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 83, Figure 84, Figure 85	Value	Controlling Variable
tack	tack	$tack \text{ (min.)} = (\text{time_ack} \times T) - (\text{tskew1} + \text{tskew2})$	time_ack
tenv	tenv	$tenv \text{ (min.)} = (\text{time_env} \times T) - (\text{tskew1} + \text{tskew2})$ $tenv \text{ (max.)} = (\text{time_env} \times T) + (\text{tskew1} + \text{tskew2})$	time_env
tdvs	tdvs	$tdvs = (\text{time_dvs} \times T) - (\text{tskew1} + \text{tskew2})$	time_dvs
tdvh	tdvh	$tdvs = (\text{time_dvh} \times T) - (\text{tskew1} + \text{tskew2})$	time_dvh
tcyc	tcyc	$tcyc = \text{time_cyc} \times T - (\text{tskew1} + \text{tskew2})$	time_cyc
t2cyc	—	$t2cyc = \text{time_cyc} \times 2 \times T$	time_cyc
trfs1	trfs	$trfs = 1.6 \times T + \text{tsui} + \text{tco} + \text{tbuf} + \text{tbuf}$	—
—	tdzfs	$tdzfs = \text{time_dzfs} \times T - (\text{tskew1})$	time_dzfs
tss	tss	$tss = \text{time_ss} \times T - (\text{tskew1} + \text{tskew2})$	time_ss
tmli	tdzfs_mli	$tdzfs_mli = \max. (\text{time_dzfs}, \text{time_mli}) \times T - (\text{tskew1} + \text{tskew2})$	—
tli	tli1	$tli1 > 0$	—
tli	tli2	$tli2 > 0$	—
tli	tli3	$tli3 > 0$	—
tcvh	tcvh	$tcvh = (\text{time_cvh} \times T) - (\text{tskew1} + \text{tskew2})$	time_cvh
—	ton toff	$ton = \text{time_on} \times T - \text{tskew1}$ $toff = \text{time_off} \times T - \text{tskew1}$	—

4.9.18 Parallel Interface (ULPI) Timing

Electrical and timing specifications of the parallel interface are presented in the subsequent sections.

Table 70. Signal Definitions—Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to the clock.
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

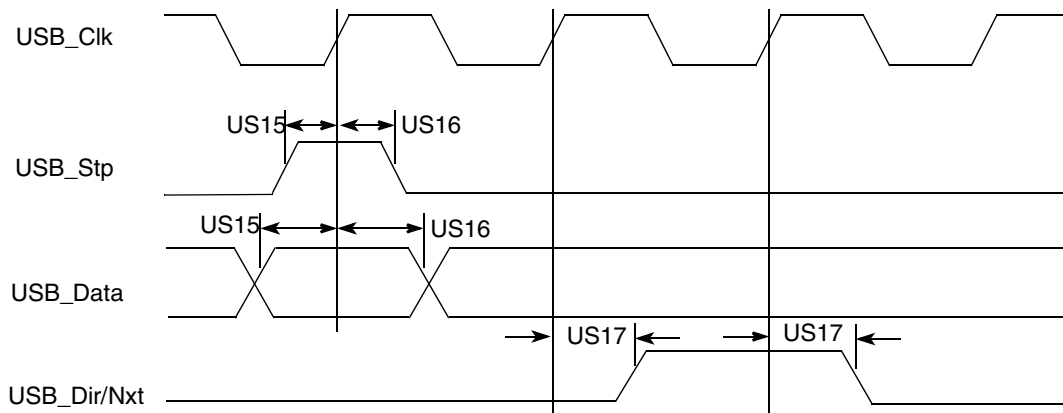


Figure 86. USB Transmit/Receive Waveform in Parallel Mode

Table 71. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Min.	Max.	Unit	Conditions / Reference Signal
US15	USB_TXOE_B	—	6.0	ns	10 pF
US16	USB_DAT_VP	—	0.0	ns	10 pF
US17	USB_SE0_VM	—	9.0	ns	10 pF

4.9.19 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external

pin. The modulated signal of the module is observed at this pin. It can be viewed as a clock signal whose period and duty cycle can be varied with different settings of the PWM. The smallest period is two ipg_clk periods with duty cycle of 50 percent.

4.9.20 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 87 depicts the SJC test clock input timing. Figure 88 depicts the SJC boundary scan timing, Figure 89 depicts the SJC test access port, Figure 90 depicts the SJC TRST timing, and Table 72 lists the SJC timing parameters.

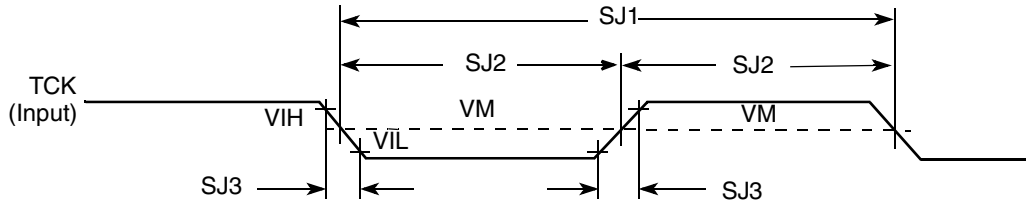


Figure 87. Test Clock Input Timing Diagram

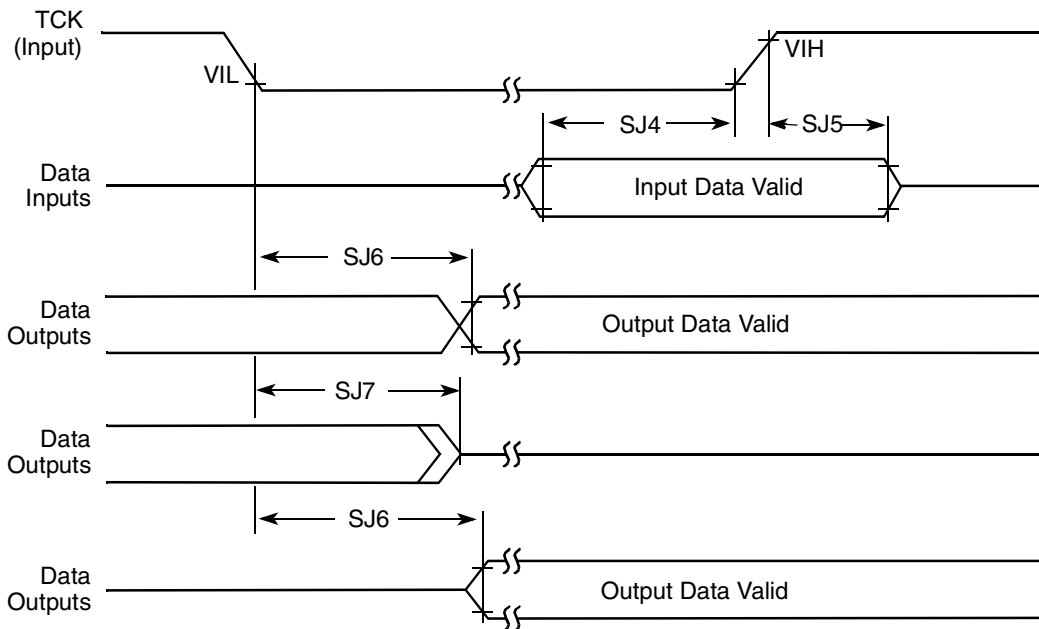


Figure 88. Boundary Scan (JTAG) Timing Diagram

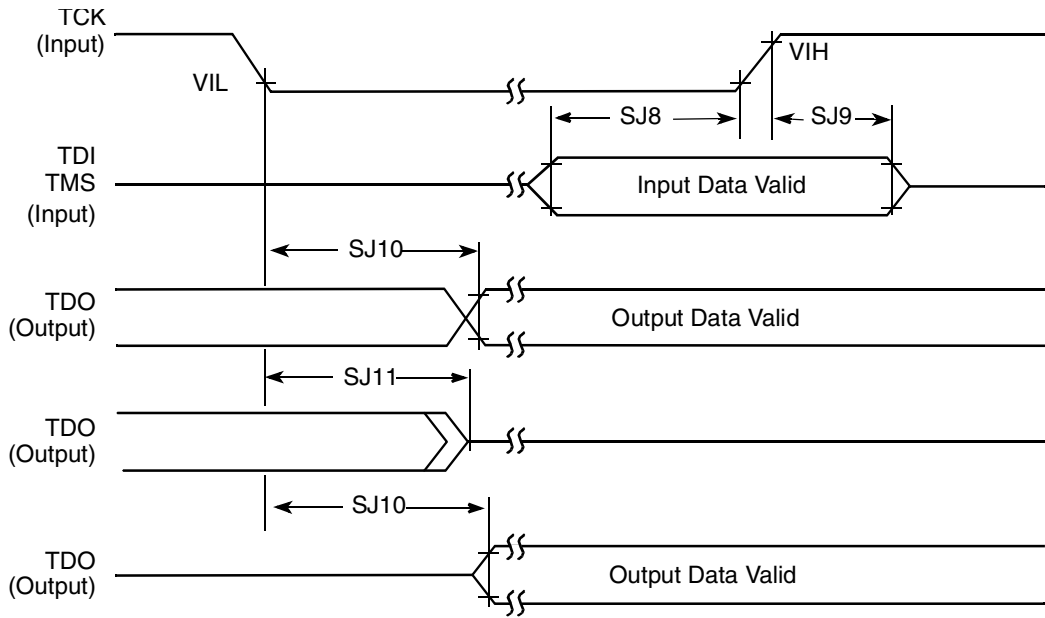


Figure 89. Test Access Port Timing Diagram

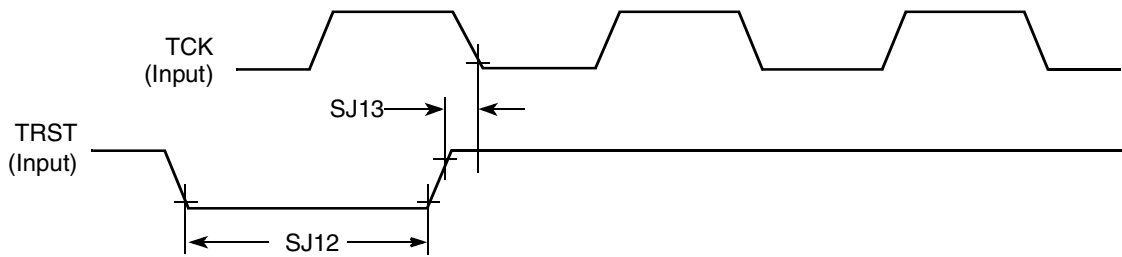


Figure 90. TRST Timing Diagram

Table 72. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100 ¹	—	ns
SJ2	TCK clock pulse width measured at V_M^2	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

Table 72. SJC Timing Parameters (continued)

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

¹ On cases where SDMA TAP is put in the chain, the max. TCK frequency is limited by max. ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max. frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

² V_M = mid point voltage

4.9.21 SPDIF Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Figure 91 shows SPDIF timing parameters, including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK). for SPDIF in Tx mode.

Table 73. SPDIF Timing Parameters

Parameters	Symbol	Timing Parameter Range		Units
		Min.	Max.	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50 pf)	—	—	1.5	ns
• Skew	—	—	24.2	
• Transition rising	—	—	31.3	
• Transition falling	—	—	—	
SPDIFOUT1 output (Load = 30 pf)	—	—	1.5	ns
• Skew	—	—	13.6	
• Transition rising	—	—	18.0	
• Transition falling	—	—	—	
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

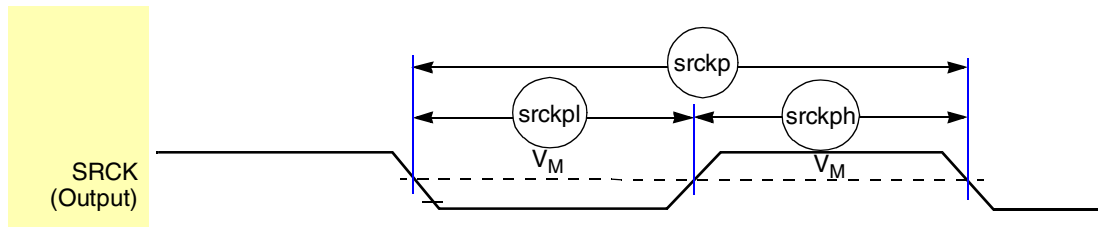


Figure 91. SRCK Timing

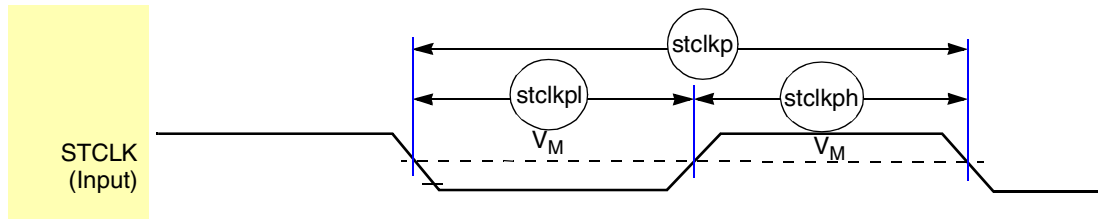


Figure 92. STCLK Timing

4.9.22 SSI Electrical Specifications

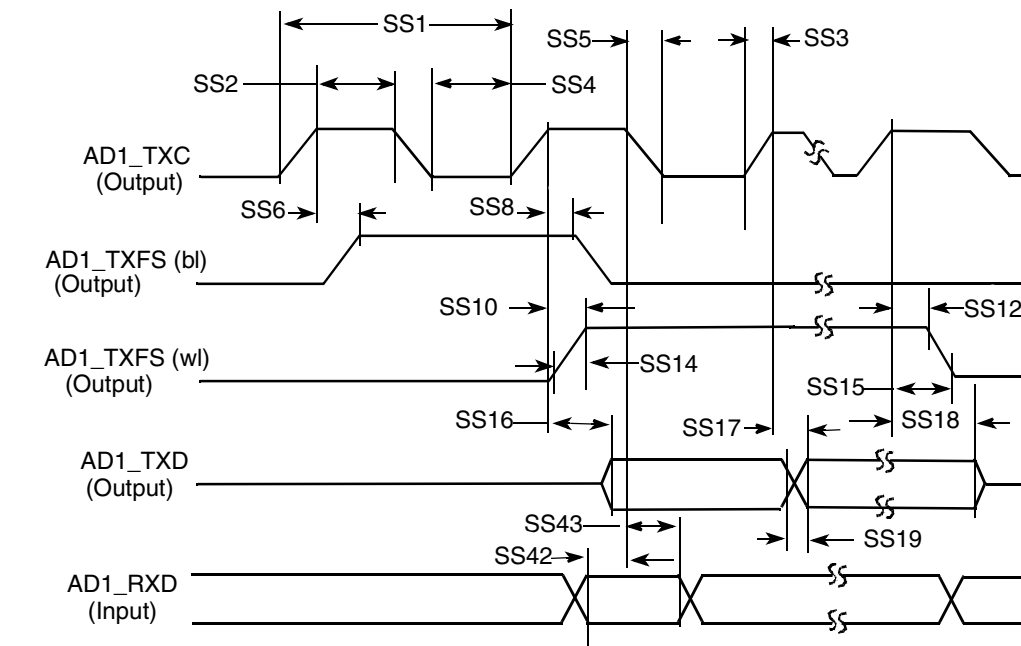
This section describes electrical characteristics of the SSI.

NOTE

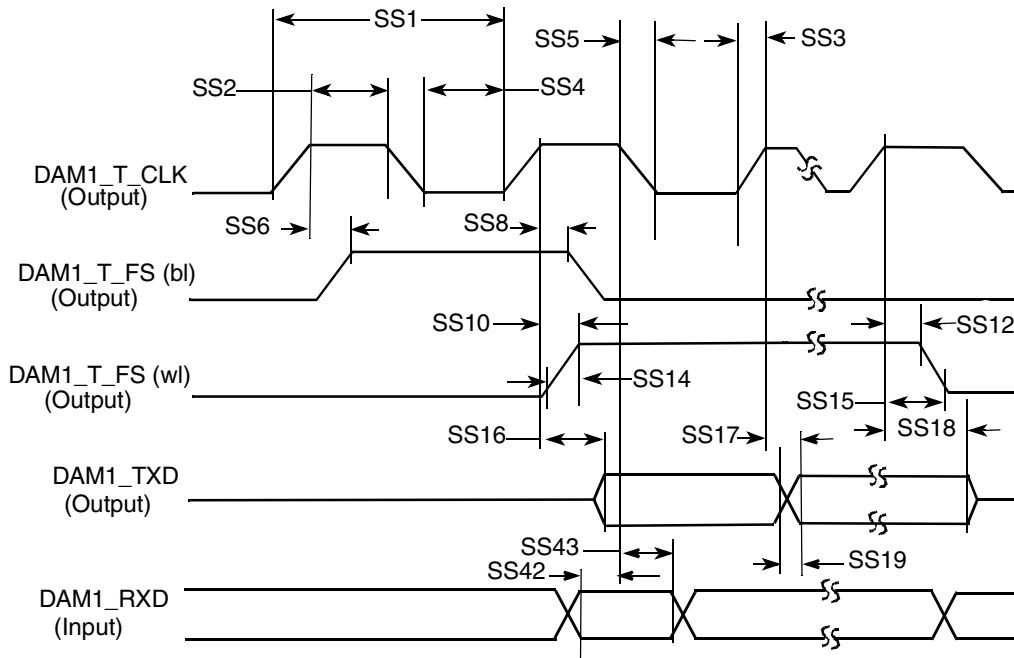
- All of the timing for the SSI is given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timing is on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the transmit and receive sections of the SSI, respectively.
- For internal frame sync operations using the external clock, the FS timing will be the same as that of Tx Data (for example, during AC97 mode of operation).

4.9.22.1 SSI Transmitter Timing with Internal Clock

Figure 93 depicts the SSI transmitter timing with internal clock, and Table 74 lists the timing parameters.



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 93. SSI Transmitter with Internal Clock Timing Diagram

Table 74. SSI Transmitter with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6	ns
SS15	(Tx/Rx) Internal FS fall time	—	6	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0	—	ns
SS52	Loading	—	25	pF

4.9.22.2 SSI Receiver Timing with Internal Clock

Figure 94 depicts the SSI receiver timing with internal clock. Table 75 lists the timing parameters shown in Figure 94.

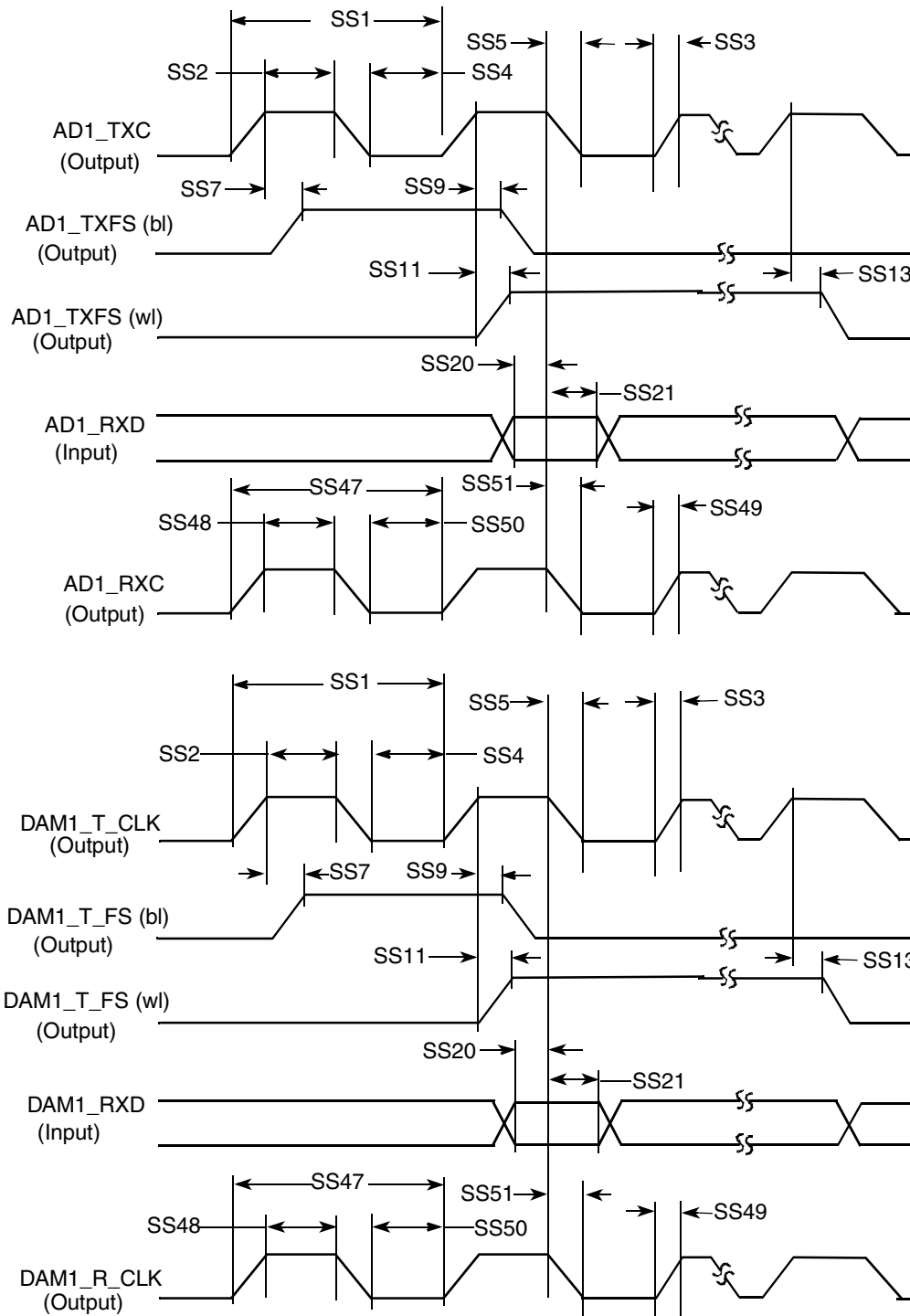


Figure 94. SSI Receiver with Internal Clock Timing Diagram

Table 75. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

4.9.22.3 SSI Transmitter Timing with External Clock

Figure 95 depicts the SSI transmitter timing with external clock, and Table 76 lists the timing parameters.

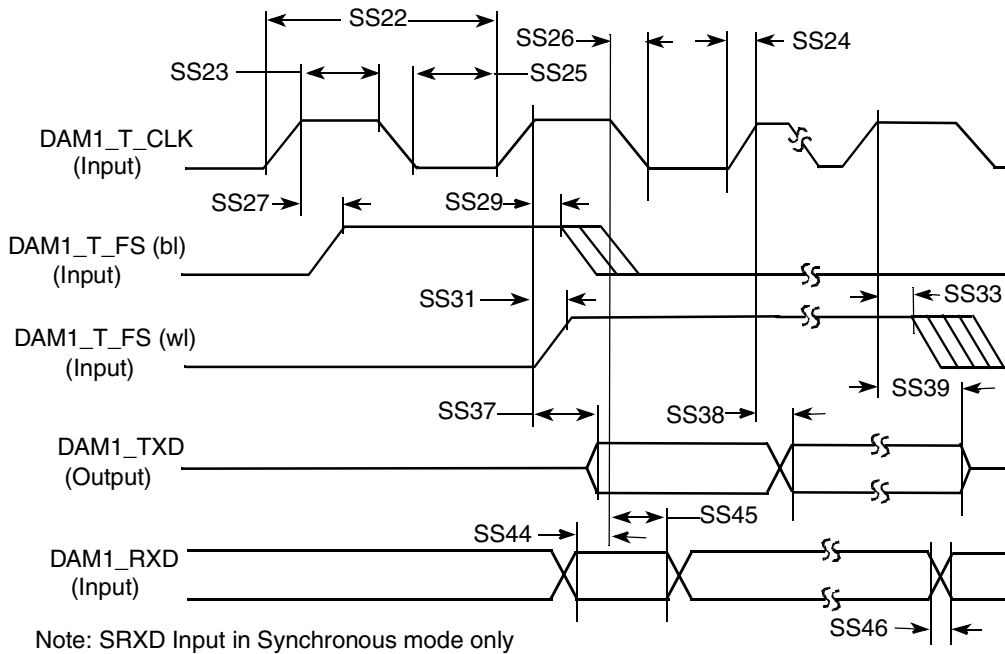
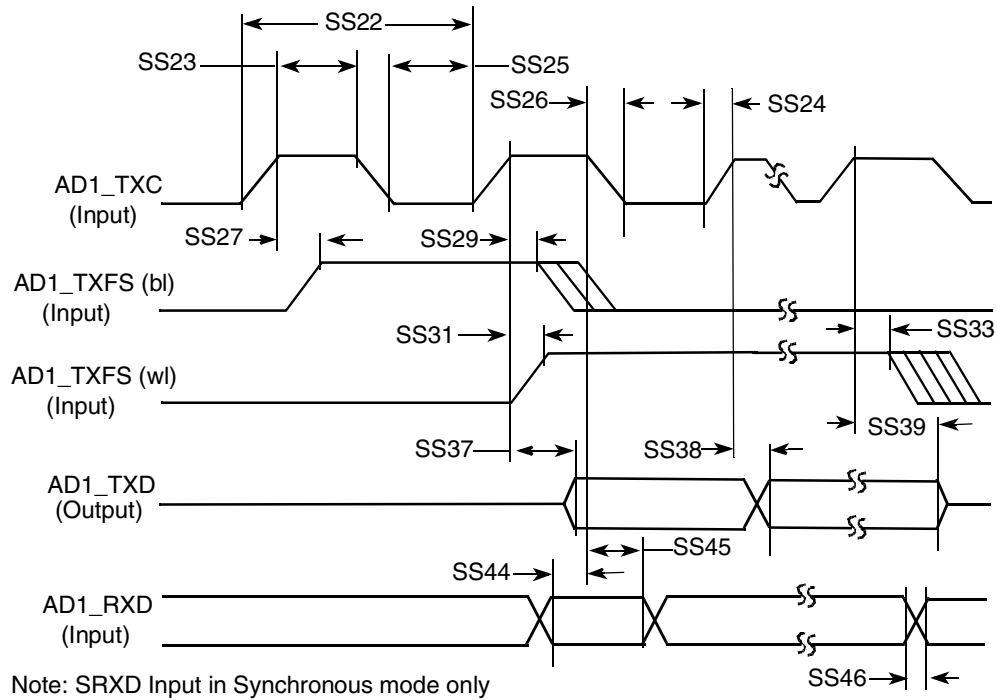


Figure 95. SSI Transmitter with External Clock Timing Diagram

Table 76. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

4.9.22.4 SSI Receiver Timing with External Clock

Figure 96 depicts the SSI receiver timing with external clock, and Table 77 lists the timing parameters.

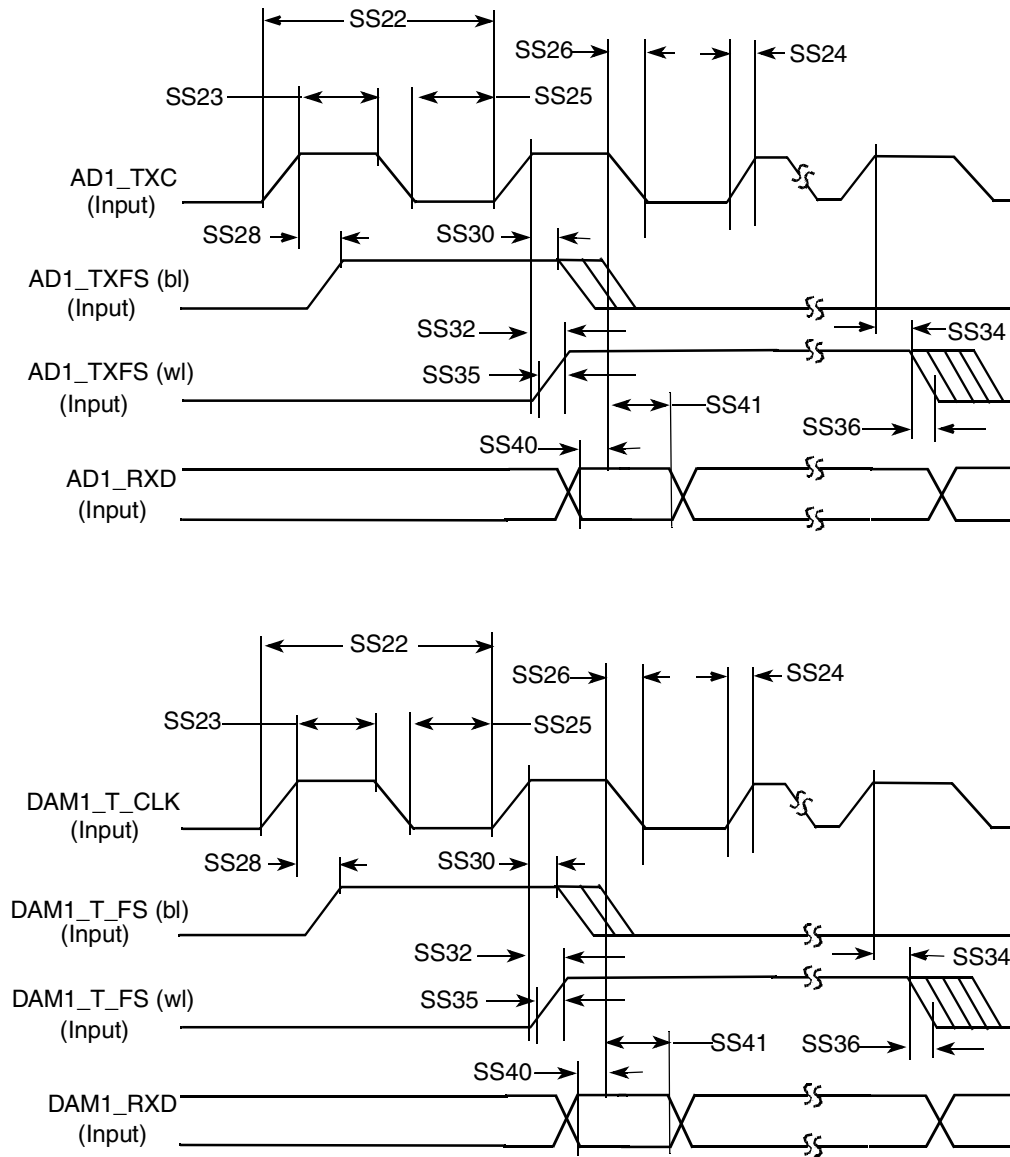


Figure 96. SSI Receiver with External Clock Timing Diagram

Table 77. SSI Receiver with External Clock Timing Parameters

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns

Table 77. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min.	Max.	Unit
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	-10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.9.23 UART Electrical

This section describes the electrical information of the UART module.

4.9.23.1 UART RS-232 Serial Mode Timing

The following subsections give the UART transmit and receive timings in RS-232 serial mode.

4.9.23.1.11 UART Transmitter

Figure 97 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 78 lists the UART RS-232 serial mode transmit timing characteristics.

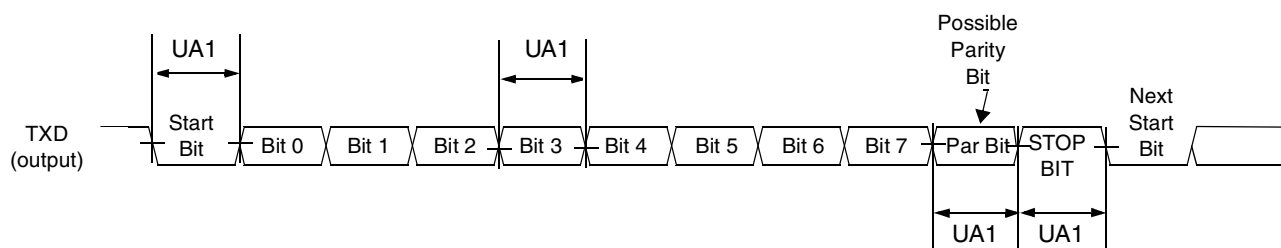


Figure 97. UART RS-232 Serial Mode Transmit Timing Diagram

Table 78. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.9.23.1.12 UART Receiver

Figure 98 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 79 lists serial mode receive timing characteristics.

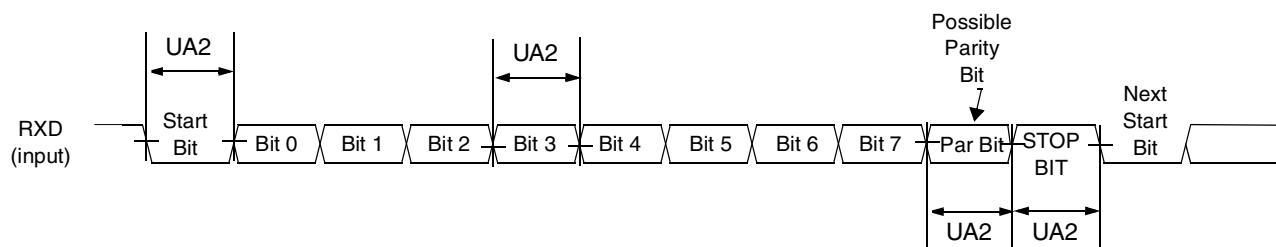


Figure 98. UART RS-232 Serial Mode Receive Timing Diagram

Table 79. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive Bit Time ¹	t_{Rbit}	$1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency}) \div 16$.

4.9.23.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.9.23.2.13 UART IrDA Mode Transmitter

Figure 99 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 80 lists the transmit timing characteristics.

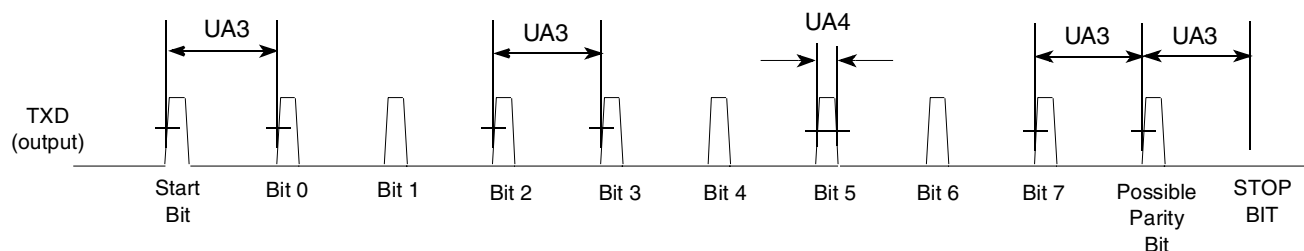


Figure 99. UART IrDA Mode Transmit Timing Diagram

Table 80. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud_rate}) - T_{ref_clk}$	$(3/16) \times (1/F_{baud_rate}) + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.9.23.2.14 UART IrDA Mode Receiver

Figure 100 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 81 lists the receive timing characteristics.

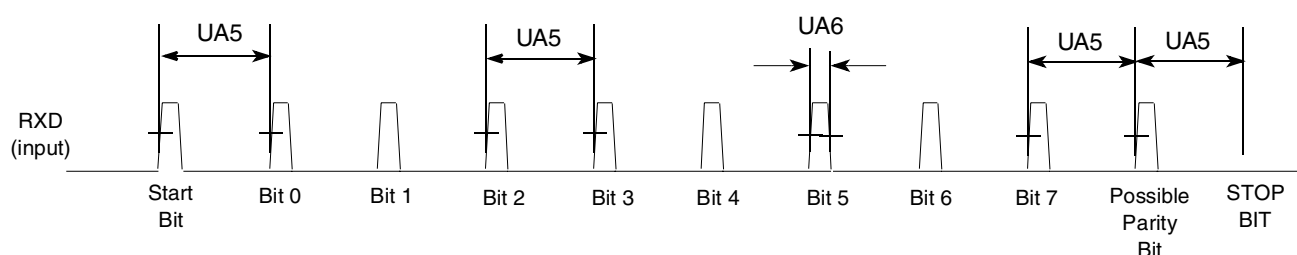


Figure 100. UART IrDA Mode Receive Timing Diagram

Table 81. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time ¹ in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 μ s	$(5/16) \times (1/F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency) \div 16.

4.9.24 USB Electrical Specifications

In order to support four different serial interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.9.24.1 DAT_SE0 Bidirectional Mode

Table 82 defines the signals for DAT_SE0 bidirectional mode. Figure 101 and Figure 102 show the transmit and receive waveforms respectively.

Table 82. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

Transmit

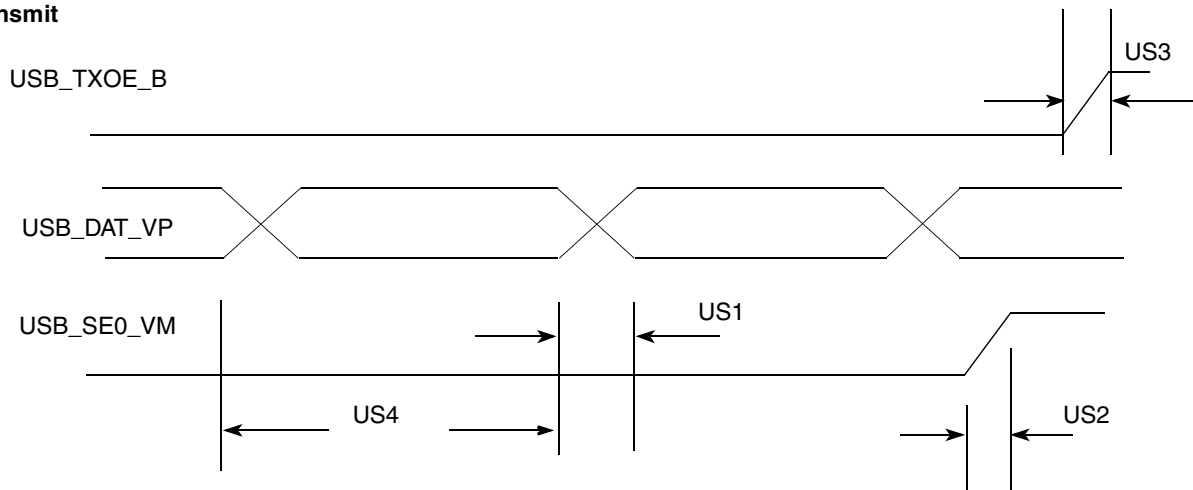


Figure 101. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

Receive

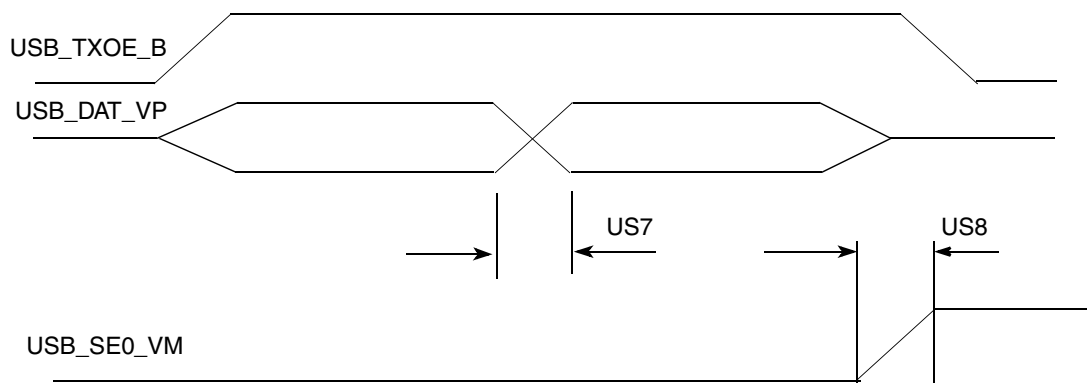


Figure 102. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 83 describes the port timing specification in DAT_SE0 bidirectional mode.

Table 83. Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.9.24.2 DAT_SE0 Unidirectional Mode

Table 84 defines the signals for DAT_SE0 unidirectional mode. Figure 103 and Figure 104 show the transmit and receive waveforms respectively.

Table 84. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

Transmit

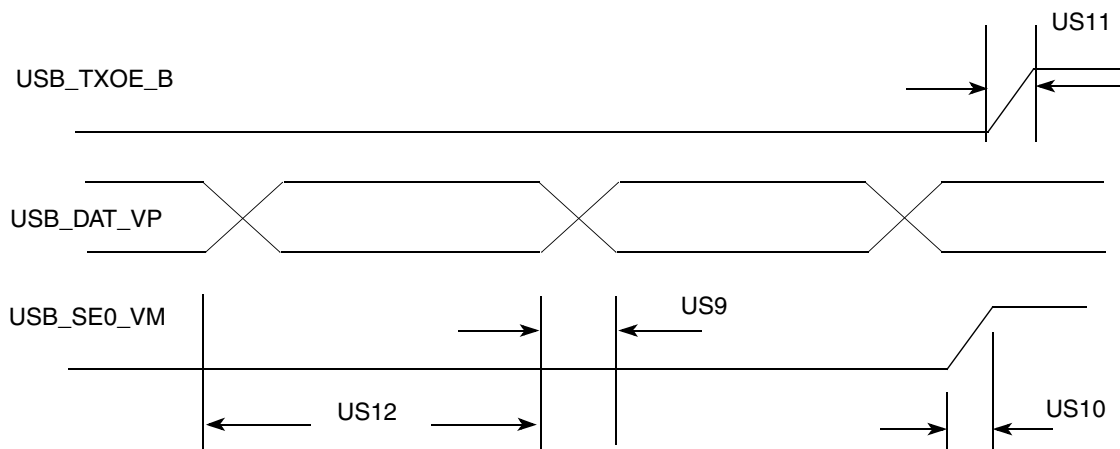


Figure 103. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

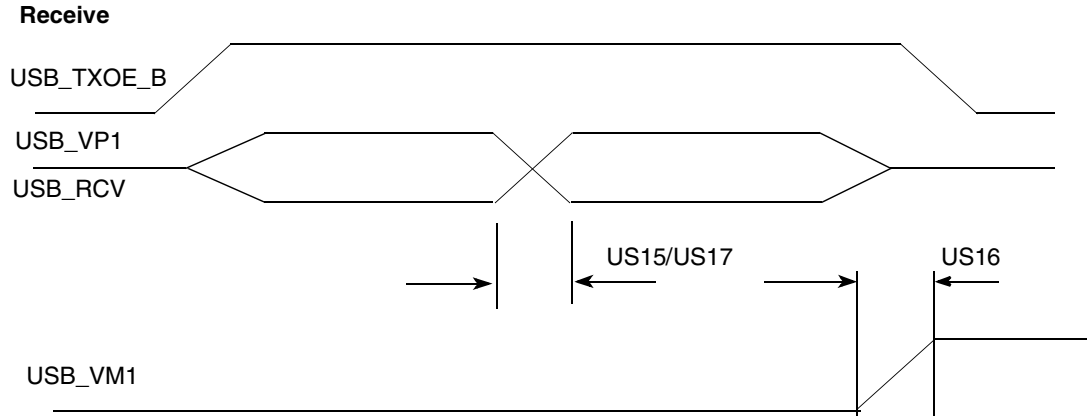


Figure 104. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 85 describes the port timing specification in DAT_SE0 unidirectional mode.

Table 85. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min.	Max.	Unit	Condition/Reference Signal
US9	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US16	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US17	Rx rise/fall time	USB_RCV	In	—	3.0	ns	35 pF

4.9.24.3 VP_VM Bidirectional Mode

Table 86 defines the signals for VP_VM bidirectional mode. Figure 105 and Figure 106 show the transmit and receive waveforms respectively.

Table 86. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	Tx VP data when USB_TXOE_B is low Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	Tx VM data when USB_TXOE_B low Rx VM data when USB_TXOE_B high
USB_RCV	In	Differential Rx data

Transmit

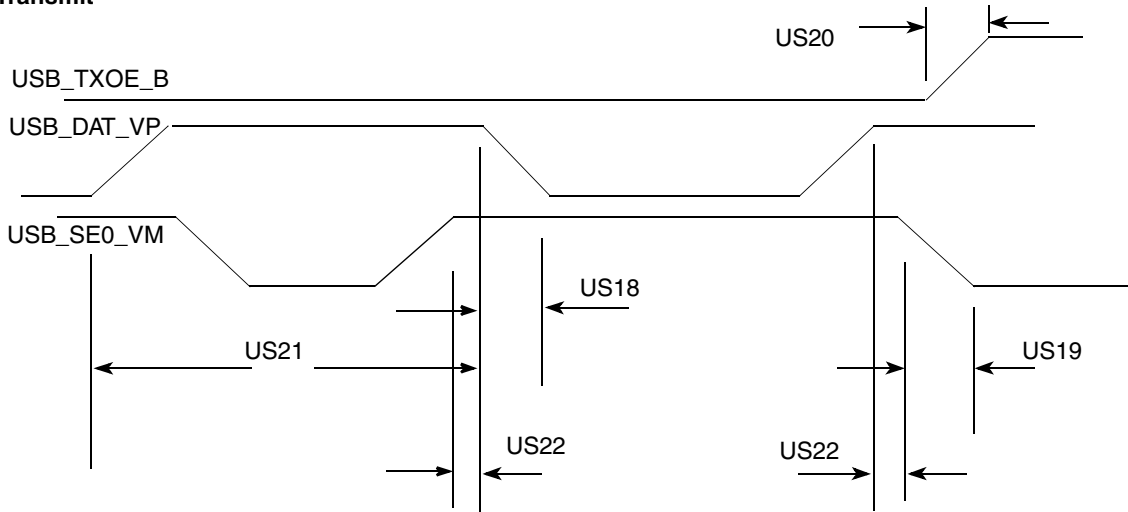


Figure 105. USB Transmit Waveform in VP_VM Bidirectional Mode

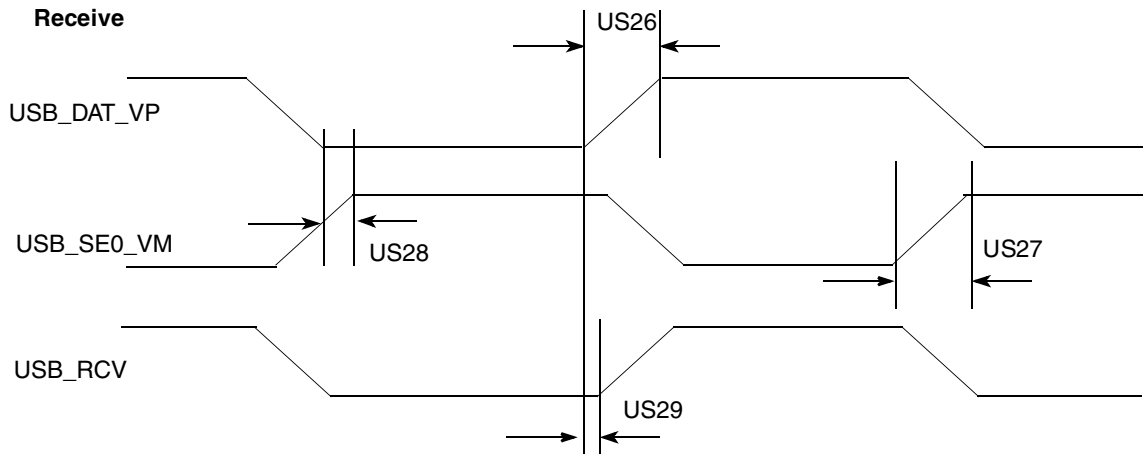


Figure 106. USB Receive Waveform in VP_VM Bidirectional Mode

Table 87 describes the port timing specification in VP_VM bidirectional mode.

Table 87. USB Port Timing Specification in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx overlap	USB_SE0_VM	Out	-3.0	+3.0	ns	USB_DAT_VP
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 87. USB Port Timing Specification in VP_VM Bidirectional Mode (continued)

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US28	Rx skew	USB_DAT_VP	In	-4.0	+4.0	ns	USB_SE0_VM
US29	Rx skew	USB_RCV	In	-6.0	+2.0	ns	USB_DAT_VP

4.9.24.4 VP_VM Unidirectional Mode

Table 88 defines the signals for VP_VM unidirectional mode. Figure 107 and Figure 108 show the transmit and receive waveforms respectively.

Table 88. Signal Definitions—VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

Transmit

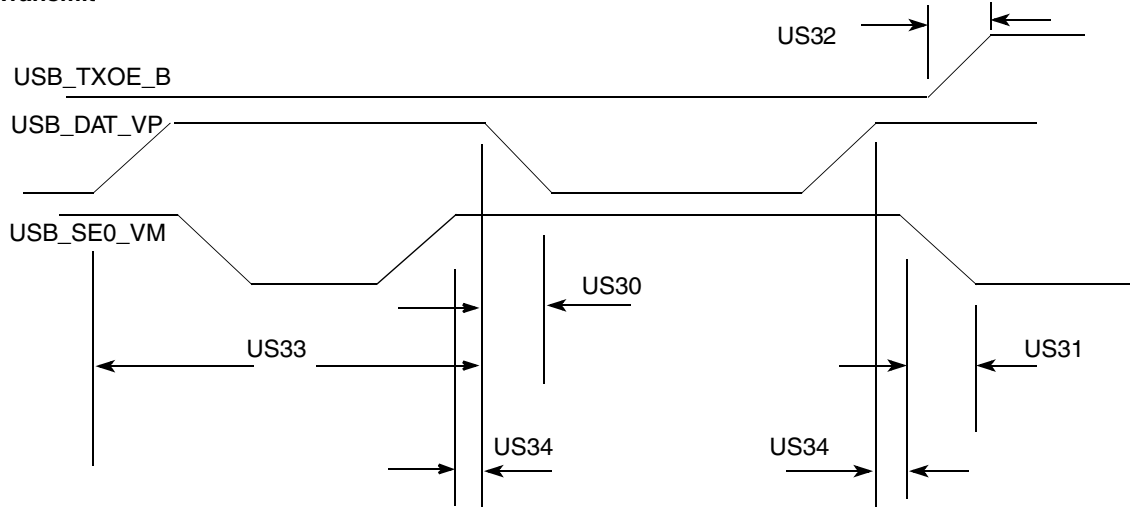


Figure 107. USB Transmit Waveform in VP_VM Unidirectional Mode

Receive

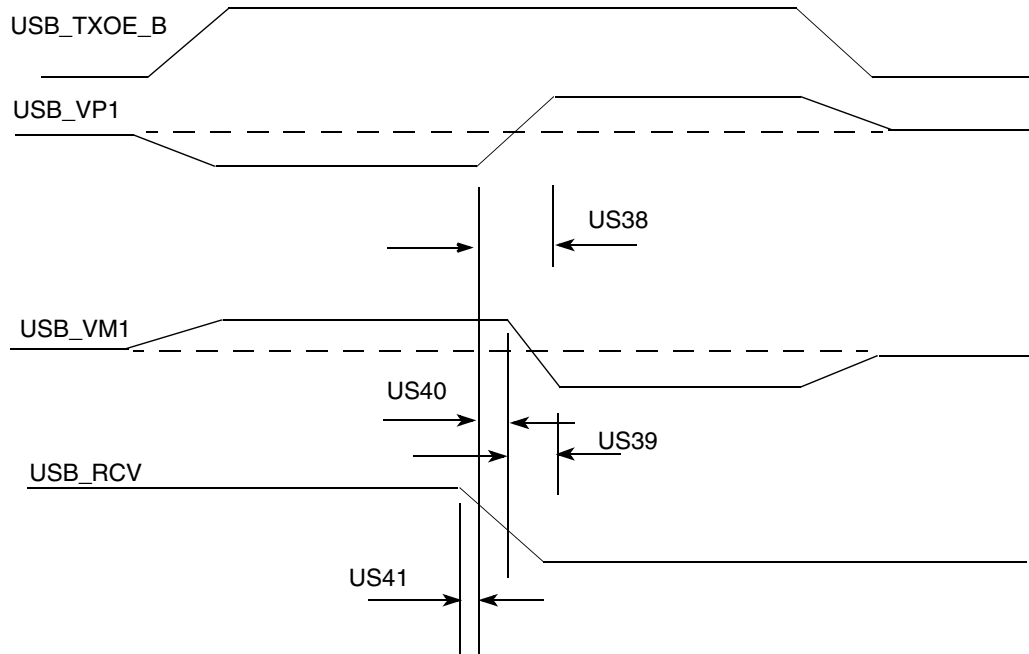


Figure 108. USB Receive Waveform in VP_VM Unidirectional Mode

Table 89 describes the port timing specification in VP_VM unidirectional mode.

Table 89. USB Timing Specification in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx overlap	USB_SE0_VM	Out	-3.0	+3.0	ns	USB_DAT_VP
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	In	-4.0	+4.0	ns	USB_VM1
US41	Rx skew	USB_RCV	In	-6.0	+2.0	ns	USB_VP1

5 Package Information and Pinout

This section includes the following:

- Mechanical package drawing
- Pin/contact assignment information

5.1 MAPBGA Production Package 1568-01, 17x17 mm, 0.8 Pitch

See Figure 109 for the package drawing and dimensions of the production package.

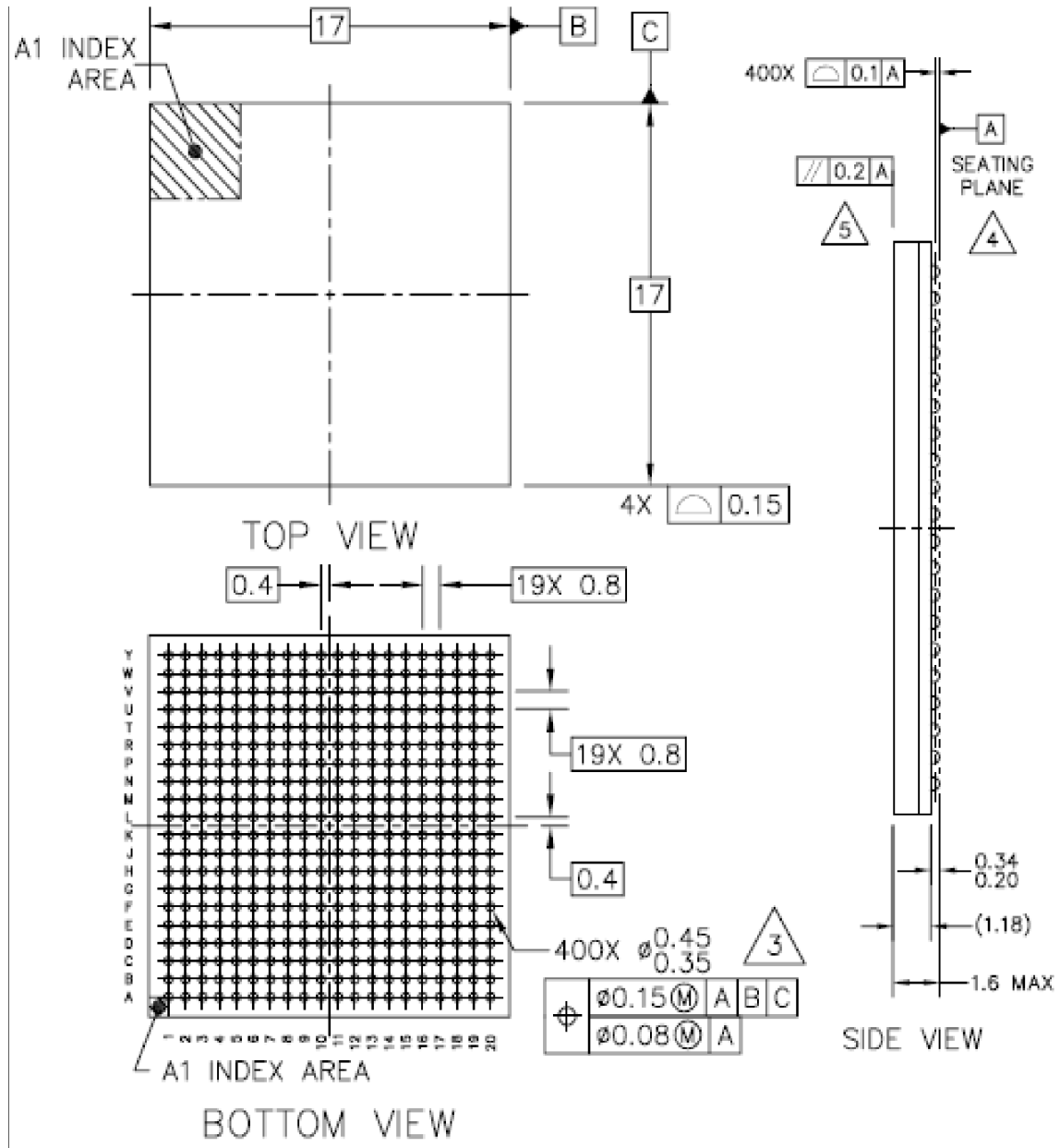


Figure 109. Production Package: Mechanical Drawing

5.2 MAPBGA Signal Assignments

Table 90 and Table 91 list MAPBGA signals, alphabetized by signal name, for silicon revisions 2.0 and 2.1, respectively. Table 92 and Table 93 show the signal assignment on the i.MX35 ball map for silicon revisions 2.0 and 2.1, respectively. The ball map for silicon revision 2.1 is different than the ballmap for silicon revision 2.0. The layout for each revision is not compatible, so it is important that the correct ballmap be used to implement the layout.

Table 90. Silicon Revision 2.0 Signal Ball Map Locations

Signal ID	Ball Location	Signal ID	Ball Location
A0	A5	ATA_DATA7	Y3
A1	D7	ATA_DATA8	U4
A10	F15	ATA_DATA9	W3
A11	D5	ATA_DIOR	Y6
A12	F6	ATA_DIOW	W6
A13	B3	ATA_DMACK	V6
A14	D14	ATA_DMARQ	T3
A15	D15	ATA_INTRQ	V2
A16	D13	ATA_IORDY	U6
A17	D12	ATA_RESET_B	T6
A18	E11	BCLK	E14
A19	D11	BOOT_MODE0	W10
A2	E7	BOOT_MODE1	U9
A20	D10	CAPTURE	V12
A21	E10	CAS	E16
A22	D9	CLK_MODE0	Y10
A23	E9	CLK_MODE1	T10
A24	D8	CLKO	V10
A25	E8	COMPARE	T12
A3	C6	CONTRAST	L16
A4	D6	CS0	F17
A5	B5	CS1	E19
A6	C5	CS2	B20
A7	A4	CS3	C19
A8	B4	CS4	E18
A9	A3	CS5	F19
ATA_BUFF_EN	T5	CSI_D10	V16
ATA_CS0	V7	CSI_D11	T15
ATA_CS1	T7	CSI_D12	W16
ATA_DA0	R4	CSI_D13	V15
ATA_DA1	V1	CSI_D14	U14
ATA_DA2	R5	CSI_D15	Y16
ATA_DATA0	Y5	CSI_D8	U15
ATA_DATA1	W5	CSI_D9	W17
ATA_DATA10	V3	CSI_HSYNC	V14
ATA_DATA11	Y2	CSI_MCLK	W15
ATA_DATA12	U3	CSI_PIXCLK	Y15

Table 90. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
ATA_DATA13	W2	CSI_VSYNC	T14
ATA_DATA14	W1	CSPI1_MISO	V9
ATA_DATA15	T4	CSPI1_MOSI	W9
ATA_DATA2	V5	CSPI1_SCLK	W8
ATA_DATA3	U5	CSPI1_SPI_RDY	T8
ATA_DATA4	Y4	CSPI1_SS0	Y8
ATA_DATA5	W4	CSPI1_SS1	U8
ATA_DATA6	V4	CTS1	R3
CTS2	G5	FEC_TDATA0	P5
D0	A2	FEC_TDATA1	M4
D1	D4	FEC_TDATA2	M5
D10	D2	FEC_TDATA3	L6
D11	E6	FEC_TX_CLK	P4
D12	E3	FEC_TX_EN	T1
D13	F5	FEC_TX_ERR	N4
D14	D1	FSR	K5
D15	E2	FST	J1
D2	B2	FUSE_VDD	P13
D3	E5	FUSE_VSS	M11
D3_CLS	L17	GPIO1_0	T11
D3_DRDY	L20	GPIO1_1	Y11
D3_FPSHIFT	L15	GPIO2_0	U11
D3_HSYNC	L18	GPIO3_0	V11
D3_REV	M17	HCKR	K2
D3_SPL	M18	HCKT	J5
D3_VSYNC	M19	I2C1_CLK	M20
D4	C3	I2C1_DAT	N17
D5	B1	I2C2_CLK	L3
D6	D3	I2C2_DAT	M1
D7	C2	LBA	D20
D8	C1	LD0	F20
D9	E4	LD1	G18
DE_B	W19	LD10	H20
DQM0	B19	LD11	J18
DQM1	D17	LD12	J16
DQM2	D16	LD13	J19
DQM3	C18	LD14	J17
EB0	F18	LD15	J20
EB1	F16	LD16	K14
ECB	D19	LD17	K19
EXT_ARMCLK	V8	LD18	K18
EXTAL_AUDIO	W20	LD19	K20
EXTAL24M	T20	LD2	G17
FEC_COL	P3	LD20	K16
FEC_CRS	N5	LD21	K17
FEC_MDC	R1	LD22	K15

Table 90. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
FEC_MDIO	P1	LD23	L19
FEC_RDATA0	P2	LD3	G16
FEC_RDATA1	N2	LD4	G19
FEC_RDATA2	M3	LD5	H16
FEC_RDATA3	N1	LD6	H18
FEC_RX_CLK	R2	LD7	G20
FEC_RX_DV	T2	LD8	H17
FEC_RX_ERR	N3	LD9	H19
MA10	C4	NVCC_EMI2	G12
MGND	N11	NVCC_EMI2	F13
MLB_CLK	W13	NVCC_EMI2	F14
MLB_DAT	Y13	NVCC_EMI3	G14
MLB_SIG	W12	NVCC_JTAG	P16
MVDD	P11	NVCC_LCDC	H14
NF_CE0	G3	NVCC_LCDC	J14
NFALE	F2	NVCC_LCDC	L14
NFCLE	E1	NVCC_LCDC	M14
NFRB	F3	NVCC_MISC	K6
NFRE_B	F1	NVCC_MISC	K7
NFWE_B	G2	NVCC_MISC	L8
NFWP_B	F4	NVCC_MLB	R10
NGND_ATA	M9	NVCC_NFC	G6
NGND_ATA	P9	NVCC_NFC	H6
NGND_ATA	L10	NVCC_NFC	H7
NGND_CRM	L11	NVCC_SDIO	P14
NGND_CSI	N10	OE	E20
NGND_EMI1	H8	OSC_AUDIO_VDD	V20
NGND_EMI1	H10	OSC_AUDIO_VSS	U19
NGND_EMI1	J10	OSC24M_VDD	T19
NGND_EMI2	J11	OSC24M_VSS	T18
NGND_EMI3	J12	PGND	M12
NGND_EMI3	K12	PHY1_VDDA	M15
NGND_JTAG	M13	PHY1_VDDA	N20
NGND_LCDC	K11	PHY1_VSSA	N16
NGND_LCDC	L12	PHY1_VSSA	P20
NGND_MISC	M7	PHY2_VDD	R13
NGND_MISC	K8	PHY2_VSS	P12
NGND_MLB	M10	POR_B	W11
NGND_NFC	K9	POWER_FAIL	Y9
NGND_SDIO	N12	PVDD	N13
NVCC_ATA	N6	RAS	E15
NVCC_ATA	P6	RESET_IN_B	U10
NVCC_ATA	P7	RTCK	U18
NVCC_ATA	P8	RTS1	U1
NVCC_CRM	R9	RTS2	G1
NVCC_CSI	R11	RW	C20

Table 90. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
NVCC_EMI1	G7	RXD1	U2
NVCC_EMI1	G8	RXD2	H3
NVCC_EMI1	G9	SCK4	L4
NVCC_EMI1	H9	SCK5	L5
NVCC_EMI1	F10	SCKR	K3
NVCC_EMI1	G10	SCKT	J4
NVCC_EMI1	F11	SD0	C17
NVCC_EMI1	G11	SD1	A19
SD1_CLK	V18	SDCLK	E12
SD1_CMD	Y19	SDCLK_B	E13
SD1_DATA0	R14	SDQS0	B17
SD1_DATA1	U16	SDQS1	A13
SD1_DATA2	W18	SDQS2	A10
SD1_DATA3	V17	SDQS3	C7
SD10	A15	SDWE	G15
SD11	B15	SJC_MOD	U17
SD12	C13	SRXD4	L1
SD13	B14	SRXD5	K4
SD14	A14	STXD4	M2
SD15	B13	STXD5	K1
SD16	C12	STXFS4	L2
SD17	C11	STXFS5	J6
SD18	A12	TCK	R17
SD19	B12	TDI	P15
SD2	B18	TDO	R15
SD2_CLK	W14	TEST_MODE	Y7
SD2_CMD	U13	TMS	R16
SD2_DATA0	V13	TRSTB	T16
SD2_DATA1	T13	TTM_PIN	M16
SD2_DATA2	Y14	TX0	G4
SD2_DATA3	U12	TX1	H1
SD20	B11	TX2_RX3	H5
SD21	A11	TX3_RX2	J2
SD22	C10	TX4_RX1	H4
SD23	B10	TX5_RX0	J3
SD24	A9	TXD1	R6
SD25	C9	TXD2	H2
SD26	B9	USBOTG_OC	U7
SD27	A8	USBOTG_PWR	W7
SD28	B8	USBPHY1_DM	N19
SD29	C8	USBPHY1_DP	P19
SD3	C16	USBPHY1_RREF	R19
SD30	A7	USBPHY1_UID	N18
SD31	B7	USBPHY1_UPLLGN	N14
SD4	A18	USBPHY1_UPLLVD	N15
SD5	C15	USBPHY1_UPLLVD	P17

Table 90. Silicon Revision 2.0 Signal Ball Map Locations (continued)

Signal ID	Ball Location
SD6	A17
SD7	B16
SD8	C14
SD9	A16
SDBA0	A6
SDBA1	B6
SDCKE0	D18
SDCKE1	E17
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
USBPHY1_VBUS	P18
USBPHY1_VDDA_BIAS	R20
USBPHY1_VSSA_BIAS	R18
USBPHY2_DM	Y17
USBPHY2_DP	Y18
VDD	M6
VDD	F7
VDD	J7
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
VSS	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, MCIMX357DVM5B, and MCIMX357DVM5B.

Table 91. Silicon Revision 2.1 Signal Ball Map Locations

Signal ID	Ball Location	Signal ID	Ball Location
A0	A5	ATA_DATA7	Y3
A1	D7	ATA_DATA8	U4
A10	F15	ATA_DATA9	W3
A11	D5	ATA_DIOR	Y6
A12	F6	ATA_DIOW	W6
A13	B3	ATA_DMACK	V6
A14	D14	ATA_DMARQ	T3
A15	D15	ATA_INTRQ	V2
A16	D13	ATA_IORDY	U6
A18	D12	ATA_RESET_B	T6
SDQS1	E11	SDQS0	E14
A19	D11	BOOT_MODE0	W10
A2	E7	BOOT_MODE1	U9
A21	D10	CAPTURE	V12
SDQS2	E10	RAS	E16
A22	D9	CLK_MODE0	Y10
SDQS3	E9	CLK_MODE1	T10
A24	D8	CLKO	V10
A25	E8	COMPARE	T12
A3	C6	CONTRAST	L16
A4	D6	CS0	F17
A5	B5	CS1	E19
A6	C5	CS2	B20
A7	A4	CS3	C19
A8	B4	CS4	E18
A9	A3	CS5	F19
ATA_BUFF_EN	T5	CSI_D10	V16
ATA_CS0	V7	CSI_D11	T15
ATA_CS1	T7	CSI_D12	W16
ATA_DA0	R4	CSI_D13	V15
ATA_DA1	V1	CSI_D14	U14
ATA_DA2	R5	CSI_D15	Y16
ATA_DATA0	Y5	CSI_D8	U15
ATA_DATA1	W5	CSI_D9	W17
ATA_DATA10	V3	CSI_HSYNC	V14
ATA_DATA11	Y2	CSI_MCLK	W15
ATA_DATA12	U3	CSI_PIXCLK	Y15
ATA_DATA13	W2	CSI_VSYNC	T14
ATA_DATA14	W1	CSPI1_MISO	V9
ATA_DATA15	T4	CSPI1_MOSI	W9
ATA_DATA2	V5	CSPI1_SCLK	W8
ATA_DATA3	U5	CSPI1_SPI_RDY	T8
ATA_DATA4	Y4	CSPI1_SS0	Y8
ATA_DATA5	W4	CSPI1_SS1	U8
ATA_DATA6	V4	CTS1	R3

Table 91. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
CTS2	G5	FEC_TDATA0	P5
D0	A2	FEC_TDATA1	M4
D1	D4	FEC_TDATA2	M5
D10	D2	FEC_TDATA3	L6
D11	E6	FEC_TX_CLK	P4
D12	E3	FEC_TX_EN	T1
D13	F5	FEC_TX_ERR	N4
D14	D1	FSR	K5
D15	E2	FST	J1
D2	B2	FUSE_VDD	P13
D3	E5	FUSE_VSS	M11
D3_CLS	L17	GPIO1_0	T11
D3_DRDY	L20	GPIO1_1	Y11
D3_FPSHIFT	L15	GPIO2_0	U11
D3_HSYNC	L18	GPIO3_0	V11
D3_REV	M17	HCKR	K2
D3_SPL	M18	HCKT	J5
D3_VSYNC	M19	I2C1_CLK	M20
D4	C3	I2C1_DAT	N17
D5	B1	I2C2_CLK	L3
D6	D3	I2C2_DAT	M1
D7	C2	LBA	D20
D8	C1	LD0	F20
D9	E4	LD1	G18
DE_B	W19	LD10	H20
DQM0	B19	LD11	J18
SDCKE1	D17	LD12	J16
DQM2	D16	LD13	J19
DQM3	C18	LD14	J17
EB0	F18	LD15	J20
EB1	F16	LD16	K14
ECB	D19	LD17	K19
EXT_ARMCLK	V8	LD18	K18
EXTAL_AUDIO	W20	LD19	K20
EXTAL24M	T20	LD2	G17
FEC_COL	P3	LD20	K16
FEC_CRIS	N5	LD21	K17
FEC_MDC	R1	LD22	K15
FEC_MDIO	P1	LD23	L19
FEC_RDATA0	P2	LD3	G16
FEC_RDATA1	N2	LD4	G19
FEC_RDATA2	M3	LD5	H16
FEC_RDATA3	N1	LD6	H18
FEC_RX_CLK	R2	LD7	G20
FEC_RX_DV	T2	LD8	H17
FEC_RX_ERR	N3	LD9	H19

Table 91. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
MA10	C4	NVCC_EMI2	G12
MGND	N11	NVCC_EMI2	F13
MLB_CLK	W13	VSS	F14
MLB_DAT	Y13	NVCC_EMI3	G14
MLB_SIG	W12	NVCC_JTAG	P16
MVDD	P11	NVCC_LCDC	H14
NF_CEO	G3	NVCC_LCDC	J14
NFALE	F2	NVCC_LCDC	L14
NFCLE	E1	NVCC_LCDC	M14
NFRB	F3	NVCC_MISC	K6
NFRE_B	F1	NVCC_MISC	K7
NFWE_B	G2	NVCC_MISC	L8
NFWP_B	F4	NVCC_MLB	R10
NGND_ATA	M9	NVCC_NFC	G6
NGND_ATA	P9	NVCC_NFC	H6
NGND_ATA	L10	NVCC_NFC	H7
NGND_CRM	L11	NVCC_SDIO	P14
NGND_CSI	N10	OE	E20
NGND_EMI1	H8	OSC_AUDIO_VDD	V20
NVCC_EMI1	H10	OSC_AUDIO_VSS	U19
NGND_EMI1	J10	OSC24M_VDD	T19
NGND_EMI2	J11	OSC24M_VSS	T18
NGND_EMI3	J12	PGND	M12
NGND_EMI3	K12	PHY1_VDDA	M15
NGND_JTAG	M13	PHY1_VDDA	N20
NGND_LCDC	K11	PHY1_VSSA	N16
NGND_LCDC	L12	PHY1_VSSA	P20
NGND_MISC	M7	PHY2_VDD	R13
NGND_MISC	K8	PHY2_VSS	P12
NGND_MLB	M10	POR_B	W11
NGND_NFC	K9	POWER_FAIL	Y9
NGND_SDIO	N12	PVDD	N13
NVCC_ATA	N6	BCLK	E15
NVCC_ATA	P6	RESET_IN_B	U10
NVCC_ATA	P7	RTCK	U18
NVCC_ATA	P8	RTS1	U1
NVCC_CRM	R9	RTS2	G1
NVCC_CSI	R11	RW	C20
NVCC_EMI1	G7	RXD1	U2
NVCC_EMI1	G8	RXD2	H3
NVCC_EMI1	G9	SCK4	L4
NVCC_EMI1	H9	SCK5	L5
NGND_EMI1	F10	SCKR	K3
NVCC_EMI1	G10	SCKT	J4
NVCC_EMI1	F11	DQM1	C17
NVCC_EMI1	G11	SD1	A19

Table 91. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location	Signal ID	Ball Location
SD1_CLK	V18	SDCLK	E12
SD1_CMD	Y19	SDCLK_B	E13
SD1_DATA0	R14	SD0	B17
SD1_DATA1	U16	SD15	A13
SD1_DATA2	W18	SD23	A10
SD1_DATA3	V17	A23	C7
SD10	A15	SDWE	G15
SD11	B15	SJC_MOD	U17
A17	C13	SRXD4	L1
SD13	B14	SRXD5	K4
SD14	A14	STXD4	M2
SD12	B13	STXD5	K1
SD16	C12	STXFS4	L2
SD17	C11	STXFS5	J6
SD18	A12	TCK	R17
SD19	B12	TDI	P15
SD2	B18	TDO	R15
SD2_CLK	W14	TEST_MODE	Y7
SD2_CMD	U13	TMS	R16
SD2_DATA0	V13	TRSTB	T16
SD2_DATA1	T13	TTM_PIN	M16
SD2_DATA2	Y14	TX0	G4
SD2_DATA3	U12	TX1	H1
SD20	B11	TX2_RX3	H5
SD21	A11	TX3_RX2	J2
A20	C10	TX4_RX1	H4
SD22	B10	TX5_RX0	J3
SD24	A9	TXD1	R6
SD25	C9	TXD2	H2
SD26	B9	USBOTG_OC	U7
SD27	A8	USBOTG_PWR	W7
SD28	B8	USBPHY1_DM	N19
SD29	C8	USBPHY1_DP	P19
SD3	C16	USBPHY1_RREF	R19
SD30	A7	USBPHY1_UID	N18
SD31	B7	USBPHY1_UPLLGND	N14
SD4	A18	USBPHY1_UPLLVD	N15
SD5	C15	USBPHY1_UPLLVD	P17
SD6	A17	USBPHY1_VBUS	P18
SD7	B16	USBPHY1_VDDA_BIAS	R20
SD8	C14	USBPHY1_VSSA_BIAS	R18
SD9	A16	USBPHY2_DM	Y17
SDBA0	A6	USBPHY2_DP	Y18
SDBA1	B6	VDD	M6
SDCKE0	D18	VDD	F7
CAS	E17	VDD	J7

Table 91. Silicon Revision 2.1 Signal Ball Map Locations (continued)

Signal ID	Ball Location
VDD	L7
VDD	N7
VDD	R7
VDD	F8
VDD	R8
VDD	F9
VDD	F12
VDD	R12
VDD	G13
VDD	H15
VDD	J15
VSS	A1
VSS	Y1
VSS	J8
VSS	M8
VSS	N8
VSS	J9

Signal ID	Ball Location
VSS	L9
VSS	N9
VSS	K10
VSS	P10
VSS	H11
VSS	H12
NVCC_EMI2	H13
VSS	J13
VSS	K13
VSS	L13
VSS	T17
VSS	A20
VSS	Y20
VSTBY	T9
WDOG_RST	Y12
XTAL_AUDIO	V19
XTAL24M	U20

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Table 92. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	D0	A9	A7	A0	SDB A0	SD3 0	SD2 7	SD2 4	SDQ S2	SD2 1	SD1 8	SDQ S1	SD1 4	SD1 0	SD9	SD6	SD4	SD1	VSS	A
B	D5	D2	A13	A8	A5	SDB A1	SD3 1	SD2 8	SD2 6	SD2 3	SD2 0	SD1 9	SD1 5	SD1 3	SD1 1	SD7	SDQ S0	SD2	DQM 0	CS2	B
C	D8	D7	D4	MA1 0	A6	A3	SDQ S3	SD2 9	SD2 5	SD2 2	SD1 7	SD1 6	SD1 2	SD8	SD5	SD3	SD0	DQM 3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM 2	DQM 1	SDC KE0	ECB	LBA	D
E	NFC LE	D15	D12	D9	D3	D11	A2	A25	A23	A21	A18	SDC LK	SDC LK_ B	BCL K	RAS	CAS	SDC KE1	CS4	CS1	OE	E
F	NFR E_B	NFA LE	NFR B	NFW P_B	D13	A12	VDD	VDD	VDD	NVC C_E MI1	NVC C_E MI1	VDD	NVC C_E MI2	NVC C_E MI2	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS 2	NFW E_B	NF_ CE0	TX0	CTS 2	NVC C_N FC	NVC C_E MI1	NVC C_E MI1	NVC C_E MI1	NVC C_E MI1	NVC C_E MI1	NVC C_E MI2	VDD	NVC C_E MI3	SDW E	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD 2	RXD 2	TX4_ RX1	TX2_ RX3	NVC C_N FC	NVC C_N FC	NGN D_E MI1	NVC C_E MI1	NGN D_E MI1	VSS	VSS	VSS	NVC C_L CDC	VDD	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_ RX2	TX5_ RX0	SCK T	HCK T	STX FS5	VDD	VSS	VSS	NGN D_E MI1	NGN D_E MI2	NGN D_E MI3	VSS	NVC C_L CDC	VDD	LD12	LD14	LD11	LD13	LD15	J
K	STX D5	HCK R	SCK R	SRX D5	FSR	NVC C_M SC	NVC C_M SC	NGN D_M FC	NGN D_N FC	VSS	NGN D_L CDC	NGN D_E MI3	VSS	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRX D4	STX FS4	I2C2_ CL K	SCK 4	SCK 5	FEC _TD ATA3	VDD	NVC C_M SC	VSS	NGN D_A TA	NGN D_C RM	NGN D_L CDC	VSS	NVC C_L CDC	D3_ FPS HIFT	CON TRA ST	D3_ CLS	D3_ HSY NC	LD23	D3_ DRD Y	L
M	I2C2_ _DAT	STX D4	FEC _RD ATA2	FEC _TD ATA1	FEC _TD ATA2	VDD	NGN D_M SC	VSS	NGN D_A TA	NGN D_M LB	FUS E_V SS	PGN D	NGN D_JT AG	NVC C_L CDC	PHY 1_V DDA	TTM _PIN	D3_ REV	D3_ SPL	D3_ VSY NC	I2C1 _CL K	M
N	FEC _RD ATA3	FEC _RD ATA1	FEC _RX _ER R	FEC _TX _ERR	FEC _CR S	NVC C_A TA	VDD	VSS	VSS	NGN D_C SI	MGN D	NGN D_S DIO	PVD D	USB PHY 1_U PLL GND	USB PHY 1_U PLL VDD	PHY 1_V SSA	I2C1 _DAT	USB PHY 1_UI D	USB PHY 1_D M	PHY 1_V DDA	N
P	FEC _MDI O	FEC _RD ATA0	FEC _CO L	FEC _TX _CLK	FEC _TD ATA0	NVC C_A TA	NVC C_A TA	NVC C_A TA	NGN D_A TA	VSS	MVD D	PHY 2_V SS	FUS E_V DD	NVC C_S DIO	TDI	NVC C_JT AG	USB PHY 1_U PLL VDD	USB PHY 1_V BUS	USB PHY 1_D P	PHY 1_V SSA	P
R	FEC _MD C	FEC _RX _CL K	CTS 1	ATA_ DA0	ATA_ DA2	TXD 1	VDD	VDD	NVC C_C RM	NVC C_M LB	NVC C_C SI	VDD	PHY 2_V DD	SD1 _DAT A0	TDO	TMS	TCK	USB PHY 1_V SSA _BIA S	USB PHY 1_R REF	USB PHY 1_V DDA _BIA S	R
T	FEC _TX _EN	FEC _RX _DV	ATA_ DMA RQ	ATA_ DATA 15	ATA_ BUF _F_E N	ATA_ RES _ET_ B	ATA_ CS1	CSPI 1_S PI_ R DY	VST BY	CLK _MO DE1	GPI O1_ 0	COM PAR E	SD2 _DAT A1	CSL _VSY NC	CSL _D11	TRS TB	VSS	OSC 24M _VS S	OSC 24M _VD D	EXT AL24 M	T
U	RTS 1	RXD 1	ATA_ DATA 12	ATA_ DATA 8	ATA_ DATA 3	ATA_ IOR DY	USB OTG _OC	CSPI 1_S S1	BOO T_M ODE 1	RES ET_ I_N_ B	GPI O2_ 0	SD2 _DAT A3	SD2 _CM D	CSL _D14	CSL _D8	SD1 _DAT A1	SJC _MO D	RTC K	OSC _AU DIO_ VSS	XTAL 24M	U

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353DVM5B, MCIMX353DVM5B, and MCIMX357DVM5B.

Table 92. Silicon Revision 2.0 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
V	ATA_DA1	ATA_INTRQ	ATA_DATA10	ATA_DATA6	ATA_DATA2	ATA_DMA CK	ATA_CS0	EXT_AR MCLK	CSPI1_MISO	CLK_O	GPI_O3_0	CAP_TUR E	SD2_DAT A0	CSL_HSY NC	CSL_D13	CSL_D10	SD1_DAT A3	SD1_CL K	XTAL_AU DIO	OSC_AU DIO_VDD	V
W	ATA_DATA14	ATA_DATA13	ATA_DATA9	ATA_DATA5	ATA_DATA1	ATA_DIO W	USB_OTG_PWR	CSPI1_S CLK	CSPI1_M OSI	BOOT_M ODE0	POR_B	MLB_SIG	MLB_CL K	SD2_CL K	CSL_MCL K	CSL_D12	CSL_D9	SD1_DAT A2	DE_B	EXT_AL_AU DIO	W
Y	VSS	ATA_DATA11	ATA_DATA7	ATA_DATA4	ATA_DATA0	ATA_DIO R	TEST_M ODE	CSPI1_S O	POWER_FAIL	CLK_M ODE0	GPI_O1_1	WD_OG_RST	MLB_DAT	SD2_DAT A2	CSL_PIXC LK	CSL_D15	USB_PHY 2_D M	USB_PHY 2_D P	SD1_CM D	VSS	Y

Table 93. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	D0	A9	A7	A0	SDB_A0	SD30	SD27	SD24	SD23	SD21	SD18	SD15	SD14	SD10	SD9	SD6	SD4	SD1	GND	A
B	D5	D2	A13	A8	A5	SDB_A1	SD31	SD28	SD26	SD22	SD20	SD19	SD12	SD13	SD11	SD7	SD0	SD2	DQM_0	CS2	B
C	D8	D7	D4	MA1_0	A6	A3	A23	SD29	SD25	A20	SD17	SD16	A17	SD8	SD5	SD3	DQM_1	DQM_3	CS3	RW	C
D	D14	D10	D6	D1	A11	A4	A1	A24	A22	A21	A19	A18	A16	A14	A15	DQM_2	SDC_KE1	SDC_KE0	ECB	LBA	D
E	NFC_LE	D15	D12	D9	D3	D11	A2	A25	SDQ_S3	SDQ_S2	SDQ_S1	SDC_LK	SDC_LK_B	SDQ_S0	BCL_K	RAS	CAS	CS4	CS1	OE	E
F	NFR_E_B	NFAL_E	NFR_B	NFW_P_B	D13	A12	VDD_7	VDD_7	VDD_7	GND	NVC_C_E MI1	VDD_7	NVC_C_E MI2	GND	A10	EB1	CS0	EB0	CS5	LD0	F
G	RTS_2	NFW_E_B	NF_CE0	TX0	CTS_2	NVC_C_N FC	NVC_C_E MI1	NVC_C_E MI1	NVC_C_E MI1	NVC_C_E MI1	NVC_C_E MI1	NVC_C_E MI2	VDD_6	NVC_C_E MI3	SDW_E	LD3	LD2	LD1	LD4	LD7	G
H	TX1	TXD_2	RXD_2	TX4_RX1	TX2_RX3	NVC_C_N FC	NVC_C_N FC	GND	NVC_C_E MI1	NVC_C_E MI1	GND	GND	NVC_C_E MI2	NVC_C_L CDC	VDD_5	LD5	LD8	LD6	LD9	LD10	H
J	FST	TX3_RX2	TX5_RX0	SCK_T	HCK_T	STX_FS5	VDD_1	GND	GND	GND	GND	GND	GND	NVC_C_L CDC	VDD_5	LD12	LD14	LD11	LD13	LD15	J
K	STX_D5	HCK_R	SCK_R	SRX_D5	FSR	NVC_C_MI SC	NVC_C_MI SC	GND	GND	GND	GND	GND	GND	LD16	LD22	LD20	LD21	LD18	LD17	LD19	K
L	SRX_D4	STX_FS4	I2C2_CLK	SCK_4	SCK_5	FEC_TDA TA3	VDD_2	NVC_C_MI SC	GND	GND	GND	GND	GND	NVC_C_L CDC	D3_F_PSHI FT	CON_TRA ST	D3_CLS	D3_HSY NC	LD23	D3_DRD Y	L
M	I2C2_DAT	STX_D4	FEC_RD_ATA2	FEC_TDA TA1	FEC_TDA TA2	VDD_2	GND	GND	GND	GND	FUS_E_V SS	PGN_D	GND	NVC_C_L CDC	PHY_1_VD DA	TTM_PAD	D3_REV	D3_S PL	D3_V SYN C	I2C1_CLK	M
N	FEC_RD_ATA3	FEC_RD_ATA1	FEC_RX_ERR	FEC_TX_ERR	FEC_CR S	NVC_C_AT A	VDD_3	GND	GND	GND	MGN_D	GND	PVD_D	USB_PHY 1_UP LLVD	USB_PHY 1_UP LLVD	PHY_1_VS SA	I2C1_DAT	USB_PHY 1_UI D	USB_PHY 1_D M	PHY_1_VD DA	N
P	FEC_MDI_O	FEC_RD_ATA0	FEC_CO_L	FEC_TX_CLK	FEC_TDA TA0	NVC_C_AT A	NVC_C_AT A	NVC_C_AT A	GND	GND	MVD_D	PHY_2_VS S	FUS_E_V DD	NVC_C_S DIO	TDI	NVC_C_JT AG	USB_PHY 1_UP LLVD	USB_PHY 1_VB US	USB_PHY 1_DP	PHY_1_VS SA	P

Table 93. Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
R	FEC_MD_C	FEC_RX_CLK	CTS_1	ATA_DA0	ATA_DA2	TXD_1	VDD_3	VDD_3	NVC_C_CRM	NVC_C_MLB	NVC_C_CSI	VDD_4	PHY_2_VDD	SD1_DATA_0	TDO	TMS	TCK	USB_PHY_1_VS_SA_BIAS	USB_PHY_1_R_REF	USB_PHY_1_VD_DA_BIAS	R
T	FEC_TX_EN	FEC_RX_DV	ATA_DMA_RQ	ATA_DATA_15	ATA_BUF_F_E_N	ATA_RES_ET_B	ATA_CS1	CSPI_1_SP_I_RD_Y	VST_BY	CLK_MOD_E1	GPIO_1_0	COM_PARE	SD2_DATA_1	CSI_VSY_NC	CSI_D11	TRSTB	GND	OSC_24M_VSS	OSC_24M_VDD	EXTAL_24M	T
U	RTS_1	RXD_1	ATA_DATA_12	ATA_DATA_8	ATA_DATA_3	ATA_IORD_Y	USB_OTG_OC	CSPI_1_SS_1	BOOT_MODE_1	RESET_IN_B	GPIO_2_0	SD2_DATA_3	SD2_CMD	CSI_D14	CSI_D8	SD1_DATA_1	SJC_MOD	RTCK	OSC_AU_DIO_VSS	XTAL_24M	U
V	ATA_DA1	ATA_INTR_Q	ATA_DATA_10	ATA_DATA_6	ATA_DATA_2	ATA_DMA_CK	ATA_CS0	EXT_ARM_CLK	CSPI_1_MISO	CLK_0	GPIO_3_0	CAP_TUR_E	SD2_DATA_0	CSI_HSY_NC	CSI_D13	CSI_D10	SD1_DATA_3	SD1_CLK	XTAL_AU_DIO	OSC_AU_DIO_VDD	V
W	ATA_DATA_14	ATA_DATA_13	ATA_DATA_9	ATA_DATA_5	ATA_DATA_1	ATA_DIO_W	USB_OTG_PW_R	CSPI_1_SCLK	CSPI_1_MOSI	BOOT_MODE_0	POR_B	MLB_SIG	MLB_CLK	SD2_CLK	CSI_MCLK	CSI_D12	CSI_D9	SD1_DATA_2	DE_B	EXTAL_AU_DIO	W
Y	GND	ATA_DATA_11	ATA_DATA_7	ATA_DATA_4	ATA_DATA_0	ATA_DIOR	TEST_MODE	CSPI_1_SS_0	POWER_FAIL	CLK_MODE_0	GPIO_1_1	WDOG_RST	MLB_DAT	SD2_DATA_2	CSI_PIXCLK	CSI_D15	USB_PHY_2_DM	USB_PHY_2_DP	SD1_CMD	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

6 Product Documentation

All related product documentation for the i.MX35 processor is located at <http://www.freescale.com/imx>.

7 Revision History

Table 94 shows the revision history of this document.

Table 94. i.MX35 Data Sheet Revision History

Revision Number	Date	Substantive Change(s)
8	04/2010	<ul style="list-style-type: none"> Updated Table 13, "I/O Pin DC Electrical Characteristics."
7	12/18/2009	<ul style="list-style-type: none"> Updated Table 1, "Ordering Information."
6	10/21/2009	<ul style="list-style-type: none"> Added information for silicon rev. 2.1 Updated Table 1, "Ordering Information." Added Table 91, "Silicon Revision 2.1 Signal Ball Map Locations." Added Table 93, "Silicon Revision 2.1 Ball Map—17 x 17, 0.8 mm Pitch."
5	08/06/2009	<ul style="list-style-type: none"> Added a line for $T_A = -40$ to 85 °C in Table 13, "I/O Pin DC Electrical Characteristics" Filled in TBDs in Table 13. Revised Figure 15 and Table 30 by removing FCE = 0 and FCE = 1. Added footnote 3 to the table. Added Table 24, "AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode Max Drive (1.8 V)."

Table 94. i.MX35 Data Sheet Revision History (continued)

Revision Number	Date	Substantive Change(s)
4	04/30/2009	<ul style="list-style-type: none"> Added Section 4.4, "Reset Timing." In Section 4.8.2, "AC Electrical Characteristics for DDR Pins (DDR2, Mobile DDR, and SDRAM Modes)," removed Slow Slew rate tables, relabeled Table 22, "AC Electrical Characteristics of DDR Type IO Pins in mDDR Mode," and Table 23, "AC Electrical Characteristics of DDR Type IO Pins in SDRAM Mode," to exclude mention of slew rate. In Section 4.9.5.2, "Wireless External Interface Module (WEIM)," modified Figure 16, "Synchronous Memory Timing Diagram for Read Access—WSC = 1," through Figure 21, "Muxed A/D Mode Timing Diagram for Synchronous Read Access— WSC = 7, LBA = 1, LBN = 1, LAH = 1, OEA = 7." In Section 4.9.6, "Enhanced Serial Audio Interface (ESAI) Timing Specifications," modified Figure 37, "ESAI Transmitter Timing," and Figure 38, "ESAI Receiver Timing," to remove extraneous signals. Removed a note from Figure 37, "ESAI Transmitter Timing."
3	03/2009	<ul style="list-style-type: none"> In Section 4.3.1, "Powering Up," reverse positions of steps 5 and 6.
2	02/2009	<ul style="list-style-type: none"> Added the following parts to Table 1, "Ordering Information": PCIMX357CVM5B, MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B. Throughout consumer data sheet: Removed or updated information related to Media Local Bus interface. Updated Section 4.3.1, "Powering Up." Updated values in Table 9, "i.MX35 Power Modes."
1	12/2008	<ul style="list-style-type: none"> Updated Section 4.3.1, "Powering Up." Section 4.7, "Module-Level AC Electrical Specifications": Updated NFC, SDRAM and mDDR SDRAM timing. Inserted DDR2 SDRAM timing.
0	10/2008	Initial public release

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCIMX353CVM5B, MCIMX353DVM5B, MCIMX357CVM5B, and MCIMX357DVM5B.

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Japan:

Freescale Semiconductor Japan Ltd.
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ARCO Tower 15F
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Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
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Chaoyang District
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