Low Voltage 1:18 Clock Distribution Chip

Features

- LVPECL Clock Input
- 2.5V LVCMOS Outputs for PentiumII™ Microprocessor Support
- 200pS Maximum Targeted Output–to–Output Skew
- Maximum Output Frequency of 250MHz @3.3 V_{CC}
- 32–Lead LQFP and TQFP Packaging
- Single 3.3V or 2.5V Supply
- Pin and Function compatible with MPC942P

Functional Description

The PCS2I9942P is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the PCS2I9942C has an LVCMOS input clock while the PCS2I9942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 200pS, the PCS2I9942P is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

* Pentium II is a trademark of Intel Corporation

With low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the PCS2I9942P are ideal for driving series terminated transmission lines. With an output impedance of 12Ω, the PCS2I9942P can drive two series terminated transmission lines from each output. This capability gives the PCS2I9942P an effective fanout of 1:36. The PCS2I9942P provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the PCS2I9942P allow the device to interface directly with a LVPECL fanout buffer to build very wide clock fanout trees or to couple to a high frequency clock source. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The PCS2I9942P is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32 lead LQFP and TQFP package is chosen to optimize performance, board space and cost of the device. The 32–lead LQFP and TQFP have a 7x7mm^2 body size with conservative 0.8mm pin spacing.

Block Diagram

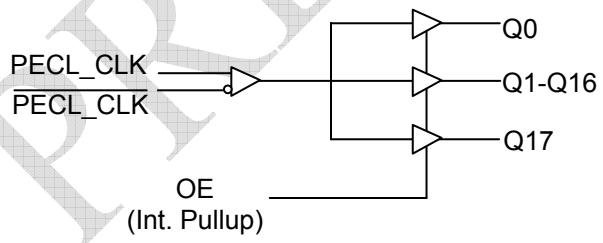

Table 1. Function Table

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

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1715 S. Bascom Ave Suite 200, Campbell, CA 95008 • Tel: 408-879-9077 • Fax: 408-879-9018
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Pin Diagram

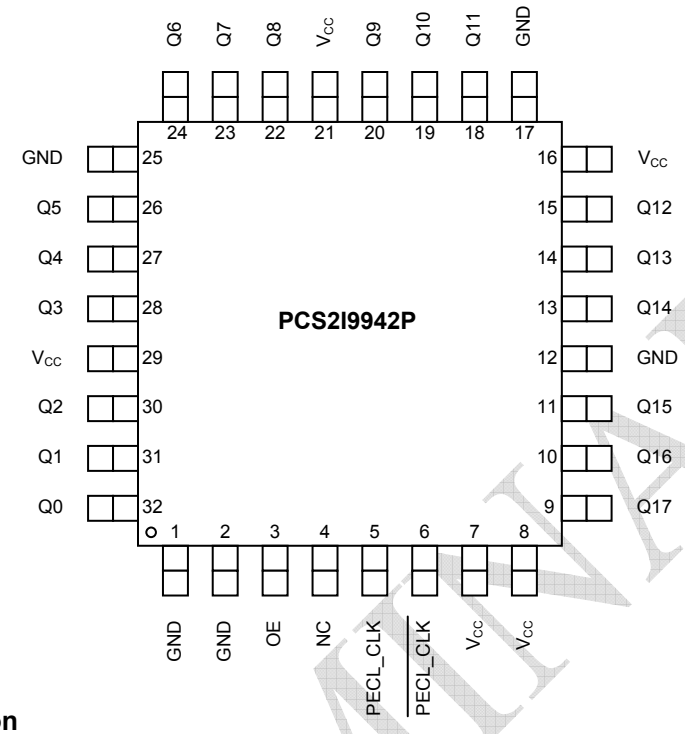


Table 2. Pin Description

Pin #	Pin Name	I/O	Type	Function
5 6	PECL_CLK, PECL_CLK	Input	LVPECL	LVPECL Clock Inputs
3	OE	Input	LVCMOS	Output enable/disable (high–impedance tristate)
4	NC			No connect
32,31,30,28,27,26,24,23,22,20,19,18,15, 14,13,11,10,9	Q0 – Q17	Output	LVCMOS	Clock outputs
1,2,12,17,25	GND	Supply	Ground	Negative power supply (GND) for I/O and core.
7,8,16,21,29	V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 3. Absolute Maximum Rating[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_I	Input Voltage	-0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	-40	125	°C

Note: 1. These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Table 4. DC Characteristics (T_A =-40° to +85°C, V_{CC} = 2.5V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL_CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}-1.0		V_{CC}-0.6	V	
V_{OH}	Output HIGH Voltage	2.0			V	I_{OH} = –16 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 16 mA
I_{IN}	Input Current			±200	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

Table 5. AC Characteristics (T_A =-40° to +85°C, V_{CC} = 2.5V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.8		4.0	nS	
t_{PHL}	Propagation Delay	2.0		4.3	nS	
$t_{sk(o)}$	Output-to-Output Skew within one bank			150	pS	
$t_{sk(pr)}$	Part–to–Part Skew [1]			2.2	nS	
$t_{sk(pr)}$	Part–to–Part Skew[2]			1.3	pS	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	nS	

Note: 1. Across temperature and voltage ranges, includes output skew.
2. For a specific temperature and voltage, includes output skew.

Table 6. DC Characteristics (T_A =-40° to +85°C, V_{CC} = 3.3V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL.CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}-1.0		V_{CC}-0.6	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage			0.6	V	I_{OL} = 20 mA
I_{IN}	Input Current			±200	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

Table 7. AC Characteristics (T_A =-40° to +85°C, V_{CC} = 3.3V ± 5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.5		3.2	nS	
t_{PHL}	Propagation Delay	1.5		3.6	nS	
$t_{sk(o)}$	Output-to-output Skew within one bank			150	pS	
$t_{sk(pr)}$	Part–to–Part Skew[1]			1.7	nS	
$t_{sk(pr)}$	Part–to–Part Skew[2]			1.0	pS	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	nS	

Note: 1. Across temperature and voltage ranges, includes output skew.
2. For a specific temperature and voltage, includes output skew.

Power Consumption of the PCS2I9942P and Thermal Management

The PCS2I9942P AC specification is guaranteed for the entire operating frequency range up to 250MHz. The PCS2I9942P power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the PCS2I9942P die junction temperature and the associated device reliability.

Table 8. Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the PCS2I9942P needs to be controlled and the thermal impedance of the board/package should be optimized.The power dissipated in the PCS2I9942P is represented in equation 1.

Where I_{CCQ} is the static current consumption of the PCS2I9942P, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 12 in case of the PCS2I9942P). The PCS2I9942P supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 8, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the PCS2I9942P in a series terminated transmission line system, equation 4.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \textit{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \left(V_{CC} - V_{OH} \right) + \left(1 - DC_Q \right) \cdot I_{OL} \cdot V_{OL} \right] \qquad \textit{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \textit{Equation 3}$$

$$f_{CLOCKMAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{JMAX} - T_A}{R_{thja}} - \left(I_{CCQ} \cdot V_{CC} \right) \right] \qquad \textit{Equation 4}$$

T_J,MAX should be selected according to the MTBF system requirements and Table 8. R_{thja} can be derived from Table 9. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in lower thermal impedance than indicated below.

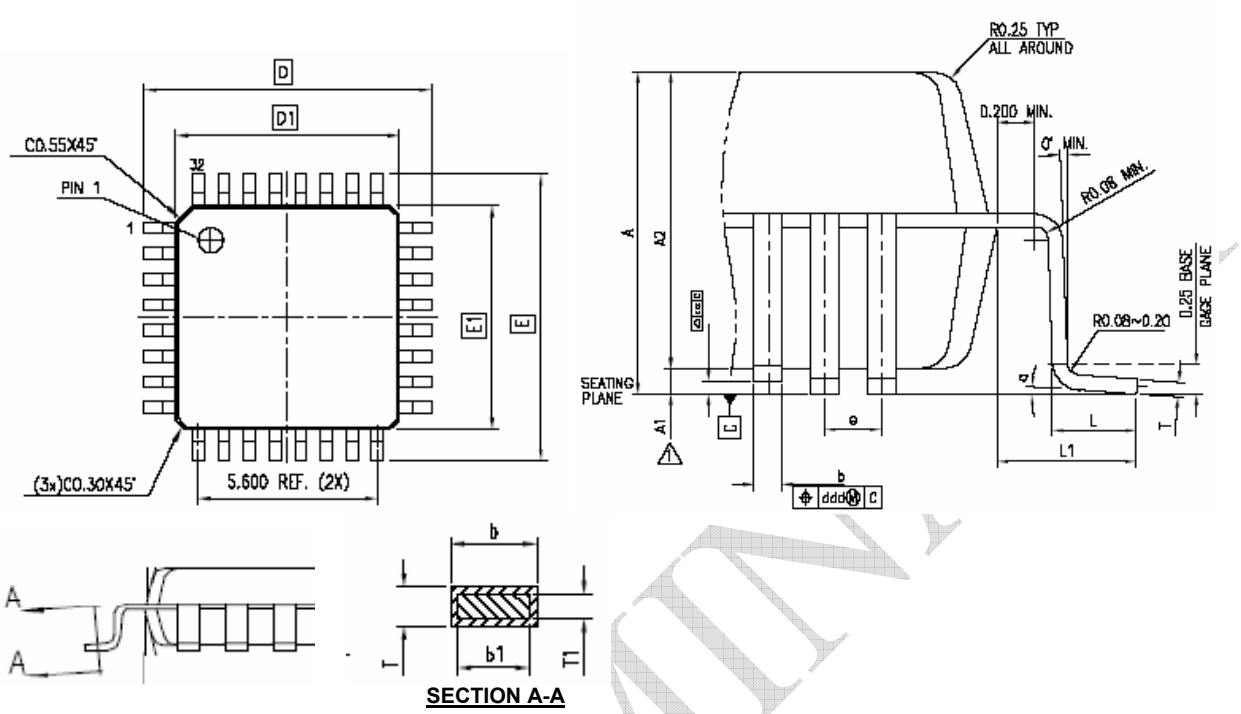
Table 9. Thermal package impedance of the 32LQFP

Convection, LFPM	R_{thja} (1P2S board), °C/W	R_{thja} (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the PCS2I9942P. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

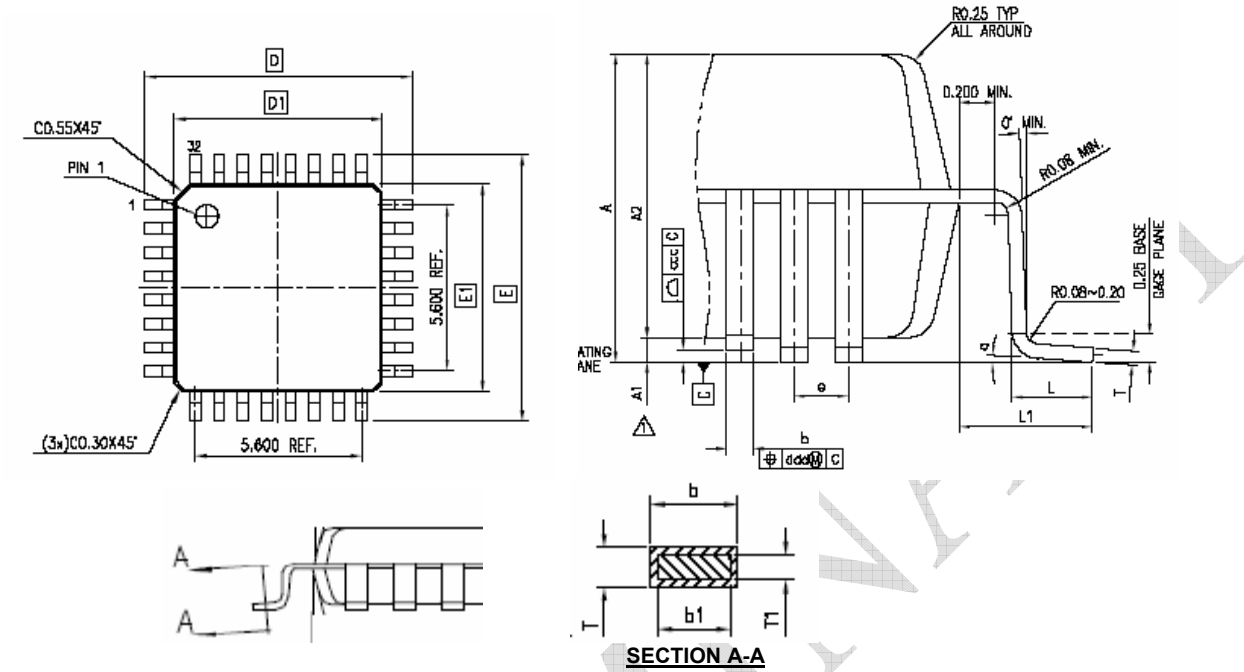
Package Information

32-lead TQFP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	…	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP

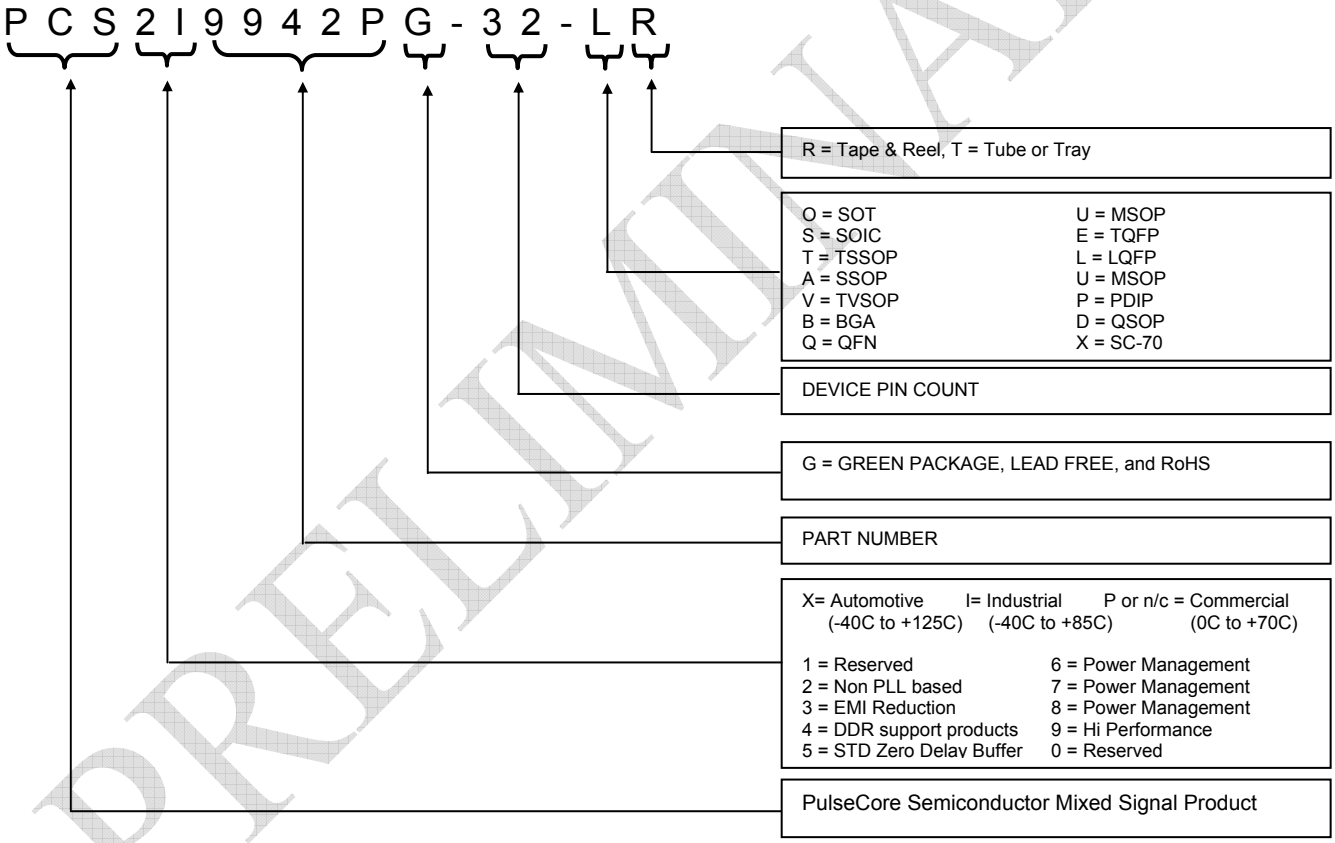


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0630	…	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

Ordering Information

Ordering Code	Marking	Package Type	Operating Range
PCS2P9942PG-32-LT	PCS2P9942PGL	32-pin LQFP, Tray, Green	Commercial
PCS2P9942PG-32-LR	PCS2P9942PGL	32-pin LQFP, Tape and Reel, Green	Commercial
PCS2P9942PG-32-ET	PCS2P9942PGE	32-pin TQFP, Green	Commercial
PCS2P9942PG-32-ER	PCS2P9942PGE	32-pin TQFP, Tape and Reel, Green	Commercial
PCS2I9942PG-32-LT	PCS2I9942PGL	32-pin LQFP, Tray, Green	Industrial
PCS2I9942PG-32-LR	PCS2I9942PGL	32-pin LQFP,Tape and Reel, Green	Industrial
PCS2I9942PG-32-ET	PCS2I9942PGE	32-pin TQFP, Green	Industrial
PCS2I9942PG-32-ER	PCS2I9942PGE	32-pin TQFP,Tape and Reel, Green	Industrial

Device Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003