Power Supply IC Series for TFT-LCD Panels

Single-channel Source Voltage Output Power Supply + Gamma Buffer Amp ICs

BD8151EFV,BD8157EFV

No.09035EBT11

●Description

The BD8151EFV,BD8157EFV power supply IC are designed for use with TFT-LCD panels. It incorporates a built-in source voltage step-up switching regulator and gamma correction buffer amp. The combination of a source power supply and gamma correction buffer on a single chip delivers significant cost savings.
Compatible with input voltages from 2.5 V to 5.5 V (BD8151EFV), 2.1 V to 4.0 V (BD8157EFV), the IC supports low-voltage operation and reaches over 85% efficiency with a 2.5 V input, contributing to low power consumption designs.

●Features

1) Single-chip implementation of a source power supply and gamma correction buffer
2) Support for low-voltage operation, with input voltages from 2.5 V to 5.5 V (BD8151EFV)
   2.1 V to 4.0 V (BD8157EFV)
3) Built-in 1.4 A, 0.2 Ω low-voltage FET
4) Switchable step-up DC/DC switching frequencies: 600 kHz/1.2 MHz
5) Current mode PWM control
6) Under-voltage lockout protection circuit
7) Built-in overcurrent protection circuit
8) Built-in thermal shutdown circuit

●Applications

Satellite navigation systems, laptop PC TFT LCD panels
LCD monitor panels

●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limit	Unit
Power supply voltage		Vcc	7	V
Power dissipation		Pd	1000*	mW
Operating temperature range	BD8151EFV	Topr	−40 to +85	℃
	BD8157EFV		−40 to +125	
Storage temperature range		Tstg	−55 to +150	℃
Switching pin current		Isw	1.5**	A
Switching pin voltage		Vsw	15	V
VS voltage		VS	15	V
Maximum junction temperature		Tjmax	150	℃

* Reduced by 8 mW/℃ over 25℃, when mounted on a glass epoxy board (70 mm x 70 mm x 1.6 mm).
** Must not exceed Pd.

●Recommended Operating Ranges (Ta = 25℃)

Parameter	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Power supply voltage BD8151EFV	Vcc	2.5	3.3	5.5	V
Power supply voltage BD8157EFV	Vcc	2.1	2.5	4.0	V
Switching current	ISW	—	—	1.4	A
Switching pin voltage	VSW	—	—	14	V
VS pin voltage	VS	5	9	14	V

●**Electrical Characteristics BD8151EFV (Unless otherwise specified, Ta = 25℃; Vcc = 3.3V, ENB = 3.3V)**

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Triangular waveform oscillator]						
Oscillating frequency 1	FOSC1	540	600	660	kHz	FCLK = 0 V
Oscillating frequency 2	FOSC2	1.08	1.20	1.32	MHz	FCLK = Vcc
[Overcurrent protection circuit]						
Overcurrent limit	ISW	—	2	—	A	
[Soft start circuit]						
SS source current	ISO	6	10	14	μA	Vss = 0.5 V
[Under-voltage lockout protection circuit]						
Off threshold voltage	VUTOFF	2.1	2.2	2.3	V	
On threshold voltage	VUTON	2.0	2.1	2.2	V	
[Error amp]						
Input bias current	IB	—	0.1	0.5	μA	
Feedback voltage	VFB	1.232	1.245	1.258	V	Buffer
[Output]						
On resistance	RON	—	200	300	mΩ	*Isw = 1 A
Max. duty ratio	DMAX	72	80	88	%	RL = 100 Ω
[ENB]						
ENB on voltage	VON	Vcc × 0.7	Vcc	—	V	
ENB off voltage	VOFF	—	0	Vcc × 0.3	V	
[Overall]						
Standby current	ISTB	—	0	10	μA	VENB = 0 V
Average consumption current	ICC	—	1.2	2.4	mA	no switching
[Amp]						
Input bias current	Ibo	−1	0	1	μA	IN += 4.5 V
Drive current 1	IOO1	50	70	140	mA	OUT1 to OUT4
Drive current 2	IOO2	150	200	400	mA	VCOM
Max. output current	Voho	VS-0.16	VS-0.1	—	V	Io = −5 mA, IN += VS
Min. output current	Vohl	—	0.1	0.16	V	Io = 5 mA, IN += 0 V

○ This product is not designed for protection against radio active rays.
* Design guarantee (No total shipment inspection is made.)

●**Electrical Characteristics BD8157EFV (Unless otherwise specified, Ta = 25℃; Vcc = 2.5V, ENB = 2.5V)**

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Triangular waveform oscillator]						
Oscillating frequency 1	FOSC1	480	600	720	kHz	FCLK = 0 V
Oscillating frequency 2	FOSC2	0.96	1.20	1.44	MHz	FCLK = Vcc
[Overcurrent protection circuit]						
Overcurrent limit	ISW	—	2	—	A	
[Soft start circuit]						
SS source current	ISO	6	10	14	μA	Vss = 0.5 V
[Under-voltage lockout protection circuit]						
Off threshold voltage	VUTOFF	1.7	1.8	1.9	V	
On threshold voltage	VUTON	1.6	1.7	1.8	V	
[Error amp]						
Input bias current	IB	—	0.1	0.5	μA	
Feedback voltage	VFB	1.232	1.245	1.258	V	Buffer
[Output]						
On resistance	RON	—	200	600	mΩ	*Isw = 1 A
Max. duty ratio	DMAX	75	85	95	%	RL = 100 Ω
[ENB]						
ENB on voltage	VON	Vcc × 0.7	Vcc	—	V	
ENB off voltage	VOFF	—	0	Vcc × 0.3	V	
[Overall]						
Standby current	ISTB	—	0	10	μA	VENB = 0 V
Average consumption current	ICC	—	1.2	2.4	mA	no switching
[Amp]						
Input bias current	Ibo	−1	0	1	μA	IN += 4.5 V
Drive current 1	IOO1	50	70	140	mA	OUT1 to OUT4
Drive current 2	IOO2	120	200	400	mA	VCOM
Max. output current	Voho	VS-0.16	VS-0.1	—	V	Io = −5 mA, IN += VS
Min. output current	Vohl	—	0.1	0.16	V	Io = 5 mA, IN += 0 V

○ This product is not designed for protection against radio active rays.
* Design guarantee (No total shipment inspection is made.)

●**Reference Data (Unless otherwise specified, Ta = 25℃)**

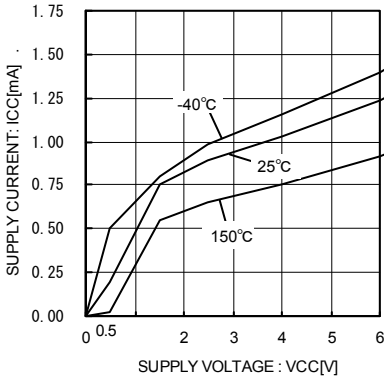


Fig. 1 Total Supply Current

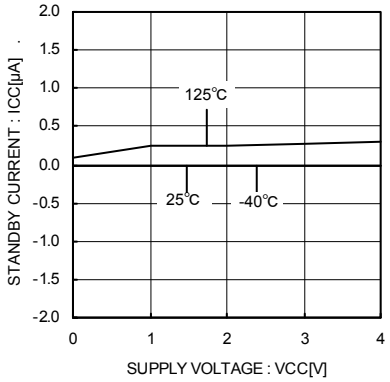


Fig. 2 Standby Current

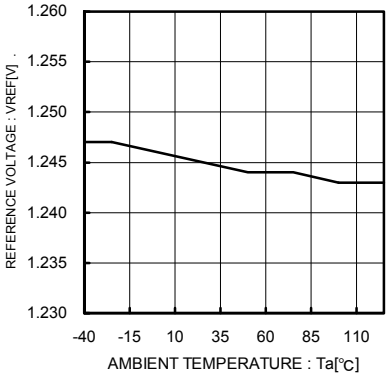


Fig. 3 Reference Voltage Temperature

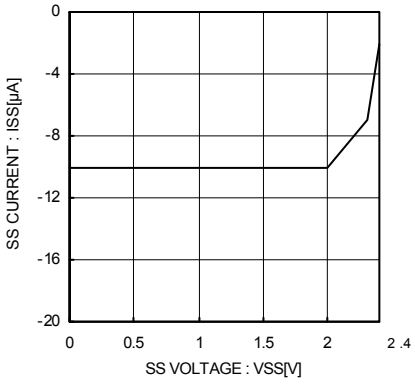


Fig. 4 SS Source Current

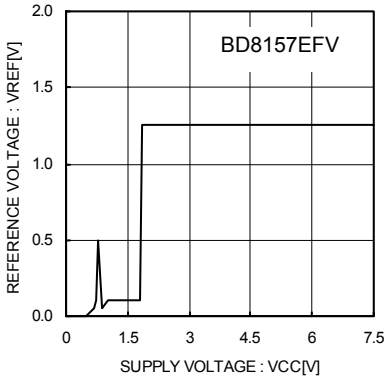


Fig. 5 Reference Voltage Temperature

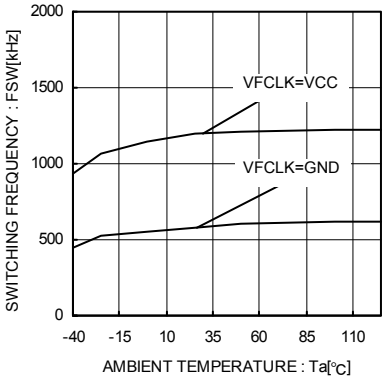


Fig. 6 Switching Frequency Temperature

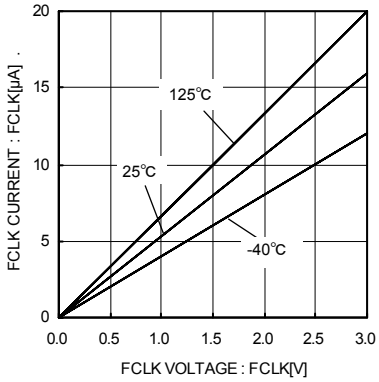


Fig. 7 FCLK Pin Current

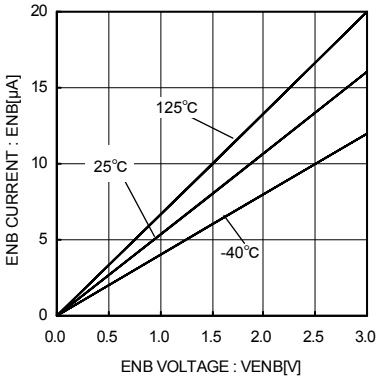


Fig. 8 ENB Pin Current

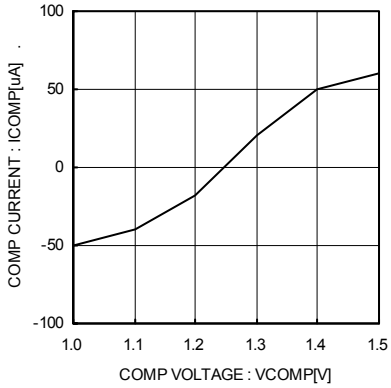


Fig. 9 COMP Sinking vs Source Current

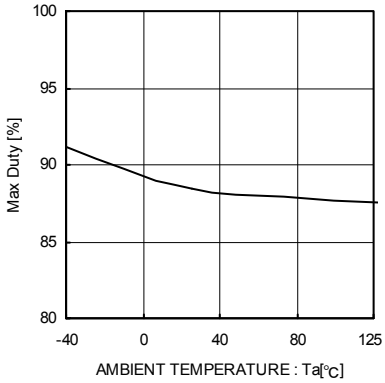


Fig. 10 Max. Duty Ratio Temperature

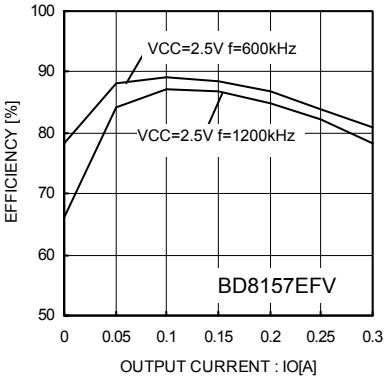


Fig. 11 Vcc = 2.5 V Power Efficiency

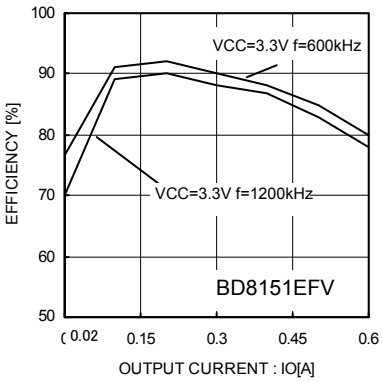


Fig. 12 Vcc = 3.3 V Power Efficiency

●Reference Data (Unless otherwise specified, Ta = 25℃)

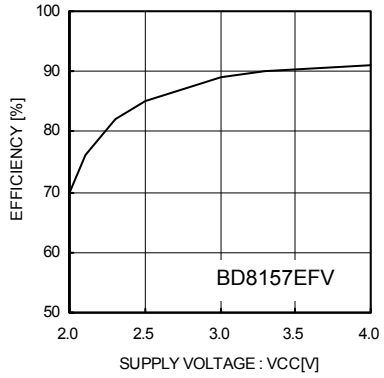


Fig. 13 Power Efficiency vs Power Supply Voltage

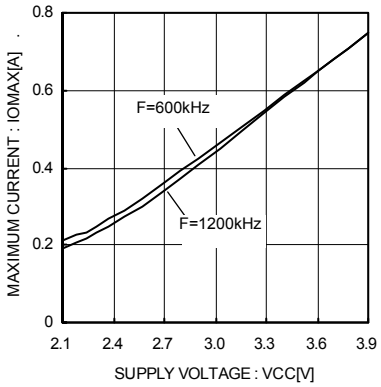


Fig. 14 Max. Load Current vs Power Supply Voltage

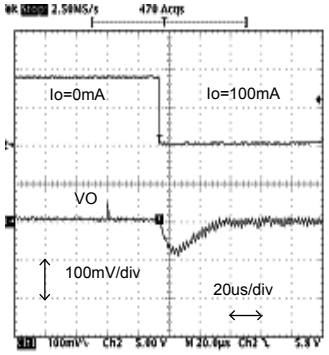


Fig. 15 Load Response Waveform

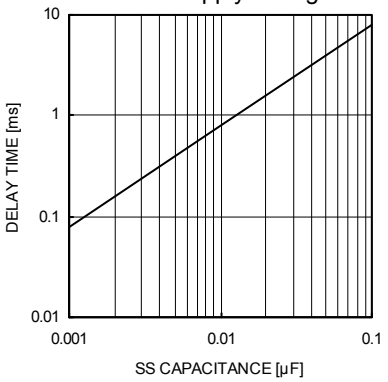


Fig. 16 SS Capacitance vs Delay Time

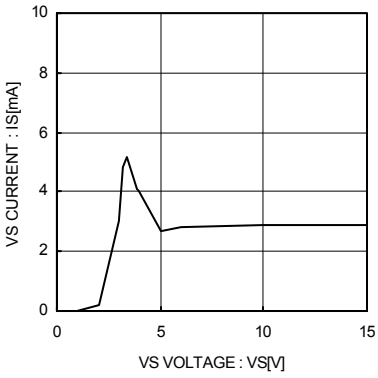


Fig. 17 VS Pin Current

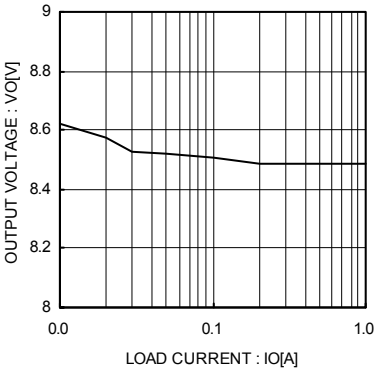


Fig. 18 Output voltage Load Regulation 1

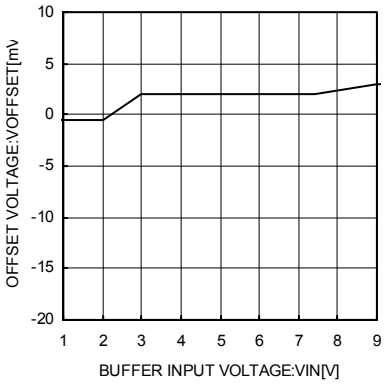


Fig. 19 Buffer Voltage

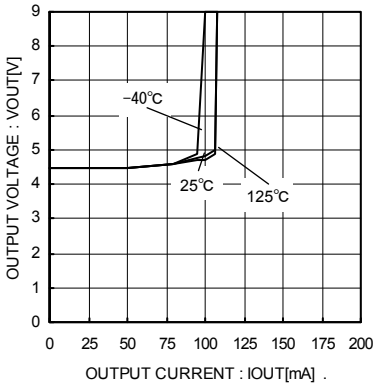


Fig. 20 Buffer Sinking Current

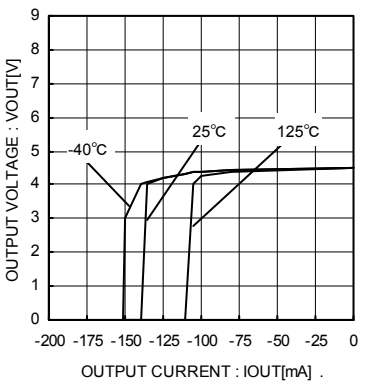


Fig. 21 Buffer Source Current

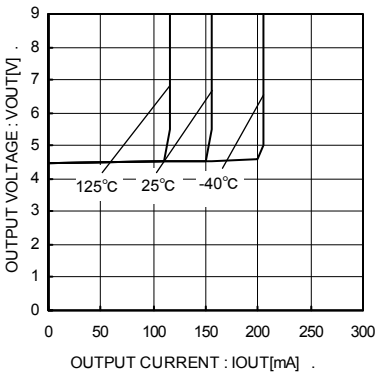


Fig. 22 VCOM Sinking Current

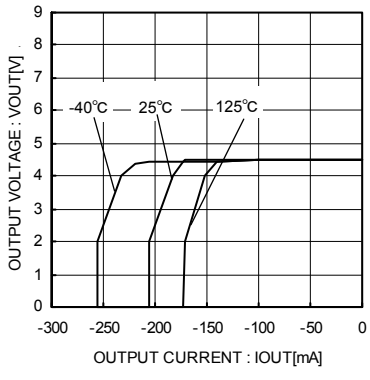


Fig. 23 VCOM Source Current

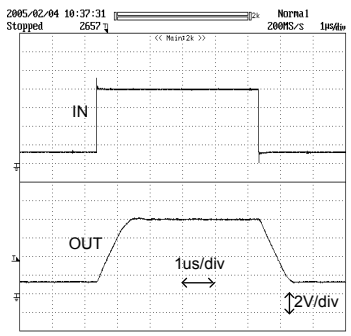
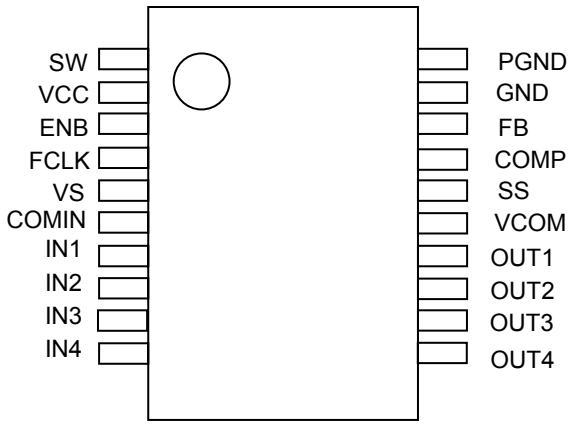


Fig. 24 Slew Rate Waveform

●**Pin Assignment Diagram**



●**Block Diagram**

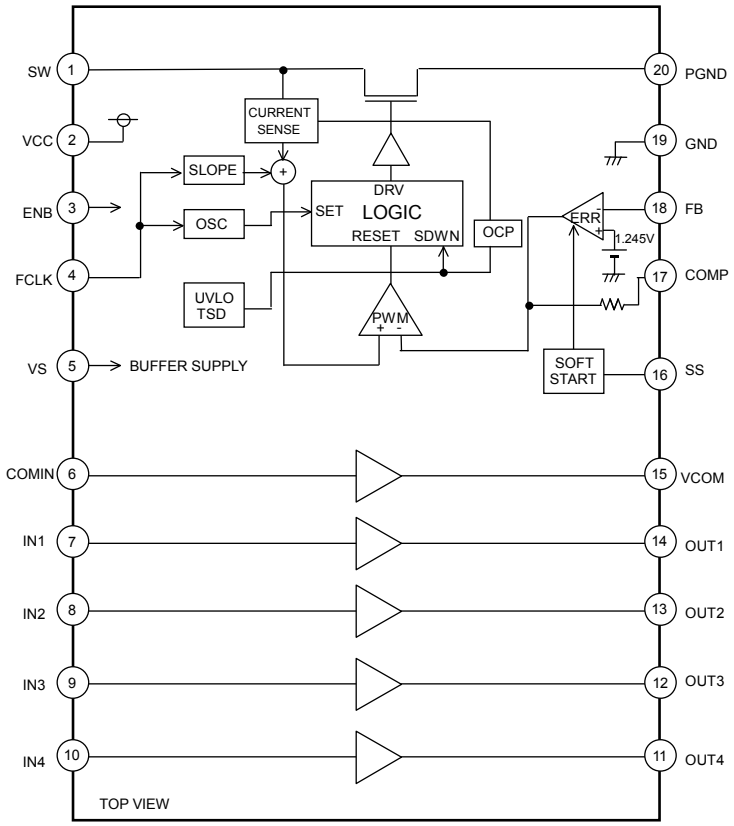


Fig. 25 Pin Assignment Diagram and Block Diagram

●**Pin Assignment Diagram and Pin Functions**

Pin No.	Pin name	Function
1	SW	N-channel power FET drain output
2	VCC	Power supply input pin
3	ENB	Control input pin
4	FCLK	Frequency switching pin
5	VS	Buffer power supply input pin
6	COMIN	VCOM input pin
7	IN1	Amp input pin 1
8	IN2	Amp input pin 2
9	IN3	Amp input pin 3
10	IN4	Amp input pin 4
11	OUT4	Amp output pin 4
12	OUT3	Amp output pin 3
13	OUT2	Amp output pin 2
14	OUT1	Amp output pin 1
15	VCOM	VCOM output pin
16	SS	Soft start current output pin
17	COMP	Error amp output pin
18	FB	Error amp inversion input pins
19	GND	Ground pin
20	PGND	Ground pin

●Description of Operation of Each Block

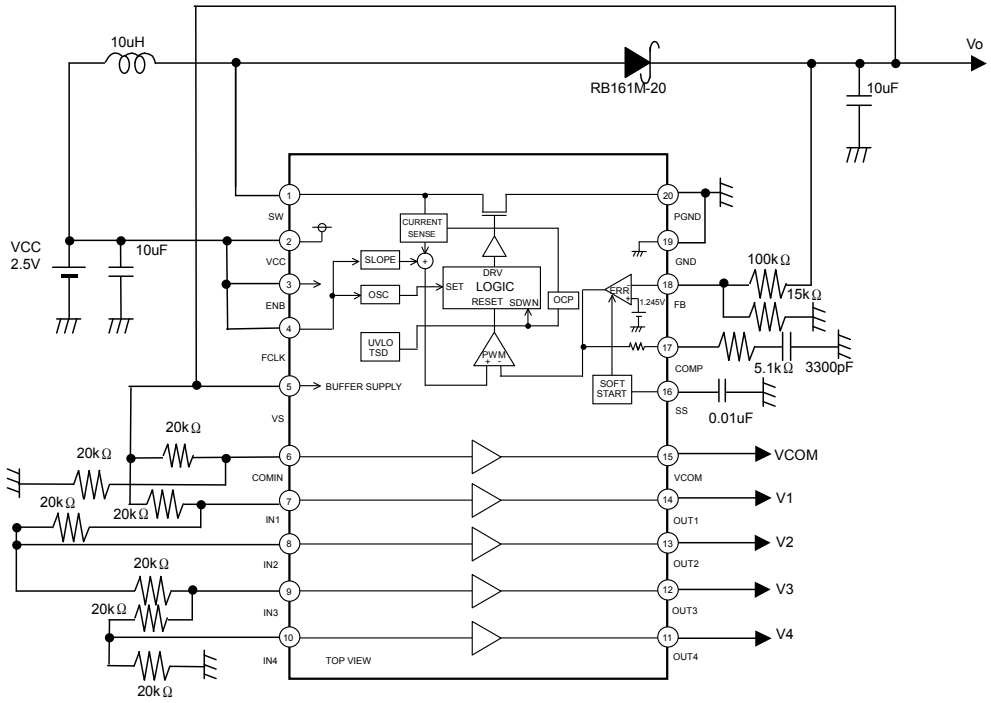


Fig. 26 Application Circuit Diagram

- Error amp (ERR)
  This is the circuit to compare the reference voltage 1.245 V (Typ.) and the feedback voltage of output voltage. The COM pin voltage resulting from this comparison determines the switching duty. At the time of start, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

- Oscillator (OSC)
  This block generates the oscillating frequency. Either a 600 kHz or 1.2 MHz (Typ.) frequency can be selected with the FCLK pin.

- SLOPE
  This block generates the triangular waveform from the clock generated by OSC. Generated triangular waveform is sent to the PWM comparator.

- PWM
  The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is decided internally, it does not become 100%.

- Reference voltage (VREF)
  This block generates the internal reference voltage of 1.245 V (Typ.).

- Protection circuit (UVLO/TSD)
  UVLO (under-voltage lockout protection circuit) shuts down the circuits when the voltages are 2.2 V (Typ.BD8151EFV) 1.8 V (Typ.ND8157EFV) or lower. Thermal shutdown circuit shuts down IC at 175°C (Typ.) and recovers at 160°C (Typ.).

- Overcurrent protection circuit (OCP)
  Current flowing to the power FET is detected by voltage at the CURRENT SENSE and the overcurrent protection operates at 3 A (Typ.). When the overcurrent protection operates, switching is turned off and the SS pin capacity is discharged.

- Soft start circuit
  Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the inrush current.

- Buffer amp and VCOM
  This buffer amp is used to set the gamma correction voltage, which can be set in from 0.2 V to (VOUT - 0.2 V). Use the VOUT resistance division to set the gamma correction voltage. The VCOM voltage is set similarly.

●**Timing Chart**

Startup sequence

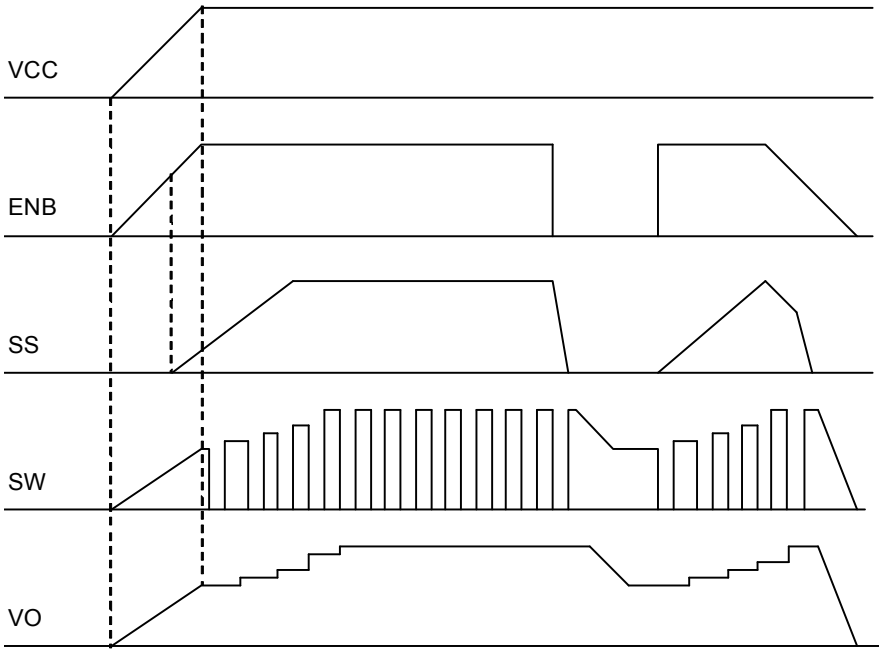


Fig. 27 Startup sequence

Overcurrent protection operating

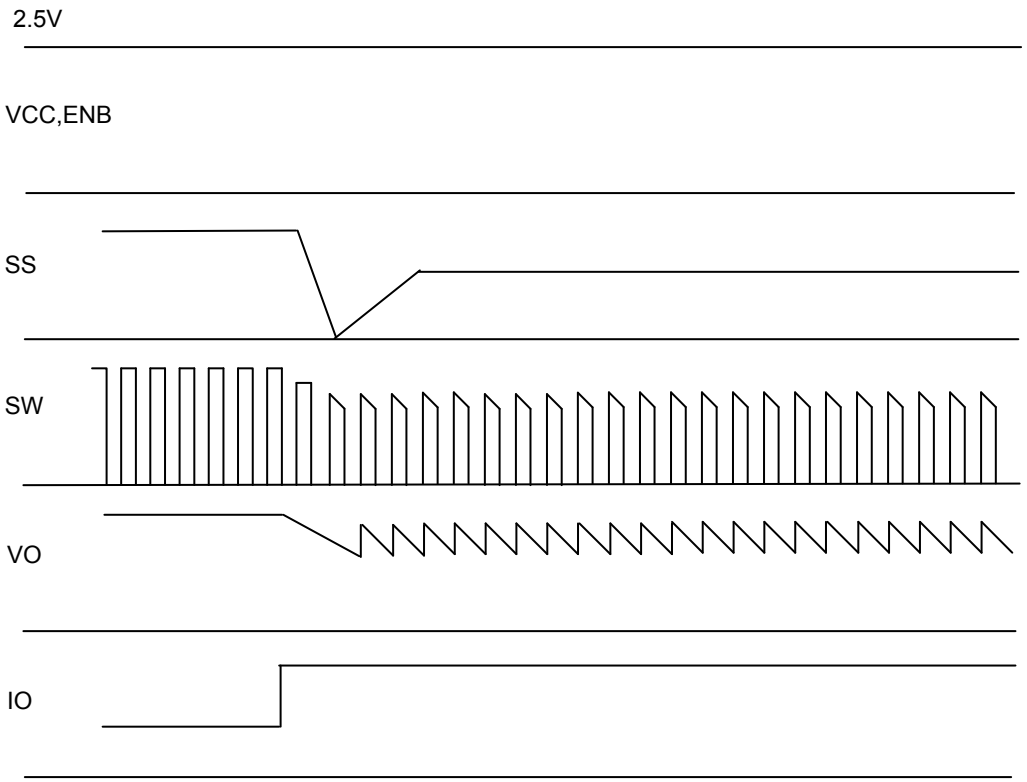


Fig. 28 Overcurrent protection operating

●**Selecting Application Components**

(1) Setting the output L constant

The coil L to use for output is decided by the rating current I_{LR} and input current maximum value I_{INMAX} of the coil.

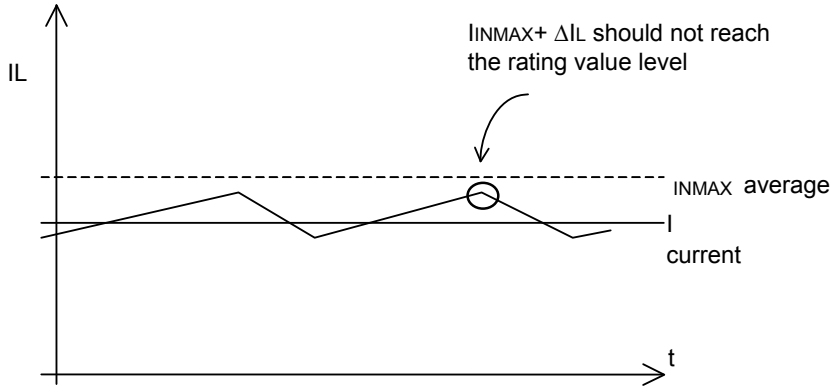


Fig. 29 Coil Current Waveform

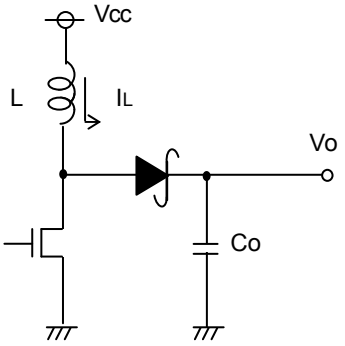


Fig. 30 Output Application Circuit Diagram

Adjust so that $I_{INMAX} + \Delta I_L$ does not reach the rating current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} Vcc \times \frac{Vo-Vcc}{Vcc} \times \frac{1}{f} \text{ [A]}$$ Where, f is the switching frequency.

Set with sufficient margin because the coil L value may have the dispersion of approx. ±30%. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD8157EFV uses the current mode DC/DC converter control and has the optimized design at the coil value. The following coil values are recommended from the aspects of power efficiency, response and safety. When the coil out of this range is selected, the stable continual operation is not guaranteed such as the switching waveform becomes irregular. Please pay attention to it.

Switching frequency: L = 10 µH to 22 µH at 600 kHz
Switching frequency: L = 4.7 µH to 15 µH at 1,200 kHz

(2) Setting the output capacitor

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{Vcc}{Vo} \times \left(I_{LMAX} - \frac{\Delta I_L}{2}\right) \text{ [V]}$$ Where, f is the switching frequency.

Perform setting so that the voltage is within the allowable ripple voltage range.
For the drop voltage during sudden load change; V_{DR}, please perform the rough calculation by the following equation.

$$VDR = \frac{\Delta I}{Co} \times 10\ \mu\text{sec} \text{ [V]}$$

However, 10 µs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the input capacitor

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For this reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 µF and less than 100 mΩ. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Selecting the output rectification diode

Schottky barrier diode is recommended as the rectification diode to use at the DC/DC converter output stage. Select the diode paying attention to the max. inductor current and max. output voltage.

Max. Inductor current $I_{INMAX} + \Delta I_L <$ Rating current of diode

Max. output voltage $V_{OMAX} <$ Rating voltage of diode

Since each parameter has 30% to 40% of dispersion, be sure to design providing sufficient margins.

(5) Design of the feedback resistor constant

Refer to the following equation to set the feedback resistor. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set to a 10 kΩ or lower, it causes the reduction of power efficiency. If it is set to 330 kΩ or larger, the offset voltage becomes larger by the input bias current 0.4 μA (Typ.) in the internal error amplifier.

$$Vo = \frac{R8 + R9}{R9} \times 1.245 \quad [V]$$

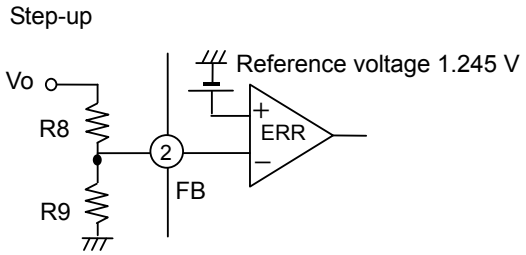


Fig. 31Feedback Resistance Setting

(6) Setting the soft start time

Soft start is required to prevent the coil current at the time of startup from increasing and the overshoot of the output voltage at the starting time. Fig. 32 shows the relation between the capacitance and soft start time. Please refer to it to set the capacitance.

As the capacitance, 0.001 μF to 0.1μF is recommended. If the capacitance is set to 0.001 μF, the overshooting may occur on the output voltage. If the capacitance is set to 0.1 μF or larger, the excessive back current flow may occur in the internal parasitic elements when the power is turned OFF and it may damage IC. When the capacitor of 0.1 μF or larger is used, be sure to insert a diode to Vcc in series, or a bypass diode between the SS pin and VCC.

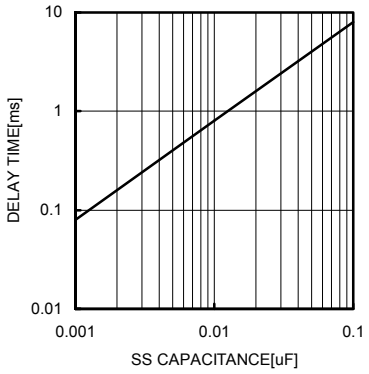


Fig.32 SS Pin Capacitance vs Delay Time

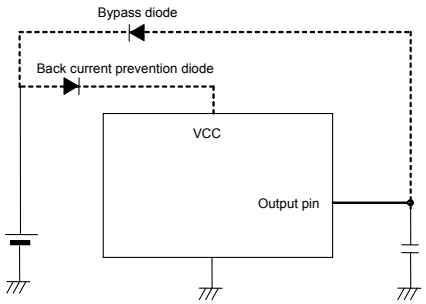


Fig. 33 Bypass Diode Example

When there is the startup relation (sequences) with other power supplies, be sure to use the high accuracy product (such as X5R). Soft start time may vary according to the input voltage, output voltage loads, coils and output capacity. Be sure to verify the operation using the actual product.

(7) Setting the ENB pin

When the ENB pin is set to Hi, the internal circuit becomes active and the DC/DC converter starts operating. When it is set to Low, the shut down is activated and all circuits will be turned OFF.

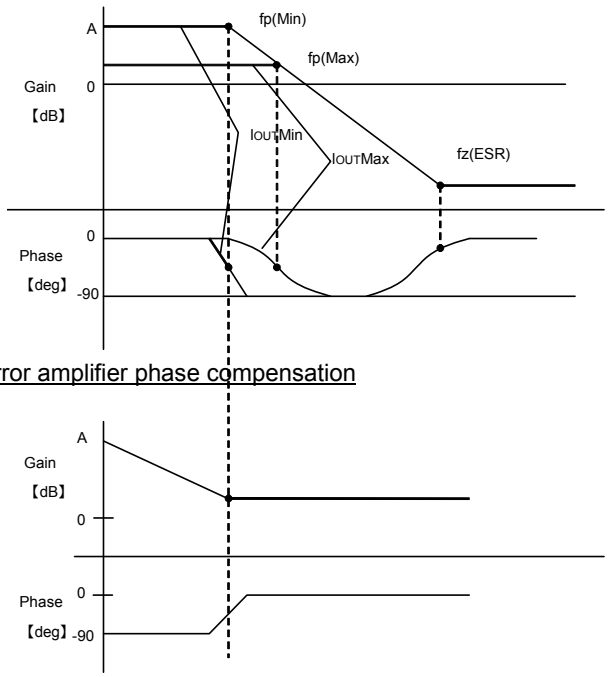
(8) Setting the frequency by FCLK

It is possible to change the switching frequency by setting the FCLK pin to Hi or Low. When it is set to Low, the product operates at 600 kHz (Typ.). When it is set to Hi, the product operates at 1,200 kHz (Typ.).

(9) Setting R_C, C_C of the phase compensation circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with C_C and R_C to the output from the error amplifier as shown in the illustration.

Open loop gain



Error amplifier phase compensation

Fig. 34 Gain vs Phase

$$fp = \frac{1}{2\pi \times Ro \times Co} \quad [Hz]$$

$$fz\ (ESR) = \frac{1}{2\pi \times ESR \times Co} \quad [Hz]$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_O increases and the pole frequency lowers.

$$fp(Min) = \frac{1}{2\pi \times ROMax \times Co} \quad [Hz] \quad \text{(At light-load)}$$

$$fz(Max) = \frac{1}{2\pi \times ROMin \times Co} \quad [Hz] \quad \text{(At heavy-load)}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$fp\ (Amp.) = \frac{1}{2\pi \times Rc \times Cc} \quad [Hz]$$

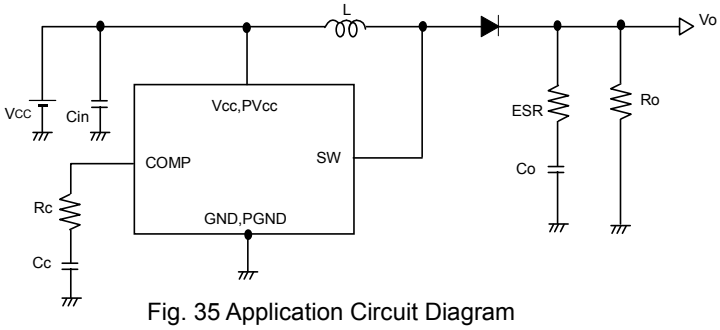


Fig. 35 Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole fp (Min.), which is created by the output capacitor and load resistor, with CR zero compensation of the error amplifier as shown below.

$$fz\ (Amp.) = fp\ (Min.)$$

$$\longrightarrow \frac{1}{2\pi \times Rc \times Cc} = \frac{1}{2\pi \times Romax \times Co} \quad [Hz]$$

As the setting range for the resistor, 1 kΩ to 10 kΩ is recommended. When the resistor is set to 1 kΩ or lower, the effect by phase compensation becomes low and it may cause the oscillation of output voltage. When it is set to 10 kΩ or larger, the COMP pin becomes Hi-Z and the switching noise becomes easy to superpose. Therefore the stable switching pulse cannot be generated and the irregular ripple voltage may be generated on the output voltage.

As the setting range for the capacitance, 3,300 pF to 10,000 pF is recommended. When the capacitance is set to 3,300 pF or lower, the irregular ripple voltage may be generated on the output voltage due to the effect of switching noise. When it is set to 10,000 pF or larger, the response becomes worse and the output voltage fluctuation becomes large. Accordingly it may require the output capacitor which is larger than the necessary value.

(10) Using the buffer amp and VCOM

The 4-channel buffer amp and 1-channel VCOM output are used to generate the gamma compensation voltage that is input to the source driver. The VS pin serves as the power supply for the buffer amp and VCOM.

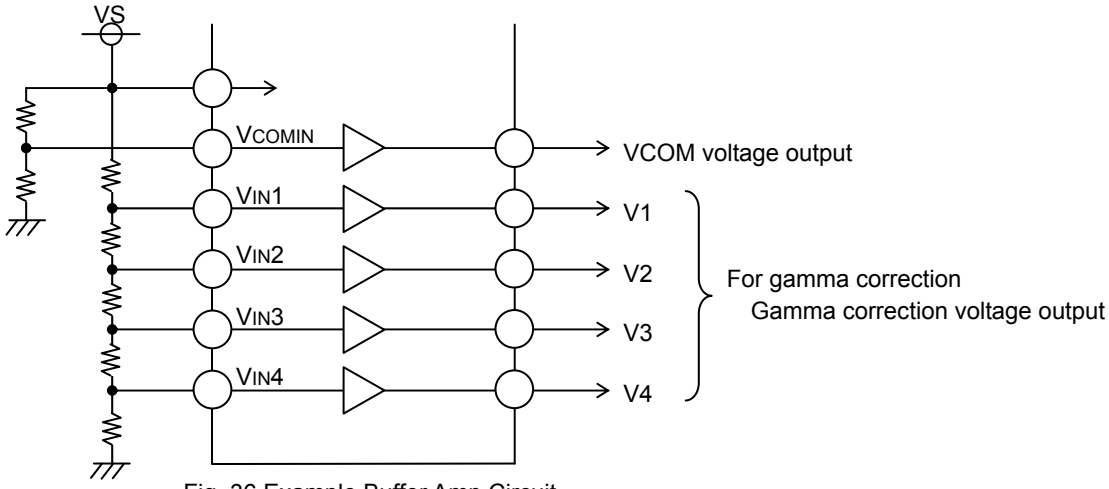


Fig. 36 Example Buffer Amp Circuit

Use caution as the gamma correction buffer amp and VCOM have different output current capacities. A range from I/O power supply to ground potentials can be set for the built-in buffer amplifier. If output voltage noise becomes problematic, insert a 0.1 µF capacitor in the output circuit. A capacitance value of 0 pF to 1 µF is recommended for this capacitor. Large capacitance values of 1 µF or larger may cause back current to flow through internal parasitic diodes in the event of a supply voltage ground fault, causing damage to internal IC elements. For applications where such modes are anticipated, implement a bypass diode or other preventive measure.

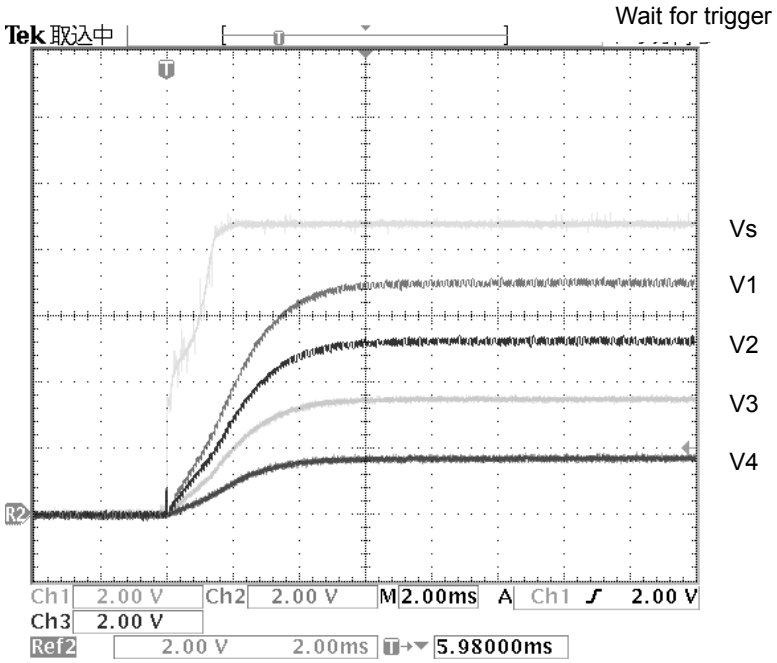


Fig. 37 Gamma Correction Voltage Startup Waveform

●Application Examples

* Although ROHM is sure that the application examples are recommendable ones, further check the characteristics of components that require high precision before using them.When a circuit is used modifying the externally connected circuit constant, be sure to decide allowing sufficient margins considering the dispersion of values by external parts as well as our IC including not only the static but also the transient characteristic.
For the patent, we have not acquired the sufficient confirmation. Please acknowledge the status.

(1) When the charge pump is removed from the DC/DC converter to make it 3-channel output mode:
It is possible to create the charge pump by using the switching operation of DC/DC converter. When the application shown in the following diagram is used, 1-channel DC/DC converter output, 1-channel positive side charge pump and 1-channel negative side charge pump can be output as a total of 3 channels.

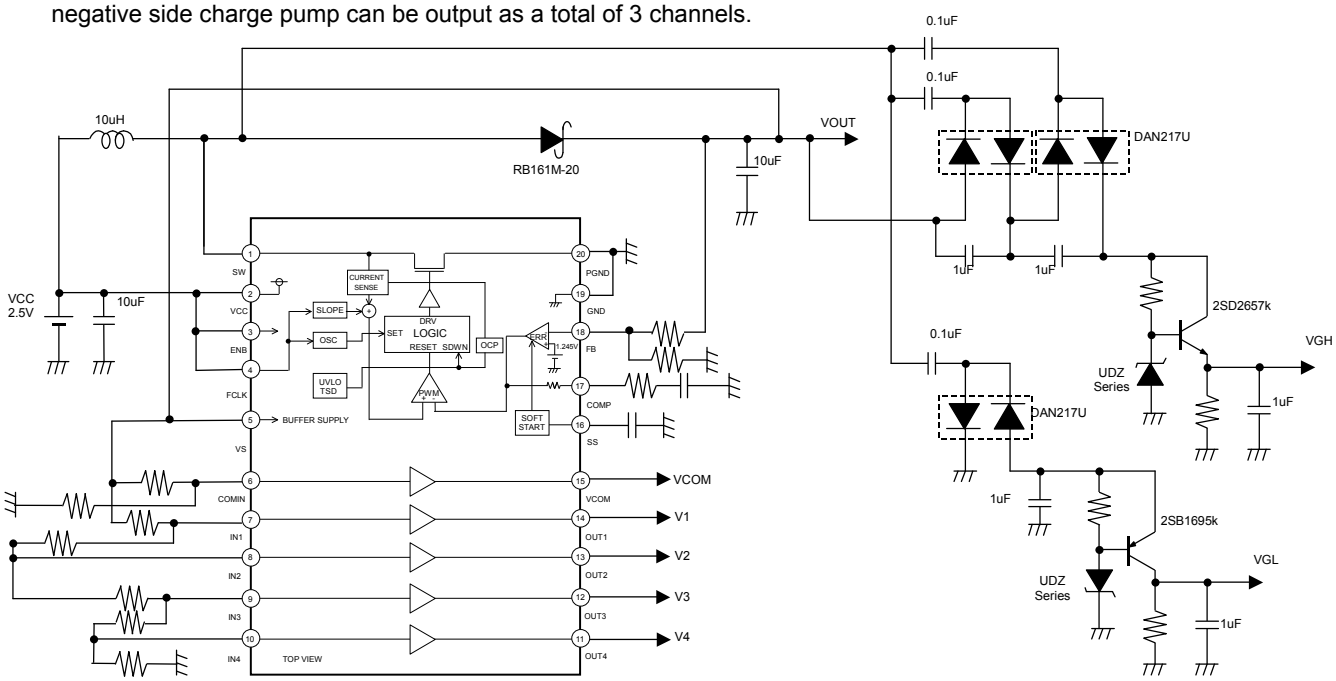


Fig. 38 3 ch Application Circuit Diagram Example

(2) When the output voltage is set to 0 V:
Since the switch does not exist between the input and output in the application using the step-up type DC/DC converter, the output voltage is generated even if the IC is turned off. When it is intended to keep the output voltage 0 V until IC operates, insert the switch as shown in the following circuit diagram.

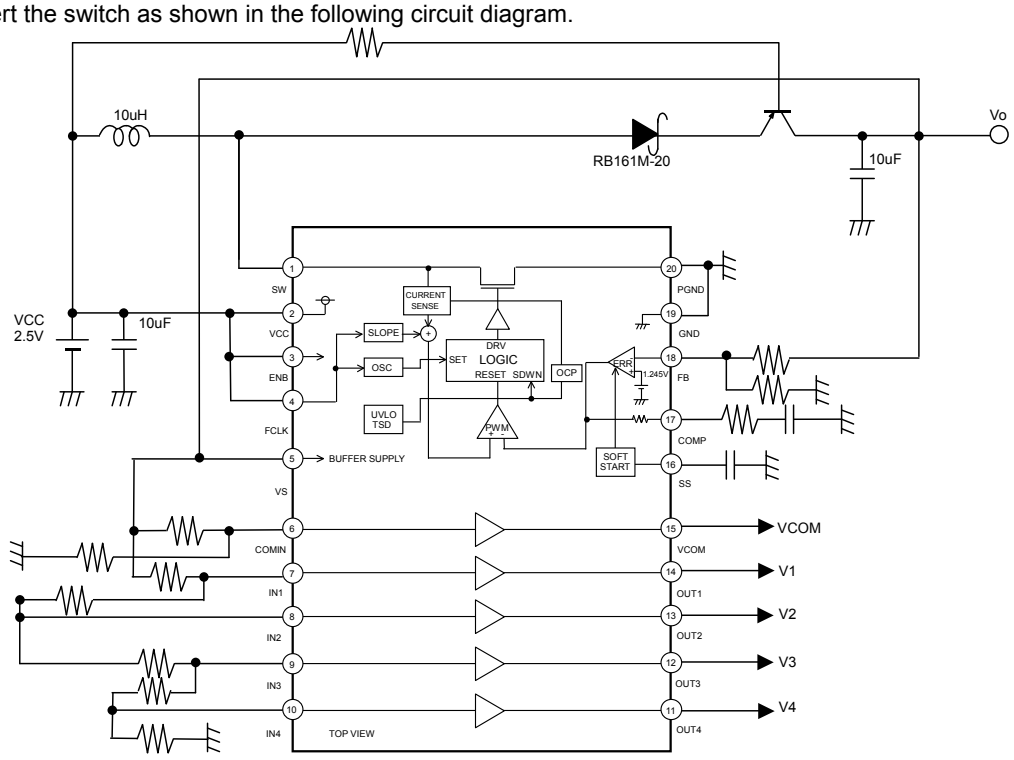
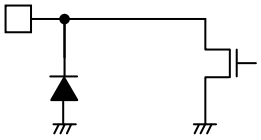


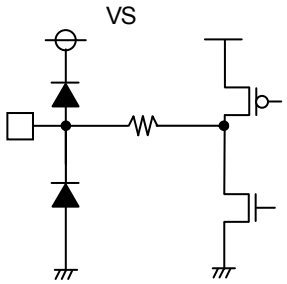
Fig. 39 Switch Application Circuit Diagram Example

●**I/O Equivalent Circuit Diagrams**

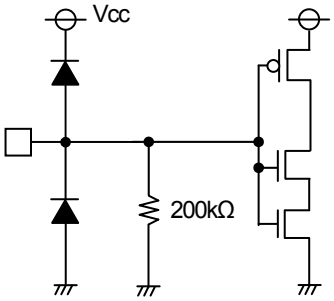
1.SW



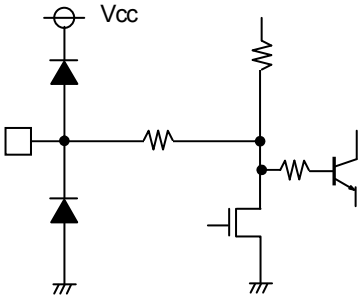
11.OUT4 12.OUT3 13.OUT2 14.OUT1 15.VCOM



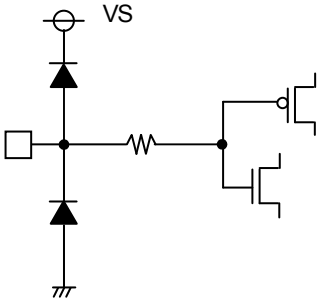
3.ENB 4.FCLK



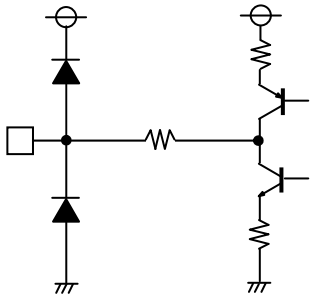
16.SS



6.COMIN 7.IN1 8.IN2 9.IN3 10.IN4



17.COMP



18.FB

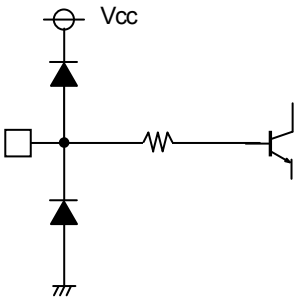


Fig.40 I/O Equivalent Circuit Diagrams

●Notes for use

1) Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
2) GND potential
   Ensure a minimum GND pin potential in all operating conditions.
3) Setting of heat
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
4) Pin short and mistake fitting
   Use caution when orienting and positioning the IC for mounting on an application board. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.
5) Actions in strong magnetic field
   Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.
6) Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.
7) Ground wiring patterns
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.
8) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in Fig. 41, a parasitic diode or a transistor operates by inversing the pin voltage and GND voltage.
   The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as the application of voltages lower than the GND (P substrate) voltage to input and output pins.

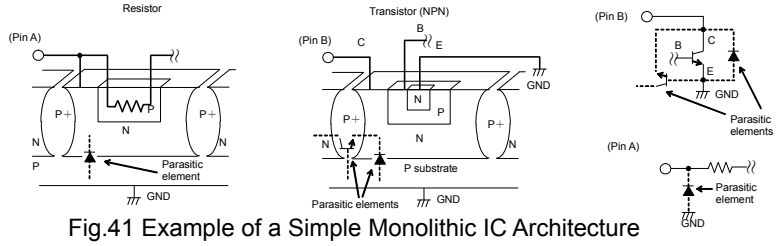


Fig.41 Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
   An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC destruction that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.
10) Thermal shutdown circuit (TSD)
   This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature Tj will trigger the temperature protection circuit to turn off all output power elements. The circuit automatically resets once the chip's temperature Tj drops.
   Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.
11) Testing on application boards
   At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●**Power Dissipation Reduction**

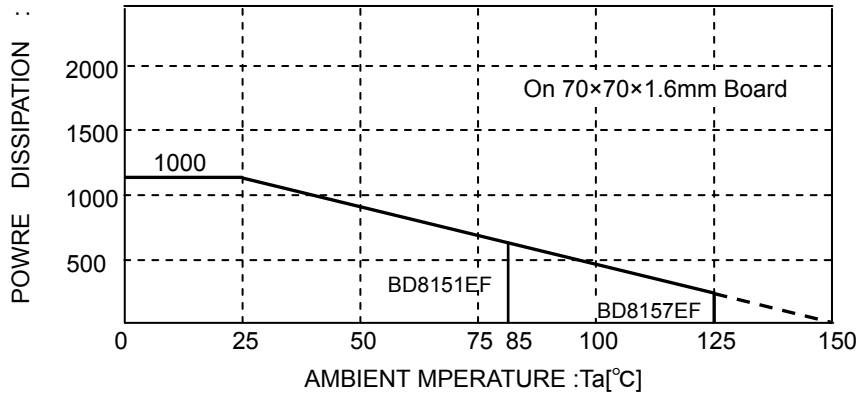


Fig.42 Power Dissipation Reduction

●Ordering part number

B	D	8	1	5	1	E	F	V	-	E	2

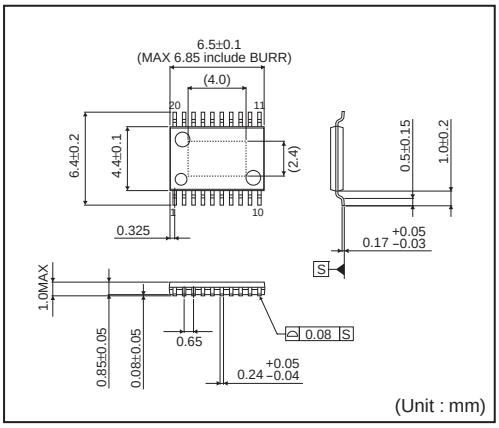
Part No.

Part No.
8151
8157

Package
EFV : HTSSOP-B20

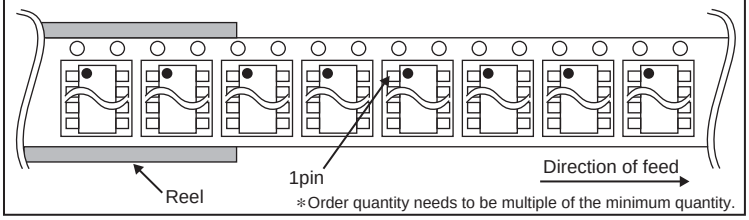
Packaging and forming specification
E2: Embossed tape and reel

HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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