ROHM
SEMICONDUCTOR

STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	Step down DC/DC converter controller for Laptop PC
PRODUCT SERIES	**BD9526AMUV**
FEATURES	■ Built in 2ch H^3REG DC/DC converter controller ■ The Light load mode efficiency is improved by SLLM (Simple Light Load Mode) ■ Adjustable Switching Frequency (f=200kHz~500kHz) ■ Built in 3ch Linear Regulator

○Absolute Maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Terminal voltage	VIN1, VIN2, CTL	30 *1*2	V
	EXTVCC, FB1, FB2, Is+1, Is+2, MCTL	7 *1*2	V
	FS1, FS2, REF1, REF2, LG1,LG2,TEST1,TEST2	INTVCC+0.3 *1*2	V
	BOOT1, BOOT2	35 *1*2	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	7 *1*2	V
	HG1	BOOT1+0.3 *1*2	V
	HG2	BOOT2+0.3 *1*2	V
	EN1, EN2	6 *1*2	V
	DGND, PGND1, PGND2	AGND±0.3 *1*2	V
Power dissipation 1	Pd1	0.38*3	W
Power dissipation 2	Pd2	0.88 *4	W
Power dissipation 3	Pd3	2.06 *5	W
Power dissipation 4	Pd4	4.56 *6	W
Operating temperature range	Topr	-10～+100	℃
Storage temperature range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Do not however exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 3.0mW for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*4 Reduced by 7.0mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer. (Copper foil area : 0mm²))
*5 Reduced by 16.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (1st and 4th copper foil area : 20.2mm², 2nd and 3rd copper foil area : 5505mm²))
*6 Reduced by 36.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 4 layers. (All copper foil area : 5505mm²))

○Operating supply voltage range (Ta=25℃)

Parameter	Symbol	MIN.	MAX.	Unit
Terminal voltage	VIN1,VIN2	7	25	V
	EXTVCC	4.5	5.5	V
	CTL	-0.3	25	V
	EN1, EN2	-0.3	5.5	V
	BOOT1, BOOT2	4.5	30	V
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	-0.3	5.5	V
	REF1, REF2	1	2.75	V
	Is+1, Is+ 2, FB1, FB2	1.9	5.6	V
	MCTL	-0.3	INTVCC+0.3	V

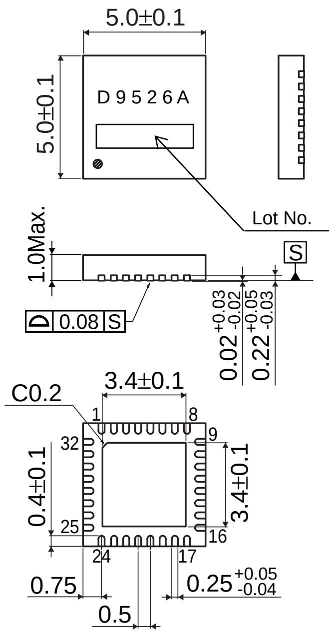
★ This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○Electrical characteristics (unless otherwise noted, Ta=25℃ VIN1=VIN2=12V, CTL=5V, EN1=EN2=5V, REF1=2.5V, REF2=1.65V, RFS1=RFS2=51kΩ)

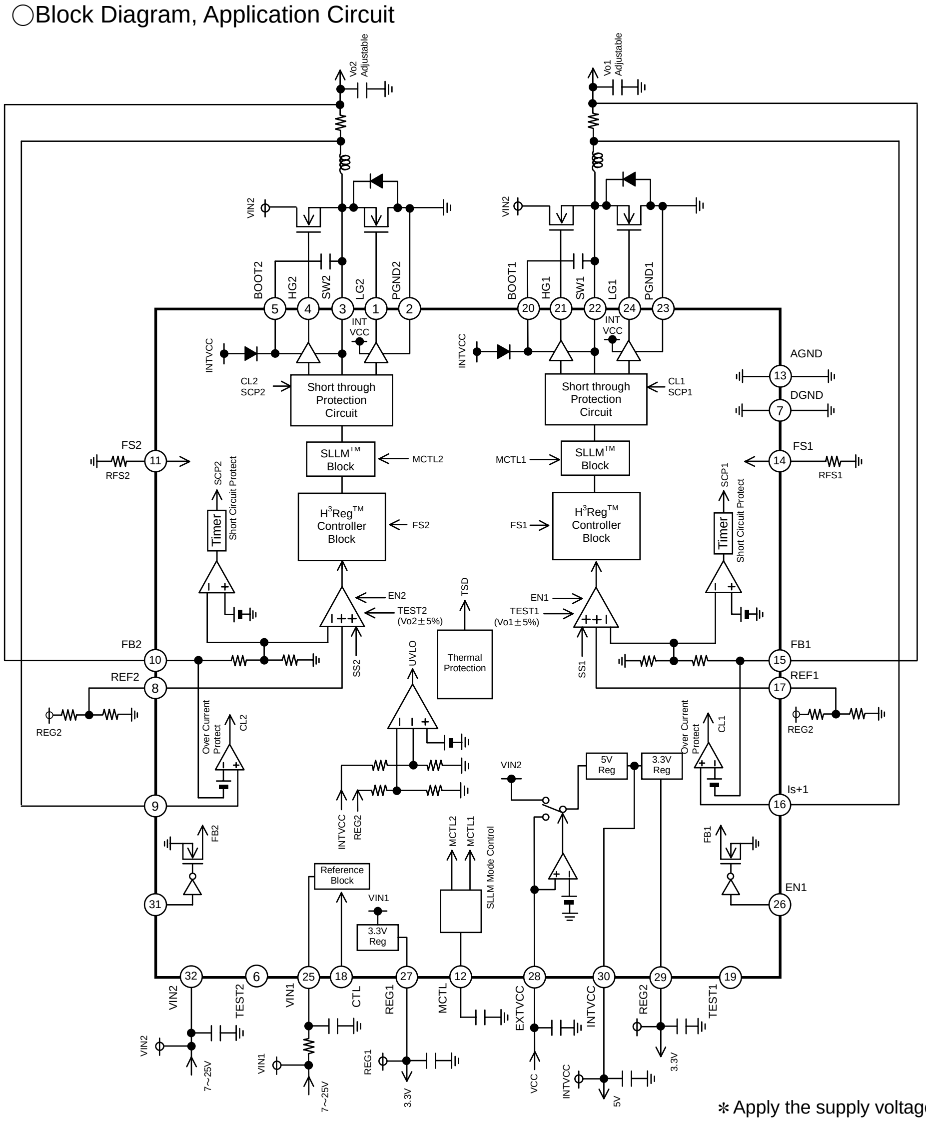
Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
VIN1 Bias Current	IIN1	-	130	200	μA	CTL=5V
VIN2 Bias Current 1	IIN2_1	-	100	150	μA	CTL=5V, EN1=EN2=0V
VIN2 Bias Current 2	IIN2_2	-	20	40	μA	CTL=5V, EN1=EN2=0V,EXTVCC=5V
VIN1 Shutdown Current	ISHD1	-	0	10	μA	CTL=0V
VIN2 Shutdown Current	ISHD2	-	0	10	μA	CTL=0V
CTL Low Voltage	VCTLL	-0.3	-	0.8	V	
CTL High Voltage	VCTLH	2.3	-	25	V	
CTL Bias Current	ICTL	-	1	3	μA	VCTL=5V
EN Low Voltage	VENL	-0.3	-	0.8	V	
EN High Voltage	VENH	2.3	-	5.5	V	
EN Bias Current	IEN	-	1	3	μA	VEN=3V
[5V Linear Regulator]						
INTVCC output Voltage	VINTVCC	4.90	5.00	5.10	V	IINTVCC1=1mA
INTVCC Maximum Current	IINTVCC	200	-	-	mA	IREG2=0mA
INTVCC Line regulation	Reg.lINT	-	-	180	mV	VIN=7.5 to 25V
INTVCC Load regulation	Reg.LINT	-	-	50	mV	IINTVCC=0 to 30mA
[3.3V Linear Regulator]						
REG1 Output Voltage	VREG1	3.27	3.30	3.33	V	IREG1=1mA
REG1Maximum Current	IREG1	100	-	-	mA	
REG1Line regulation	Reg.l1	-	-	33	mV	VIN=7.5 to 25V
REG1Load regulation	Reg.L1	-	-	33	mV	IREG1=0 to 50mA
REG2 Output Voltage	VREG2	3.27	3.30	3.33	V	IREG2=1mA
REG2Maximum Current	IREG2	100	-	-	mA	
REG2Line regulation	Reg.l2	-	-	20	mV	VIN=7.5 to 25V
REG2Load regulation	Reg.L2	-	-	30	mV	IREG2=0 to 100mA
[5V Switch Block]						
EXTVCC Input Threshold Voltage	Vcc_UVLO	4.2	4.4	4.6	V	EXTVCC: Sweep up
EXTVCC Input Delay Time	TVcc	2	4	8	ms	
Switch Resistance	RVcc	-	1.0	2.0	Ω	
[Under voltage lock out block for DC/DC]						
INTVCC Threshold Voltage	REG1_UVLO	4.0	4.2	4.4	V	INTVCC: Sweep up
REG2 Threshold Voltage	REG2_UVLO	2.45	2.65	2.85	V	REG2: Sweep up
Hysteresis voltage	dV_UVLO	50	100	200	mV	INTVCC, REG2: Sweep down
[Error amplifier block]						
Feed back voltage 1	VFB1	REF1×2 -25m	REF1×2	REF1×2 +25m	V	
FB1 Bias Current	IFB1	5	25	50	μA	FB1=5V
Output Discharge Resistance 1	RDISOUT1	-	1	3	kΩ	
Feed back voltage 2	VFB2	REF2×2 -25m	REF2×2	REF2×2 +25m	V	
FB2 Bias Current	IFB2	3	16	32	μA	FB2=3.3V
Output Discharge Resistance 2	RDISOUT2	-	1	3	kΩ	
REF1, REF2 Bias Current	IREF1, IREF2	-1	-	1	μA	
[H^3REG block]						
ON Time 1	TON1	0.860	0.960	1.060	μs	REF=2.5V
ON Time 2	TON2	0.570	0.670	0.770	μs	REF=1.65V
Maximum On Time	TONMAX	3.5	7	14	μs	
Minimum Off Time	TOFFMIN	-	0.2	0.4	μs	
[FET Driver block]						
HG higher side ON resistor	HGHON	-	3.0	6.0	Ω	
HG lower side ON resistor	HGLON	-	2.0	4.0	Ω	
LG higher side ON resistor	LGHON	-	2.0	4.0	Ω	
LG lower side ON resistor	LGLON	-	0.5	1.0	Ω	
[Short circuit protection block]						
SCP Threshold Voltage	VSCP	REF×2×0.66	REF×2×0.7	REF×2×0.74	V	
Delay Time	TSCP	0.5	1	2	ms	
[Current limit protection block]						
Maximum offset voltage	dVSMAX	43	50	57	mV	
Is+1 bias current	IISP1	-	2.5	10	μA	Is+1=2V
Is+2 bias current	IISP2	-	2.5	10	μA	Is+2=2V
[Soft Start block]						
Soft Start Time	TSS	0.5	1.0	2.0	ms	
[SLLM mode control block]						
MCTL terminal voltage 1	VCONT	-0.3	-	0.3	V	Continuous mode
MCTL terminal voltage 2	VQLLM	1.5	-	3.0	V	QL^2M mode (Maximum LG off time : 40usec)
MCTL terminal voltage 3	VSLLM	4.5	-	INTVCC+0.3	V	SL^2M mode (Maximum LG off time : ∞)
MCTL float level	VMCTL	1.5	-	3.0	V	

○Physical Dimensions



VQFN032-V5050
(UNIT : mm)

○Block Diagram, Application Circuit



○Pin Description

PIN No.	PIN Name
1	LG2
2	PGND2
3	SW2
4	HG2
5	BOOT2
6	TEST2
7	DGND
8	REF2
9	Is+2
10	FB2
11	FS2
12	MCTL
13	AGND
14	FS1
15	FB1
16	Is+1
17	REF1
18	CTL
19	TEST1
20	BOOT1
21	HG1
22	SW1
23	PGND1
24	LG1
25	VIN1
26	EN1
27	REG1
28	EXTVCC
29	REG2
30	INTVCC
31	EN2
32	VIN2
-	FIN

＊Apply the supply voltage EXTVCC pin after INTVCC pin is operated.

○Output condition table

Input			Output				
CTL	EN1	EN2	REG1(3.3V)	REG2(3.3V)	INTVCC	DC/DC1	DC/DC2
Low	Low	Low	OFF	OFF	OFF	OFF	OFF
Low	Low	High	OFF	OFF	OFF	OFF	OFF
Low	High	Low	OFF	OFF	OFF	OFF	OFF
Low	High	High	OFF	OFF	OFF	OFF	OFF
High	Low	Low	ON	ON	ON	OFF	OFF
High	Low	High	ON	ON	ON	OFF	ON
High	High	Low	ON	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON	ON

○NOTE FOR USE

(1) Absolute maximum rating
The device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the source, such as short mode or open mode, cannot be identified if the device is destroyed, it is important to take physical safety measures (such as fusing) if a special mode in excess of absolute rating limits is to be implemented.

(2) Supply line
In case the motor’s reverse electromotive force gives rise to the return of regenerative current, measures should be taken to establish a channel for the current, such as adding a capacitor between the power supply and GND. In determining the approach to take, make sure that no problems will be posed by the various characteristics involved, such as capacitance loss at low temperatures with an electrolytic capacitor.

(3) GND potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

(4) Thermal design
Be sure to factor in allowable power dissipation (Pd) in actual operation, and to build sufficient margin into the thermal design to accommodate this power loss.

(5) Operation in strong magnetic fields
Use in strong electromagnetic fields may cause malfunctions. Exercise caution with respect to electromagnetic fields.

(6) ASO
Set the parameters so that output Tr will not exceed the absolute maximum rating or ASO value when the IC is used.

(7) Thermal shutdown circuit
This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the chip temperature reaches the threshold value listed below. When TSD is on, the device goes to high impedance mode. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature [℃] (typ.)
175	15

(8) Ground wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(9) Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND.

(10) For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

(11) Short-circuits between pins and and mounting errors
Do not short-circuit between output pin and supply pin or ground, or between supply pin and ground. Mounting errors, such as incorrect positioning or orientation, may destroy the device.

Notes

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