ROHM SEMICONDUCTOR

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT SERIES	8-Channel Switching Regulator Controller for Digital Camera
TYPE	BD9757MWV
PIN ASSIGNMENT	Fig.1
BLOCK DIAGRAM	Fig.2
PACKAGE	Fig.3

Functions

- ●1.5V minimum input operating
- ●Supplies power for the internal circuit by step-up converter(CH1).
- ●Contains step-up converter(2ch), step-down converter(4ch), ,inverting (1ch), with 31 step brightness controller for step-up converter(1ch).
- ●5channels contain transistor for synchronous rectifying action mode.
- ●2channels contain FETs for the step-up converter.
- ●All channels contain internal compensation.
- ●It is possible separately control except CH1 and CH3.
- ●Operating frequency 1.2MHz(CH1～5), 600kHz(CH6～8).
- ●Contains output interception circuit when over load.
- ●2 channels have high side switches with soft start function.
- ●Thermally enhanced UQFN044V6060 package(6mm x 6mm, 0.4mm pitch).

○Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VBAT	−0.3～7	V
Power Input Voltage	VHx1～5	−0.3～7	V
	HS78H	−0.3～7	V
	VLx7,8	−0.3～22	V
Output Current	IomaxLx1	±2.5	A
	IomaxHx1	±1.5	A
	IomaxHx2,5	+1.0	A
	IomaxHx3,4	+0.8	A
	IomaxHS78	+1.2	A
	IomaxLx7,8	±1.0	A
Power Dissipation	Pd	0.54 (*1)	W
Operating Temperature	Topr	−25～+85	°C
Storage Temperature	Tstg	−55～+150	°C
Junction Tempareture	Tjmax	+150	°C

(*1) Without external heat sink, the power dissipation reduces by 4.32mW/°C over 25°C

○Recommended operating conditions

Parameter	Symbol	Limit MIN	Limit TYP	Limit MAX	Unit
Power Supply Voltage	VBAT	1.5	−	5.5	V
VREF Pin Connecting Capacitor	CVREF	0.47	1.0	4.7	μF
VREGA Pin Connecting Capacitor	CVREGA	0.47	1.0	4.7	μF

Status of this document

The Japanese version of this document is the official specification. Please use the translation version of this document as a reference to expedite understanding of the official version.

If these are any uncertainty in translation version of this document, official version takes priority.

○CH8 recommended operating conditions

Parameter	Symbo	Limit MIN	Limit TYP	Limit MAX	Unit
Fixed H when determine brightness	T(ON)	265X1/fosc	−	−	S
Fixed L when OFF	T(OFF)	256X1/fosc	−	−	S
Fixed H when setting brightness	T(H)	500	−	10000	nS
Fixed L when setting brightness	T(L)	500	−	10000	nS
Fixed H when EN start-up	T(EN)	4X1/fosc	−	−	S
Fixed L before setting brightness	T(CLR)	7X1/fosc	−	255X1/fosc	S
Brightness setting time When start-up	T(SET)	−	−	2048X1/fosc	S

○Electrical characteristics（Ta=25°C, VCCOUT=5.0V, VBAT=3V, STB13～7=3V,UPIC8=2.5V）

Parameter	Symbol	Limit MIN	Limit TYP	Limit MAX	Unit	Conditions
【Internal Regulator VREGA】						
Output Voltage	VREGA	2.4	2.5	2.6	V	Io=5mA
【Prevention Circuit of Miss Operation by Low voltage Input】						
Threshold Voltage	Vstd1	－	2.0	2.3	V	VREGA Monitor
Hysteresis Width1	⊿Vstd1	50	100	200	mV	
Threshold Voltage 2	Vstd2	－	2.4	2.5	V	VCCOUT Monitor
Hysteresis Width	⊿Vstd1	100	200	300	mV	
【Short Circuit Protection】						
SCP detect time	Tscp	20	25	30	ms	
Timer start threshold voltage	Vtcinv	0.38	0.48	0.58	V	INV Monitor CH3～5
【Start-up Circuit】						
Frequency	Fstart	150	300	600	kHz	
Start-up VBAT Voltage	Vst1	1.5	－	－	V	
Start-up CH Soft Start Time	Tss1	1.8	3.0	5.3	msec	
【Oscillator】						
Frequency CH1～5	fosc1	1.0	1.2	1.4	MHz	
Frequency CH6～8	fosc2	0.5	0.6	0.7	MHz	
Max duty 2,3,4,5 (step-down)	Dmax1d	－	－	100	%	(※1)
Max duty 1 (step-up)	Dmax1u	86	92	96	%	
Max duty 6,7,8	Dmax2	86	92	96	%	
【Error Amp】						
Input Bias current	IINV	－	0	50	nA	INV1～8, NON6=3.0V
INV threshold 1	VINV1	0.79	0.80	0.81	V	CH1～5
INV threshold 2	VINV2	0.99	1.00	1.01	V	CH7,8V
INV threshold 3 (max)	VINV3	370	400	430	mV	CH8I
【For Inverting Base Bias Voltage Vref】						
CH6 Output Voltage	VOUT6	-6.09	-6.00	-5.91	V	NON5 12kΩ, 72kΩ (※2)
Line Regulation	DVLi	－	4.0	12.5	mV	VCCOUT=2.8～5.5V
Output Current When Shorted	Ios	0.2	1.0	－	mA	Vref=0V
【Soft Start】						
CH2,5 Soft Start Time	Tss2,5	3.4	4.4	5.4	msec	
CH3,4 Soft Start Time	Tss3,4	1.2	2.2	3.2	msec	
CH6 Soft Start Time	Tss6	3.4	4.4	5.4	msec	
CH7,8 Soft Start Time	Tss7,8	4.4	5.4	6.6	msec	

Parameter	Symbol	Limit MIN	Limit TYP	Limit MAX	Unit	Conditions
【Output Driver】						
CH1 Highside SW ON Resistance	RON1p	－	120	270	mΩ	Hx1=5V
CH1 Lowside SW ON Resistance	RON1N	－	80	240	mΩ	VCCOUT=5.0V
CH2 Highside SW ON Resistance	RON21p	－	250	400	mΩ	Hx2=3V
CH2 Lowside SW ON Resistance	RON21N	－	250	400	mΩ	VCCOUT=5.0V
CH3 Highside SW ON Resistance	RON3p	－	250	400	mΩ	Hx3=3V, VCCOUT=5V
CH3 Lowside SW ON Resistance	RON3N	－	250	400	mΩ	VCCOUT=5.0V
CH4 Highside SW ON Resistance	RON4p	－	250	400	mΩ	Hx4=3V, VCCOUT=5V
CH4 Lowside SW ON Resistance	RON4N	－	250	400	mΩ	VCCOUT=5.0V
CH5 Highside SW ON Resistance	RON5p	－	250	400	mΩ	Hx5=3V
CH5 Lowside SW ON Resistance	RON5N	－	150	300	mΩ	VCCOUT=5.0V
CH6 Driver Output voltage H	Vout6H	VCCOUT -1.5	VCCOUT -1.0	－	V	IOUT6=50mA ,NON6=0.2V
CH6 Driver Output voltage L	Vout6L	－	0.5	1.0	V	IOUT6=-50mA NON6=-0.2V
CH7,8 NMOS SW ON Resistance	RON7,8N	－	500	800	mΩ	VCCOUT=5.0V
CH7,8 Load SW ON Resistance	RON7,8p	－	200	350	mΩ	HS7,8H=3V, VCCOUT=5.0V
【STB13～7】						
STB Control voltage Active	VSTBH1	1.5	－	5.5	V	
STB Control voltage Not Active	VSTBL1	-0.3	－	0.3	V	
Pull down Resistance	RSTB1	250	400	700	kΩ	
【UPIC8】						
UPIC8 Control voltage Active	VUPIH	2.1	－	4.00	V	
UPIC8 Control voltage Not Active	VUPIL	0	－	0.40	V	
Pull down Resistance	RUPIC1	30	50	80	kΩ	
【Circuit Current】						
Stand-by Current VBAT terminal	ISTB1	－	－	5	μA	
Stand-by Current Hx terminal	ISTB2	－	－	5	μA	Step down
Stand-by Current Lx terminal	ISTB3	－	－	5	μA	Step up
Stand-by Current HS7,8H terminal	ISTB4	－	－	5	μA	
Circuit Current when start-up (VBAT current when voltage supplied for the terminal)	IST	－	150	450	μA	VBAT=1.5V
Circuit Current 1 (VBAT current when voltage supplied for the terminal)	Icc1	－	45	150	μA	VBAT=3.0V
Circuit Current 2 (VCCOUT current when voltage supplied for the terminal)	Icc2	－	5.0	9.7	mA	INV1～8=1.2V, NON6=-0.2V

(※1)The protective circuit start working when circuit is operated by 100% duty.
So it is possible to use only for transition time shorter than charge time for SCP.
(※2)Recommend resistor value over 20kΩ between VREF to NON6, because VREF current is under 100uA.
◎This product is not designed for normal operation with in a radioactive environment

○Block Diagram

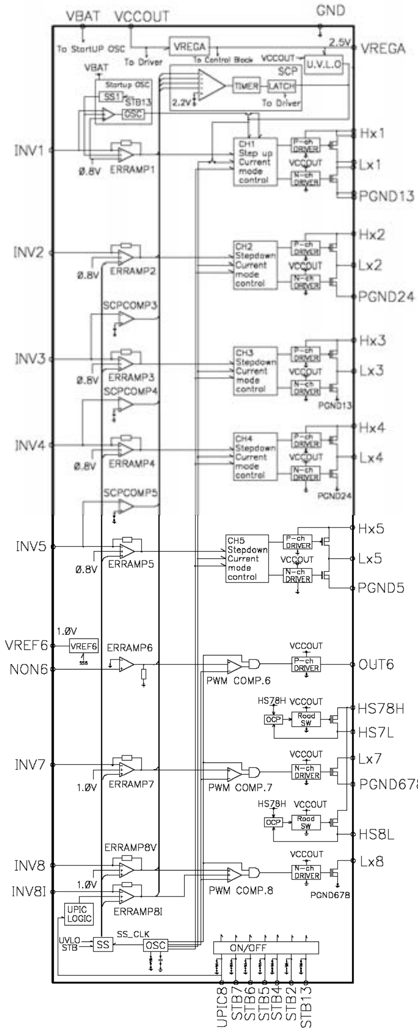

Fig.1

○Pin Description

端子名	機　　能
VBAT	Input for battery voltage
VCCOUT	Power Supply Input Terminal voltage (Input CH1 output voltage)
GND	Ground terminal
PGND13, 24, 5, 678	Ground terminal for internal FET
VREGA	VREGA Output
VREF6	CH6 base bias voltage
OUT6	Terminal for connecting gate of CH6 PMOS
Hx1,2,3,4,5	Input terminal for synchronous High side switch, Power supply for Pch Driver
Lx1,2,3,4,5,7,8	Terminal for connecting inductors
HS78H	Power supply for internal load switch
HS7L,HS8L	Output terminal for internal load switch
INV1,2,3,4,5,7,8	Error AMP inverted input
NON6	Error AMP non-inverted input
INV8I	Error AMP inverted input
STB13,2,4,5,6,7	ON/OFF switch H: operating over 1.5V
UPIC8	CH8 ON/OFF switch、 for CH8 brightness control

○Pin Assignment

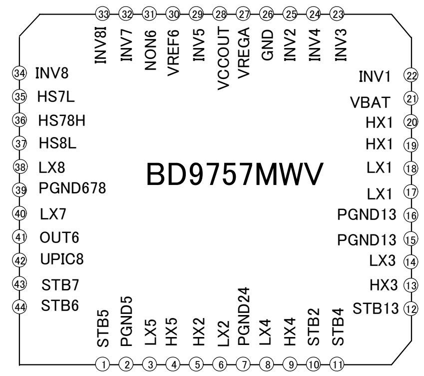

Fig.2

○Package

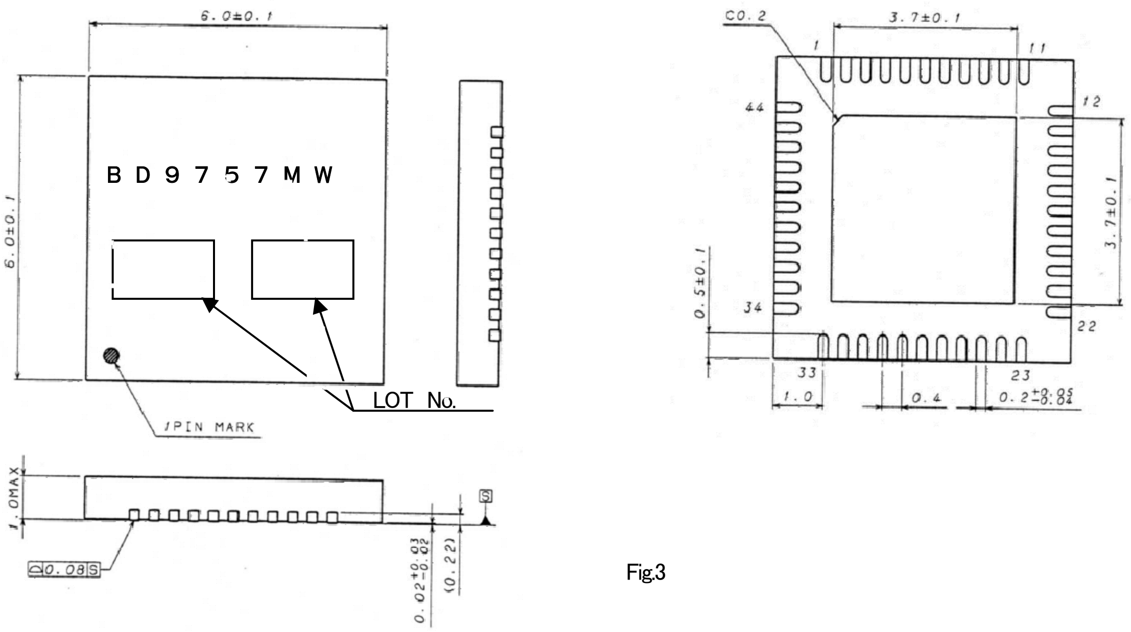

Fig.3

○Operation Notes

1.) Absolute maximum ratings
This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential
Make sure GND is connected at lowest potential. All pins except NON6, must not have voltage below GND. Also, NON6 pin must not have voltage below - 0.3V on start up.

3.) Setting of heat
Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting
Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field
Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance
Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Voltage of STB pin
The threshold voltages of STB pin are 0.3V and 1.5V. STB state is set below 0.3V while action state is set beyond 1.5V.
The region between 0.3V and 1.5V is not recommended and may cause improper operation.
The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01 μF.

8.) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.)Rush current at the time of power supply injection.
An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power Supply and GND pattern wiring.

10.)IC Terminal Input
This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed.
For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.9):
○When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.
Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements Induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

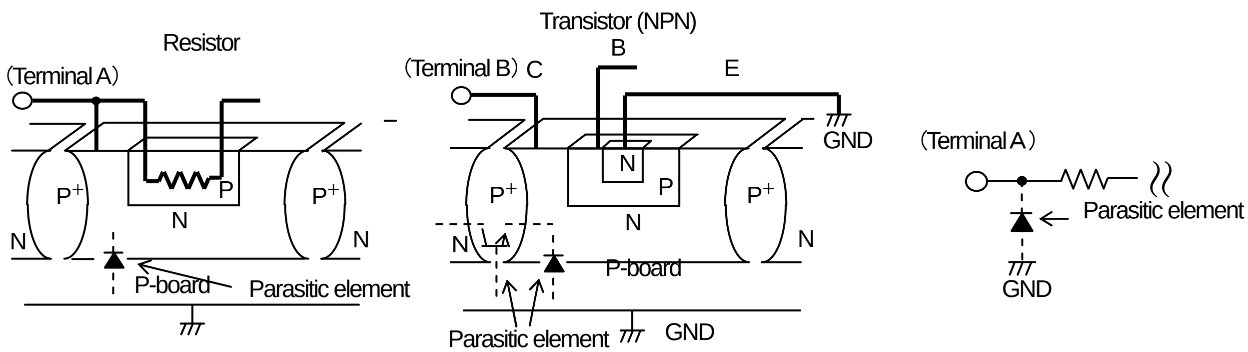

Fig – 9 Simplified structure of a Bipolar IC

Notes

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