Control integrated Power System (CIPOS™)

IKCS12F60AA
IKCS12F60AC

http://www.infineon.com/cipos

Power Management & Drives

Never stop thinking.

Revision History:	2009-04	Rev. 2.3
Previous Version:	2.2	
Page	Subjects (major changes since last revision)	
4	High temperature stress tests duration	
10	Changed $V_{IT,HYS}$	
14	Updated Zth-diagram of Diode	

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CIPOS™
Control integrated Power System

Single In-Line Intelligent Power Module

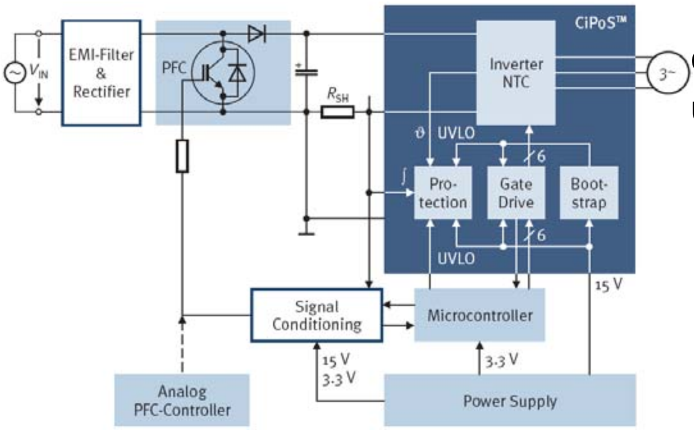
3Φ-bridge 600V / 12A @ 25°C

Features

- Fully isolated Single In-Line molded module
- TrenchStop® IGBTs with lowest $V_{CE(sat)}$
- Optimal adapted antiparallel diode for low EMI
- Integrated bootstrap diode and capacitor
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Temperature monitor and over temperature shutdown
- Overcurrent shutdown
- Undervoltage lockout at all channels
- Matched propagation delay for all channels
- Low side emitter pins accessible for all phase current monitoring (open emitter)
- Cross-conduction prevention
- Lead-free terminal plating; RoHS compliant
- Qualified according to JEDEC[1] (high temperature stress tests for 1000h) for target applications

Target Applications

- Washing machines
- Consumer Fans and Consumer Compressors



Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

This SIL-IPM is designed to control AC motors in variable speed drives for applications like air conditioning, compressors and washing machines. The package concept is specially adapted to power applications, which need extremely good thermal conduction and electrical isolation, but also EMI-save control and overload protection. The features of Infineon TrenchStop® IGBTs and antiparallel diodes are combined with a new optimized Infineon SOI gate driver for excellent electrical performance.

System Configuration

- 3 halfbridges with TrenchStop® IGBT & FW-EmCon™ diodes
- 3Φ SOI gate driver
- Bootstrap diodes for high side supply
- Integrated 100nF bootstrap capacitance
- Temperature sensor, passive components for adaptions
- Isolated heatsink
- Creepage distance typ. 3.2mm

Certification

UL 1577 (UL file E314539)

[1] J-STD-020 and JESD-022

Internal Electrical Schematic

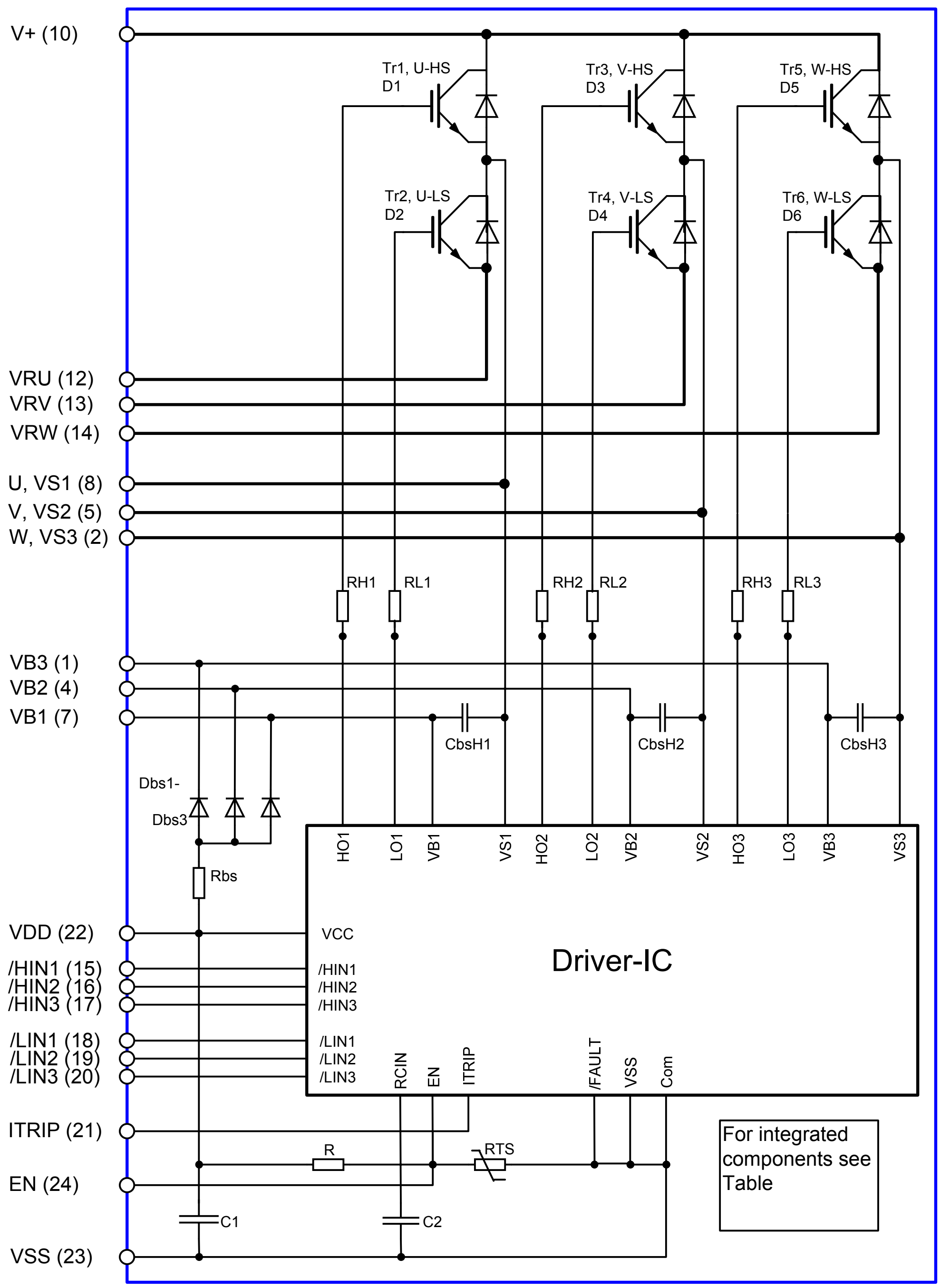


Figure 1: Internal Schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	VB3	high side floating IC supply voltage
2	W,VS3	motor output W, high side floating IC supply offset voltage
3	n.a.	None
4	VB2	high side floating IC supply voltage
5	V,VS2	motor output V, high side floating IC supply offset voltage
6	n.a.	None
7	VB1	high side floating IC supply voltage
8	U,VS1	motor output U, high side floating IC supply offset voltage
9	n.a.	None
10	V+	positive bus input voltage
11	n.a.	None
12	VRU	low side emitter
13	VRV	low side emitter
14	VRW	low side emitter
15	/HIN1	input gate driver high side 1/U
16	/HIN2	input gate driver high side 2/V
17	/HIN3	input gate driver high side 3/W
18	/LIN1	input gate driver low side 1/U
19	/LIN2	input gate driver low side 2/V
20	/LIN3	input gate driver low side 3/W
21	ITRIP	input overcurrent shutdown
22	VDD	module control supply
23	VSS	module negative supply
24	EN	input logic enable, output temperature monitoring

Pin Description

/HIN1,2,3 and /LIN1,2,3 (Low side and high side control pins, Pin 15 - 20)

These pins are active low and they are responsible for the control of the integrated IGBT The Schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-up resistor of about 75 kOhm is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

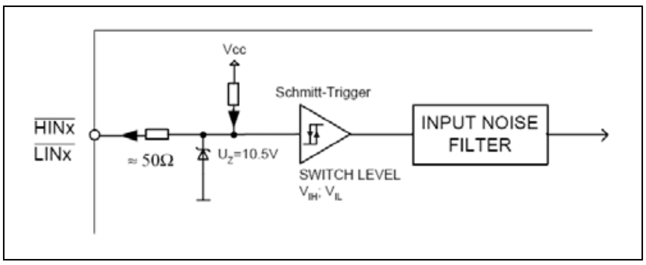


Figure 2: Input pin structure

It is recommended for proper work of CiPoS™ not to provide input pulse-width lower than 1us.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3).

A minimum deadtime insertion of typ 380ns is also provided, in order to reduce cross-conduction of the external power switches.

EN (enable, Pin 24)
The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. The internal structure of the pin is the same as Figure 2 made exception of the switching levels of the Schmitt-Trigger, which are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 1.3 V. The typical propagation delay time is t_{EN} = 900 ns.

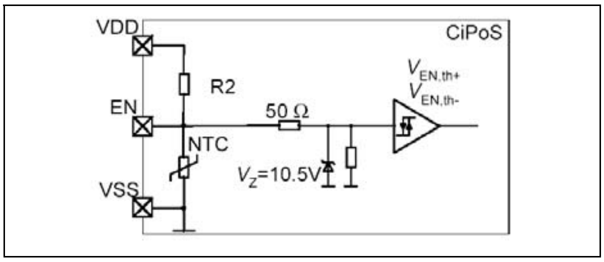


Figure 3: Internal Circuit at pin EN

This pin may also be used for reading out the temperature close to the gate drive IC. Please refer to section "Integrated Components" for the specification of the integrated parts.

ITRIP (Over-current detection function, Pin 21)
CiPoS™ provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.46V) is referenced to VSS ground. A input noise filter prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver after the shutdown propagation delay of typically 900ns.

The fault-clear time is set to typically to 4.7 ms.

VDD, VSS (control side supply and reference, Pin 22, 23)
VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.1 V is at least present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{DDUV-} = 10.4 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB1,2,3 and VS1,2,3 (High side supplies, Pin 1, 2, 4, 5, 7, 8)
VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit connected to VDD. This includes also integrated bootstrap capacitors of 100 nF at each floating supply, which are located very close to the gate drive circuit.

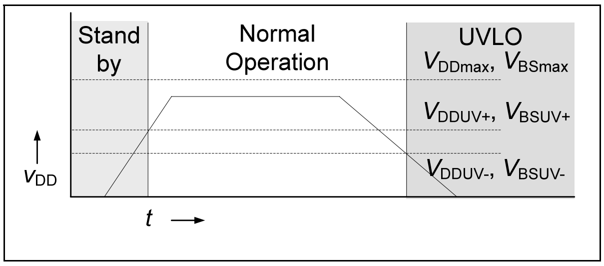


Figure 4: Input filter timing diagram

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 12.1 V and a falling threshold of V_{DDUV-} = 10.4 V according to Figure 4.

VS1,2,3 provide a high robustness against negative voltage in respect of VSS of -50 V. This ensures very stable designs even under rough conditions.

VRU, VRV, VRW (low side emitter, Pin 12, 13, 14)
The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

V+ (positive bus input voltage, Pin 10)
The high side IGBT are connected to the bus voltage. It is recommended, that the bus voltage does not exceed 500 V.

Absolute Maximum Ratings

(T_c = 25°C, if not stated otherwise)

Module Section

Description	Condition	Symbol	Value		Unit
			Min	max	
Storage temperature range		T_{stg}	-40	125	°C
Operating temperature control PCB[1]		T_{PCB}	-	125	°C
Solder temperature	Wave soldering, 1.6mm (0.063in.) from case for 10s	T_{sol}	-	260	°C
Insulation test voltage	RMS, f=50Hz, t =1min	V_{ISOL}	2500	-	V
Mounting torque	M3 screw and washer	M_S	-	0.6	Nm
Mounting pressure on surface	Package flat on mounting surface	N_{MC}	-	150	N/mm²
Creepage distance		d_S	3.1	-	mm
External bootstrap capacitor	single capacitor charging, VDD = 15V	$C_{bs,ext}$		19	µF

IGBT and Diode Section

Description	Condition	Symbol	Value		Unit
			min	max	
Max. blocking voltage	V_{IN}=5V, I_C=0.25mA	V_{CES}	600	-	V
DC output current	T_c = 25°C, T_{vJ} < 150°C T_c = 80°C, T_{vJ} < 150°C	I_u, I_v, I_w	-12 -6	12 6	A
Repetitive peak collector current	t_p limited by T_{vJmax}	I_u, I_v, I_w	-18	18	A
Short circuit withstand time[2] (SCSOA)	V_{DD} = 15V, V_{DC} ≤ 400V, T_j ≤ 150°C	t_{sc}	-	5	µs
IGBT reverse bias safe operating area (RBSOA)	V_{DD} = 15V, V_{DC} ≤ 500V, T_j = 150°C, I_C = 6A, V_{CEmax} = 600V		Full Square		
Power dissipation per IGBT	T_c = 25°C	P_{tot}	-	35	W
Operating junction temperature range	IGBT Diode	T_{vjI} T_{vjD}	-40 -40	150 150	°C

[1] Monitored by pin 24
[2] Allowed number of short circuits: <1000; time between short circuits: >1s.

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Single IGBT thermal resistance, junction-case		R_{thJC}	-	-	3.0	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	-	4.2	

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
High side floating supply voltage (VB vs. VS)		V_{BS}	-1	20	V
High side floating IC supply offset voltage	 t_p < 500ns	$V_{S1,2,3}$	VDD-VBS-6 VDD-VBS-50	600	V
Input voltage	LIN, HIN, EN, ITRIP	V_{in}	-1	10	V
Operating junction temperature[1]		$T_{J,IC}$	-	125	°C
Max. switching frequency		f_{PWM}	-	20	kHz

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -Potential unless otherwise specified.

Description	Symbol	Value		Unit
		min	max	
High side floating supply offset voltage	V_S	-3	500	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	12.5	17.5	
Low side power supply	V_{DD}	12.5	17.5	
Logic input voltages LIN,HIN,EN,ITRIP	V_{IN}	0	5	

[1] Monitored by pin 24

Static Parameters

(T_c = 25°C, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter blocking voltage	V_{IN} = 5V, I_C = 0.25mA	$V_{(BR)CES}$	600	-	-	V
Collector-Emitter saturation voltage	V_{DD} = 15V, I_{out} = +/- 6A 25°C 150°C	$V_{CE(sat)}$	 - -	 1.6 1.9	 2.1 -	
Diode forward voltage	V_{IN} =5V, I_{out} = +/- 6A 25°C 150°C	V_F	 - -	 1.65 1.6	 2.05 -	
Zero gate voltage collector current of IGBT	V_{CE} = 600V, V_{IN} = 5V T_j = 25°C T_j = 150°C	I_{CES}	 - -	 - -	 40 1000	µA
Short circuit collector current[1]	V_{DD} = 15V, $t_{SC} \leq$ 5µs V_{DC} = 400V, T_{vJ} = 150°C	$I_{C(SC)}$ [2]	-	40	-	A
Logic "0" input voltage (LIN,HIN)		V_{IH}	1.7	2.1	2.4	V
Logic "1" input voltage (LIN,HIN)		V_{IL}	0.7	0.9	1.1	V
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3	V
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5	V
ITRIP positive going threshold		$V_{IT,TH+}$	360	460	540	mV
ITRIP input hysteresis		$V_{IT,HYS}$	45	75	-	mV
V_{DD} and V_{BS} supply undervoltage positive going threshold		V_{DDUV+}, V_{BSUV+} [2]	11.0	12.1	12.8	V
V_{DD} and V_{BS} supply undervoltage negative going threshold		V_{DDUV-}, V_{BSUV-} [2]	9.5	10.4	11.0	V
V_{CC} and V_{BS} supply undervoltage lockout hysteresis		V_{DDUVH}, V_{BSUVH} [2]	1.2	1.7	-	V
Input clamp voltage (/HIN, /LIN, EN, ITRIP)	I_{IN} = 4 mA	$V_{INCLAMP}$	9.0	10.1	13.0	V
Quiescent VB_x supply current (VB_x only)	V_{HIN} = low	I_{QB}	-	360	550	µA
Quiescent *VDD* supply current (VDD only)	V_{IN} = float	I_{QDD}	-	2.0	3.0	mA
Input bias current	V_{IN} = 5V	I_{IN+}	-	55	100	µA
Input bias current	V_{IN} = 0V	I_{IN-}	-	110	200	µA
ITRIP Input bias current	V_{ITRIP} = 5V	I_{ITRIP+}	-	75	120	µA
EN Input bias current	V_{EN} = 5V	I_{EN+}	-	180	300	µA
Leakage current of high side	$T_{j,IC}$ = 125°C, VS = 600V	I_{LVS} [2]	-	30	-	µA

[1] Allowed number of short circuits: <1000; time between short circuits: >1s.

[2] Test is not subject of product test, verified by characterisation

Dynamic Parameters

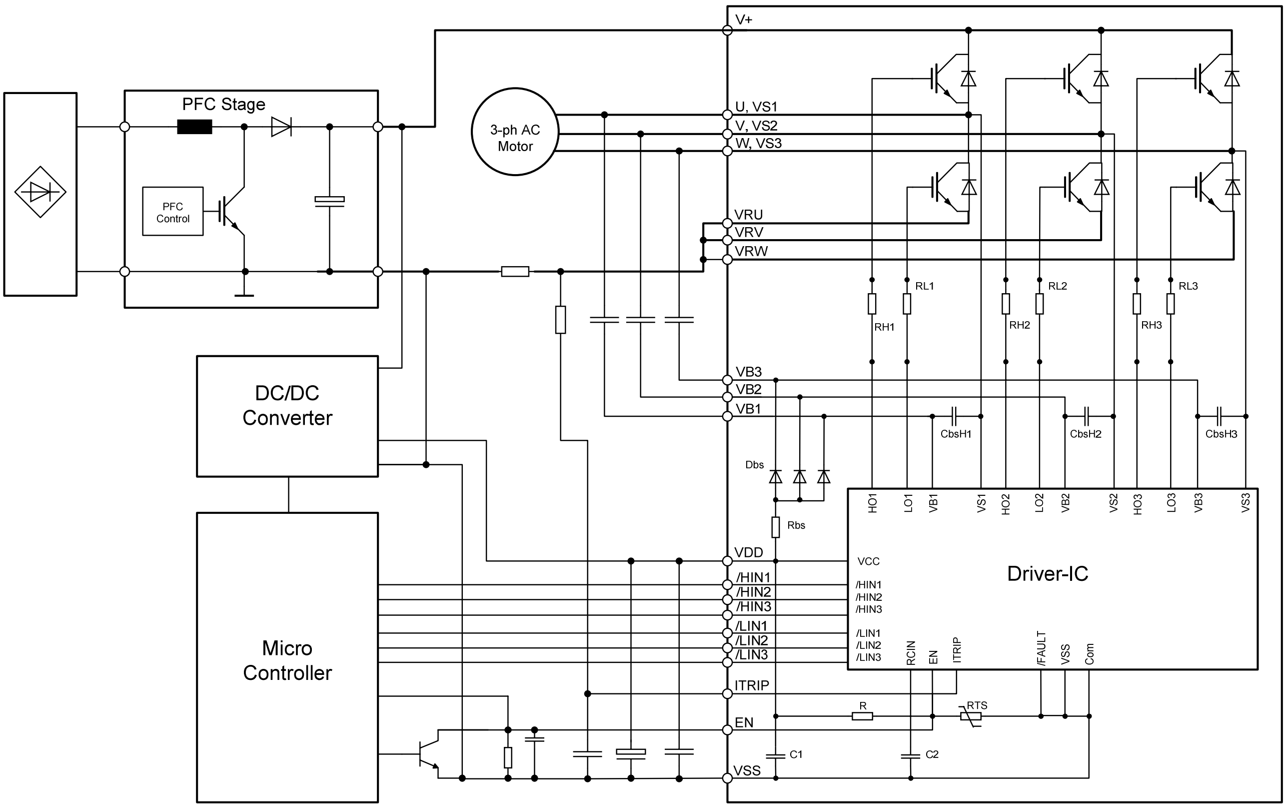
(T_c = 25°C, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay High side or low side	$V_{LIN,HIN}$ = 0V; I_{out} = 6A, V_{DC} = 300V	$t_{d(on)}$	-	617	-	ns
Turn-on rise time High side or low side	I_{out} = 6A, V_{DC} = 300V $V_{LIN,HIN}$ = 5V	t_r	-	21	-	ns
Turn-off propagation delay High side or low side	$V_{LIN,HIN}$ = 5V; I_{out} = 6A, V_{DC} = 300V	$t_{d(off)}$	-	832	-	ns
Turn-off fall time High side or low side	I_{out} = 6A, V_{DC} = 300V $V_{LIN,HIN}$ = 0V	t_f	-	29	-	ns
Shutdown propagation delay ENABLE	V_{EN} = 0V, I_u, I_v, I_w = 6A	t_{EN}	-	900	-	ns
Shutdown propagation delay ITRIP	V_{ITRIP} = 1V, I_u, I_v, I_w = 6A	t_{ITRIP}	-	900	-	ns
Input filter time ITRIP	V_{ITRIP} = 1V	$t_{ITRIPmin}$	155	210	380	ns
Input filter time at LIN for turn on and off and input filter time at HIN for turn on only	$V_{LIN,HIN}$ = 0 V & 5V	t_{FILIN}	120	270	-	ns
Input filter time at HIN for turn off	V_{HIN} = 5V	t_{FILIN1}	-	220	-	ns
Input filter time at HIN for turn off	V_{HIN} = 5 V	t_{FILIN2}	-	400	-	ns
Input filter time EN		t_{FILEN}	300	430	-	ns
Fault clear time after ITRIP-fault	$V_{LIN,HIN}$ = 0 V & 5V V_{ITRIP} = 0 V	t_{FLTCLR}	-	4.7	-	ms
Min. deadtime between low side and high side		DT_{PWM}	-	1	-	µs
Deadtime of gate drive circuit		DT_{IC}	-	380	-	ns
IGBT Turn-on Energy (includes reverse recovery of diode)	I_{out} = 6A, V_{DC} = 300V T_{vj} = 25°C T_{vj} = 150°C	E_{on}	 - -	 145 195	 - -	µJ
IGBT Turn-off Energy	I_{out} = 6A, V_{DC} = 300V T_{vj} = 25°C T_{vj} = 150°C	E_{off}	 - -	 122 160	 - -	µJ
Diode recovery Energy	I_{out} = 6A, V_{DC} = 300V T_{vj} = 25°C T_{vj} = 150°C	E_{rec}	 - -	 31 81	 - -	µJ

Integrated Components

Description	Condition	Symbol[1]	Value			Unit
			min	typ	max	
Resistor (0.25 W)		Rbs	-	10	-	Ω
Resistor		R	-	24	-	kΩ
Resistor	T_{NTC} = 25°C	RTS	-	100	-	
B-Constant of NTC (Negative Temperature Coefficient)	T_{NTC} = 25°C	B25	-	4250	-	K
Bootstrap diode forward voltage	I_{FDbs} = 100mA	V_{FDbs}	-	1.9	2.05	V
Capacitor		C1	-	100	-	nF
Capacitor		C2	-	2.2	-	
Bootstrap Capacitor		$CbsH_x$	-	100	-	

Circuit of a Typical Application



[1] Symbols according to Figure 1

Characteristics

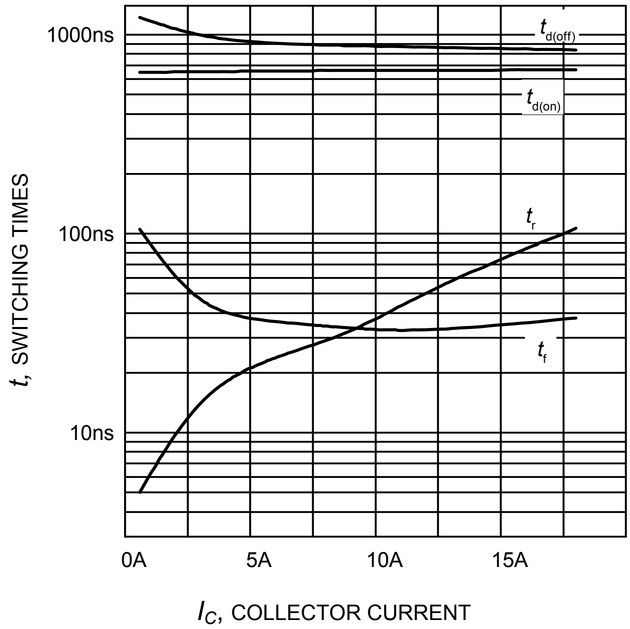


Figure 5. Typical switching times as a function of collector current
(inductive load, T_J=150°C,
V_{CE} = 300V, V_{DD} = 15V
Dynamic test circuit in Figure A)

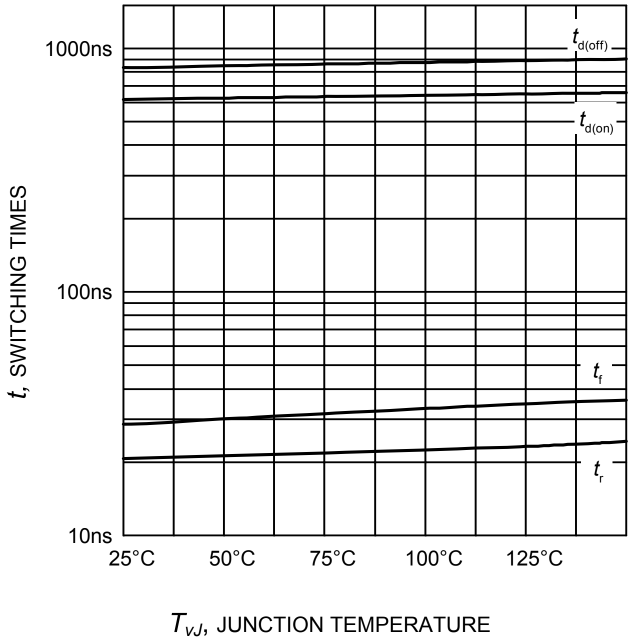


Figure 6. Typical switching times as a function of junction temperature
(inductive load, V_{DD}= 15V, V_{CE} = 300V, I_C = 6A
Dynamic test circuit in Figure A)

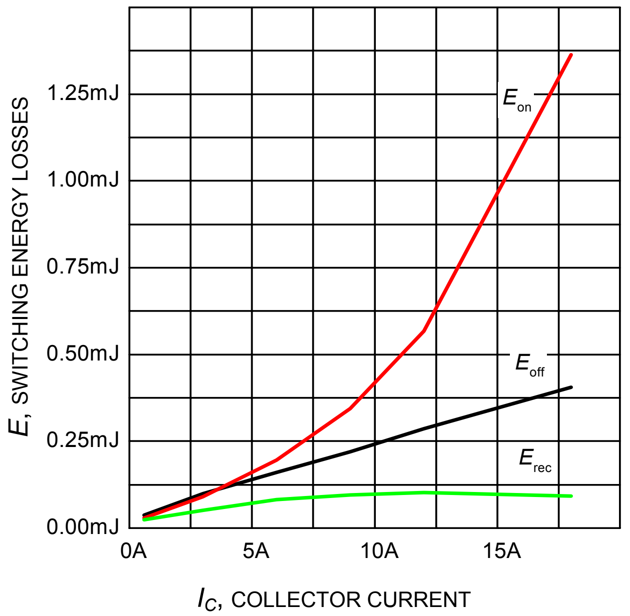


Figure 7. Typical switching energy losses as a function of collector current
(inductive load, T_J = 150°C,
V_{CE} = 300V, V_{DD} = 15V
Dynamic test circuit in Figure A)

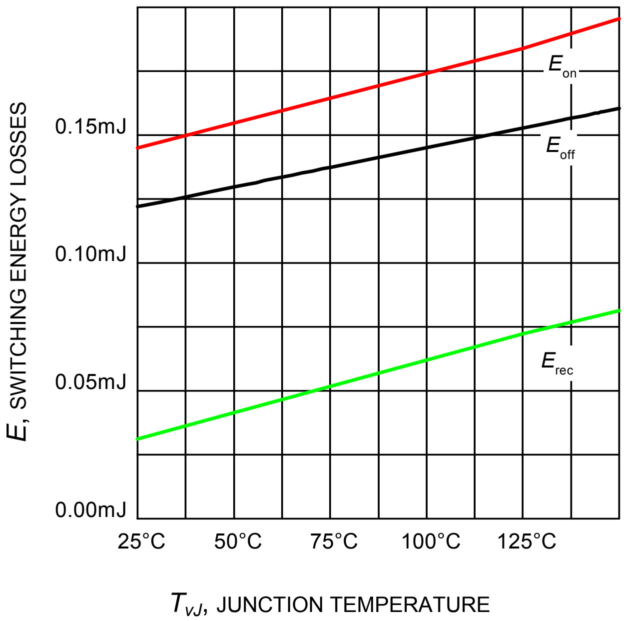


Figure 8. Typical switching energy losses as a function of junction temperature
(inductive load, V_{CE} = 300V,
V_{DD} = 15V, I_C = 6A
Dynamic test circuit in Figure A)

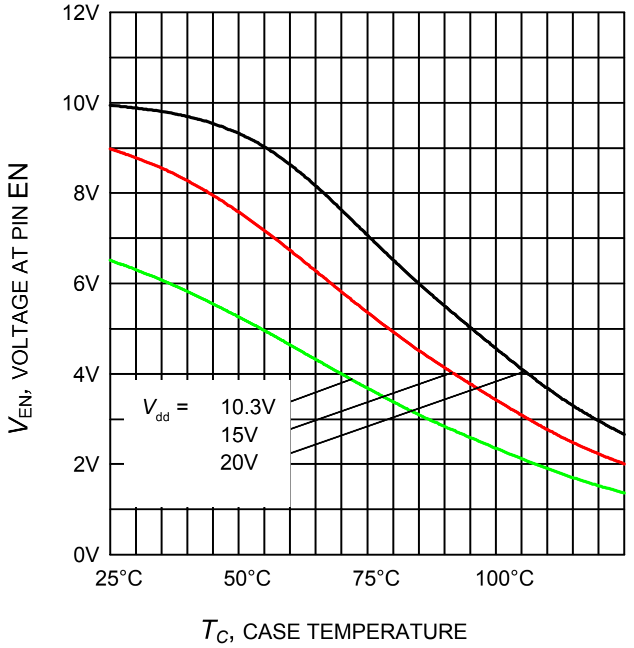


Figure 9. Typical voltage at pin EN as a function of case temperature

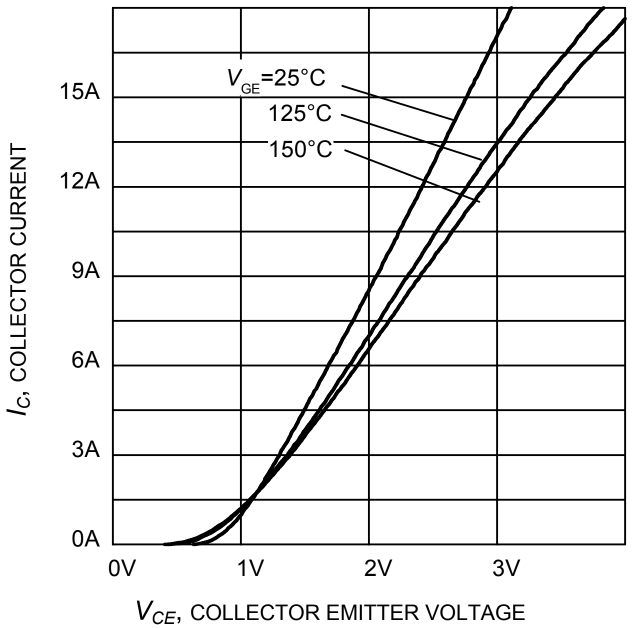


Figure 10. Typical output characteristic of IGBT as a function of collector emitter voltage (V_{DD} = 15V)

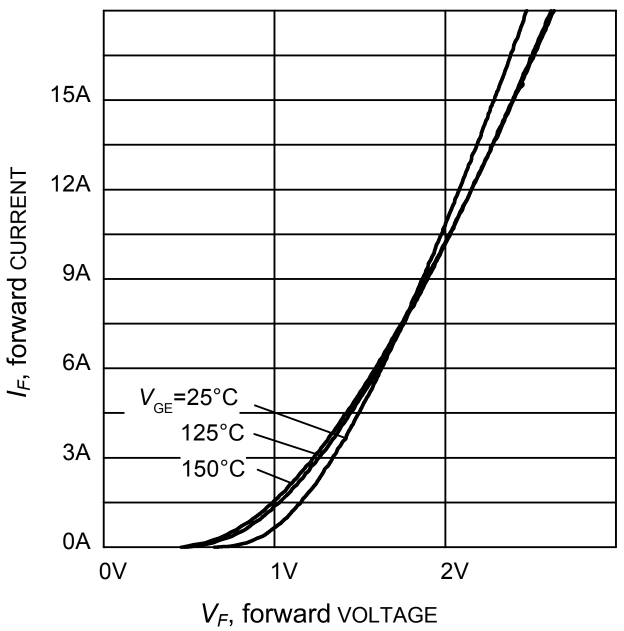


Figure 11. Typical diode forward current as a function of forward voltage

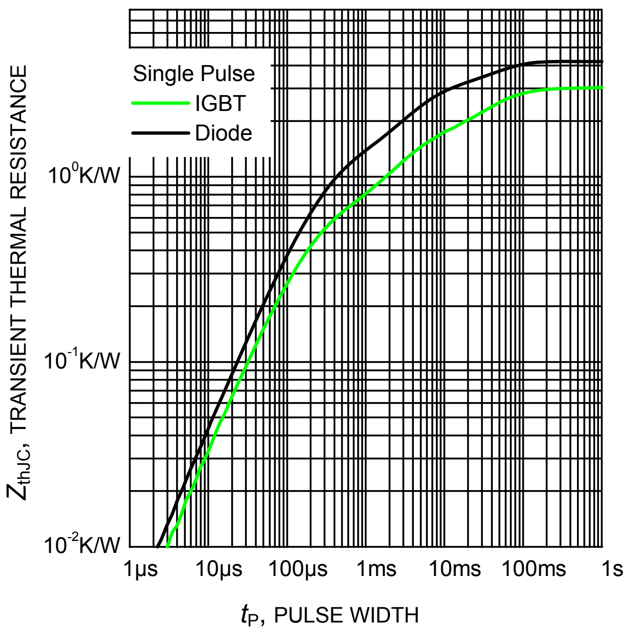


Figure 24. Transient thermal impedance as a function of pulse width
($D=t_P/T$)

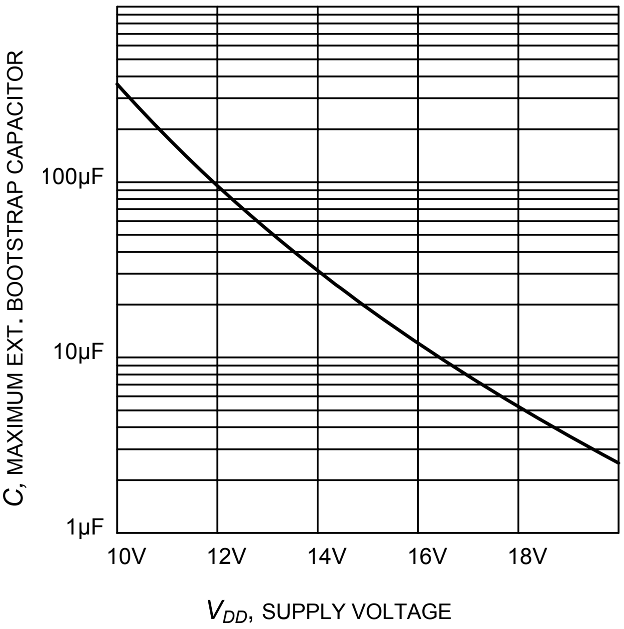


Figure 12. Maximum ext. bootstrap capacitor as a function of supply voltage V_{DD}
(T_J=25°C, single capacitor charging)

Test Circuits and Parameter Definition

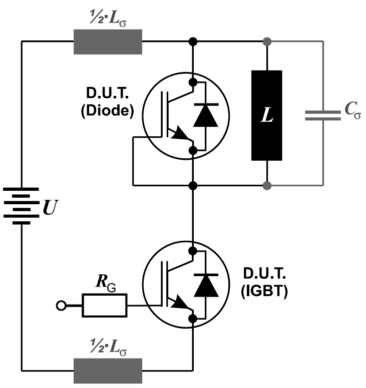


Figure A: Dynamic test circuit
Leakage inductance L_σ =180nH
Stray capacitance C_σ =39pF

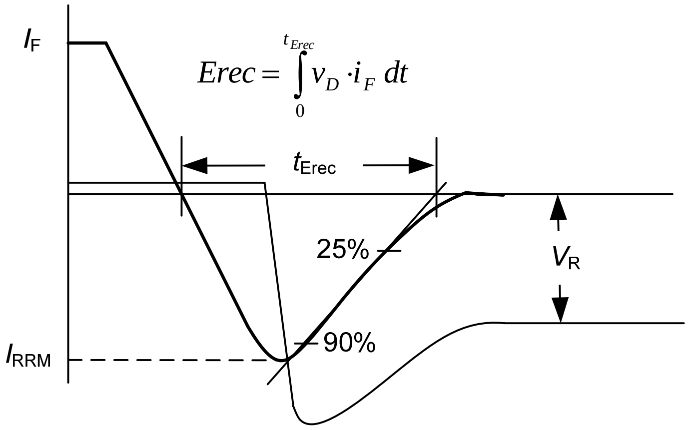


Figure B: Definition of diodes switching characteristics

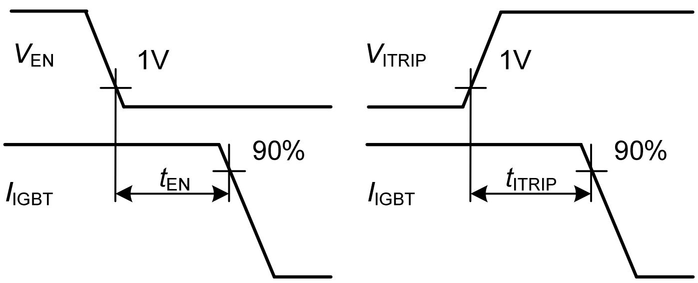


Figure C: Definition of Enable and ITRIP propagation delay

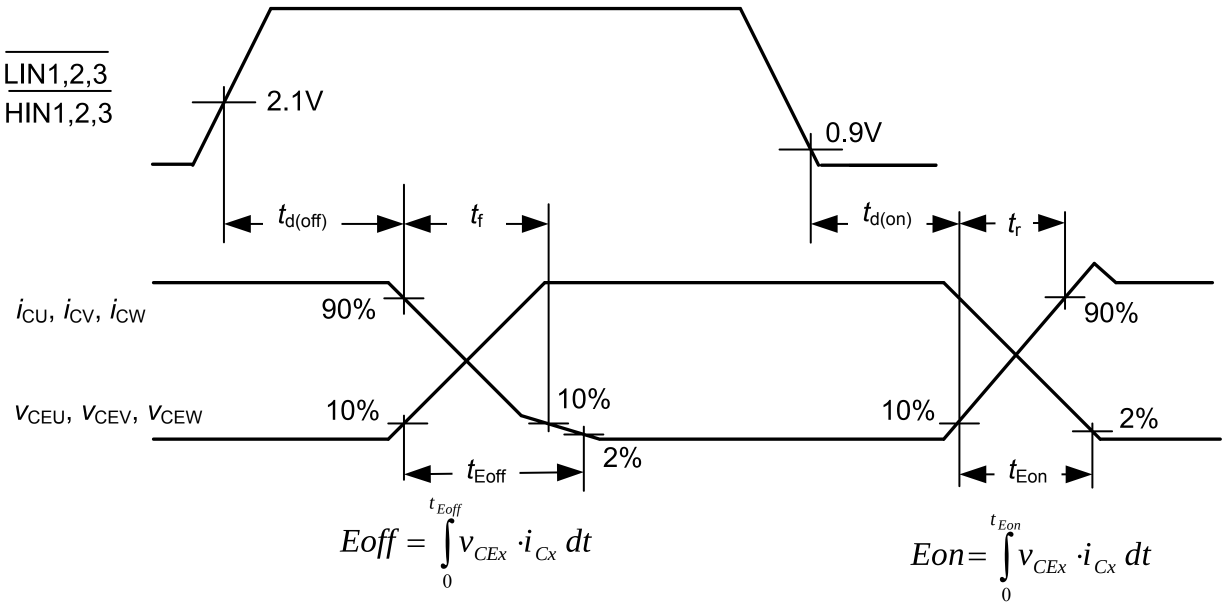


Figure D: Switching times definition and switching energy definition

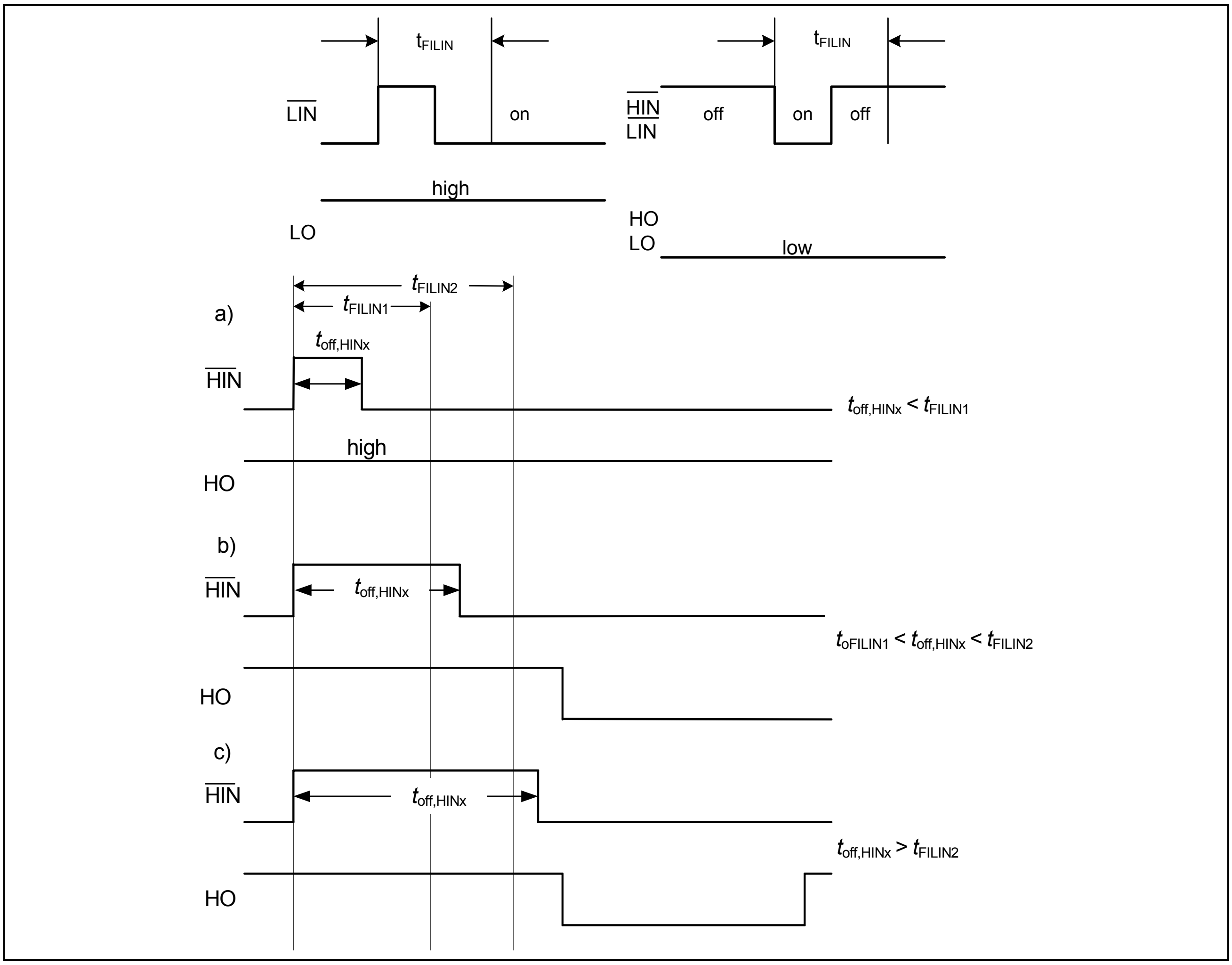
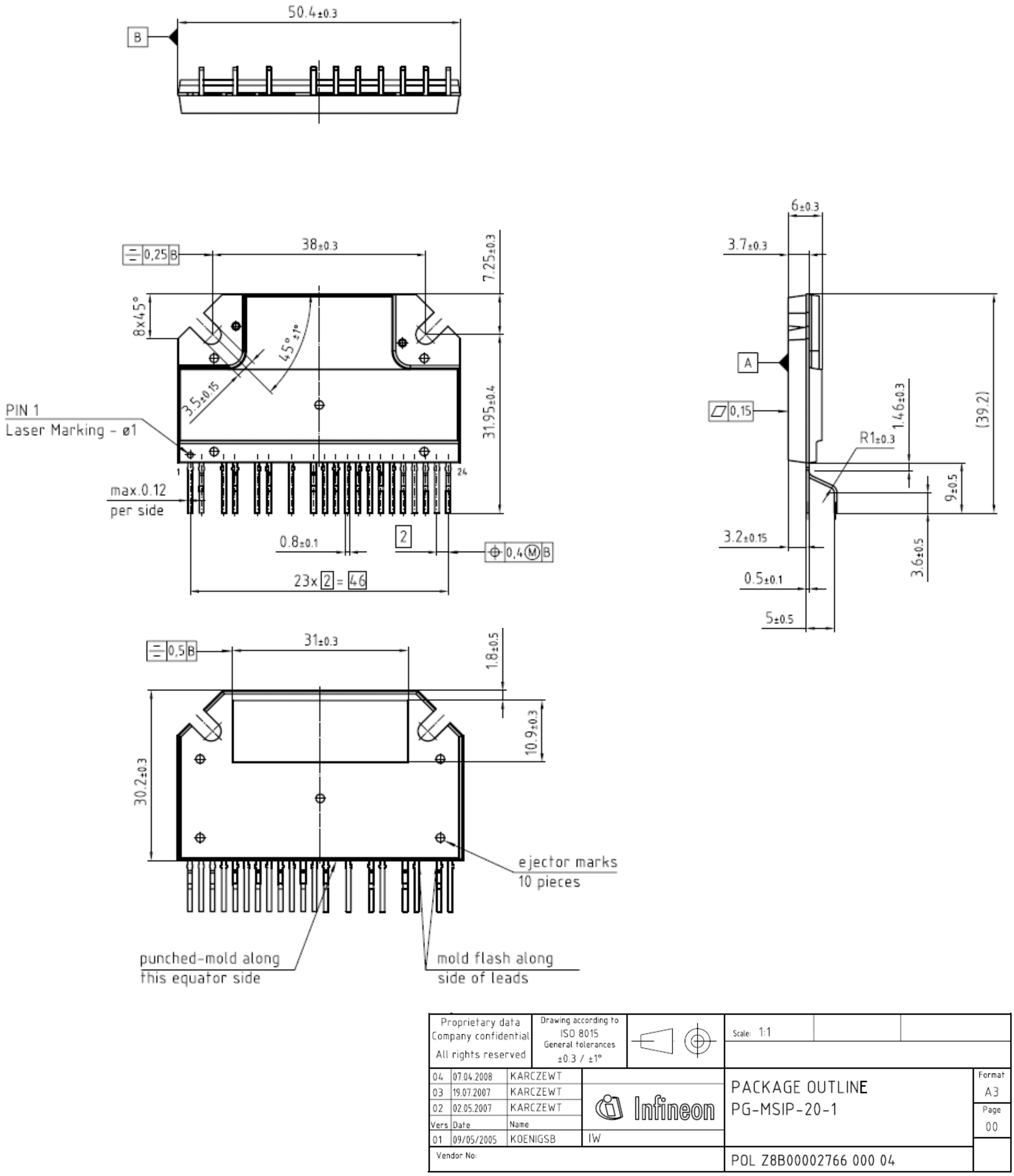


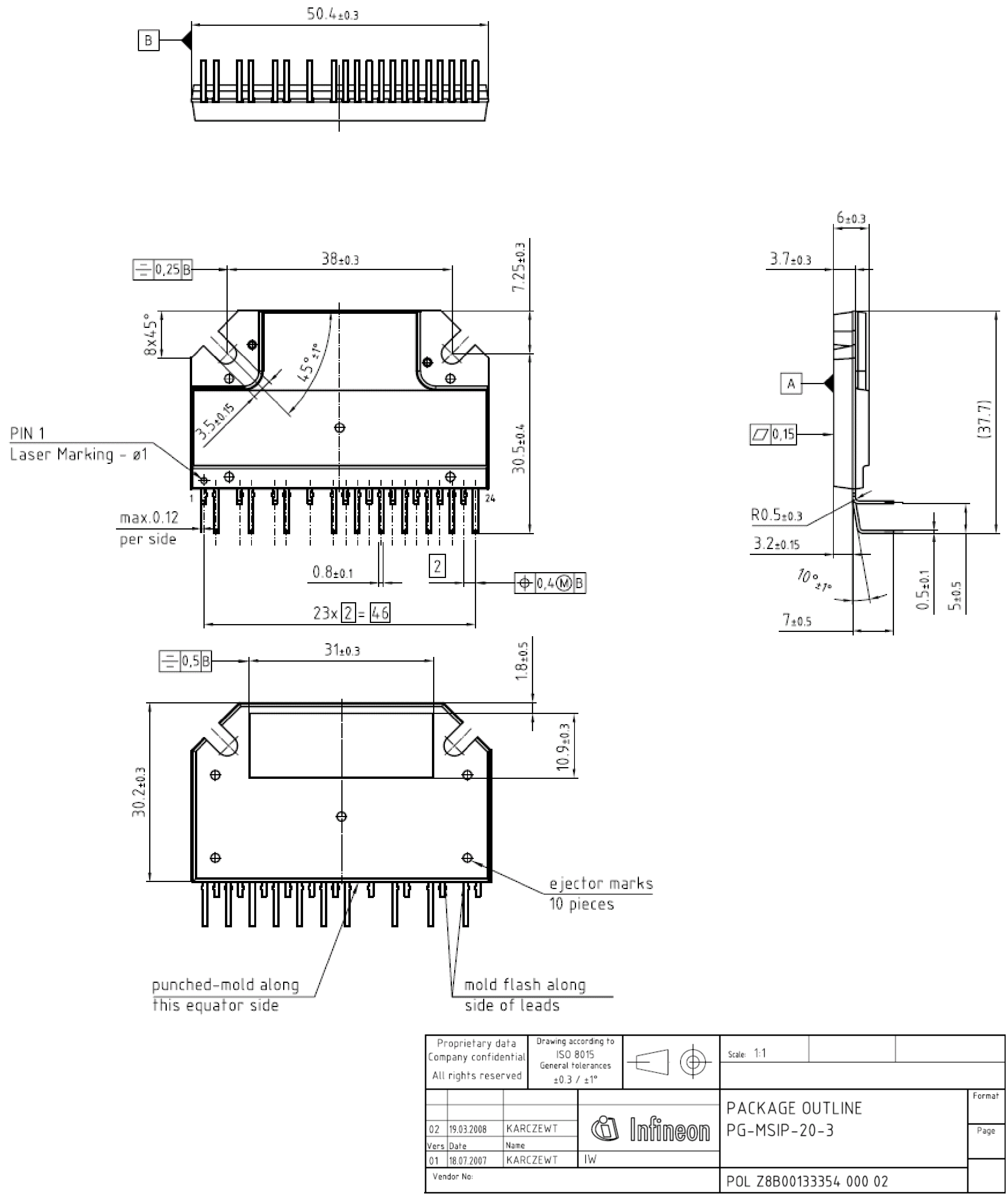
Figure E: Short Pulse suppression

Package Outline IKCS12F60AA



Note: There may occur discolourations on the copper surface without any effect on the thermal properties.

Package Outline IKCS12F60AC



Description	Condition	Symbol	Value			Unit
			min	typ	max	
Weight		m_P	-	17	-	g

Note: There may occur discolourations on the copper surface without any effect on the thermal properties.