

1 · General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of EPROM, and 176 bytes of static RAM.

The application areas of this MDT11P0122 range from appliance motor control and high speed automotive to low power remote transmitters/receivers and tele-communications processors, such as Remote controller, small instruments, toy, automobile and keyboard ... etc.

2 · Features

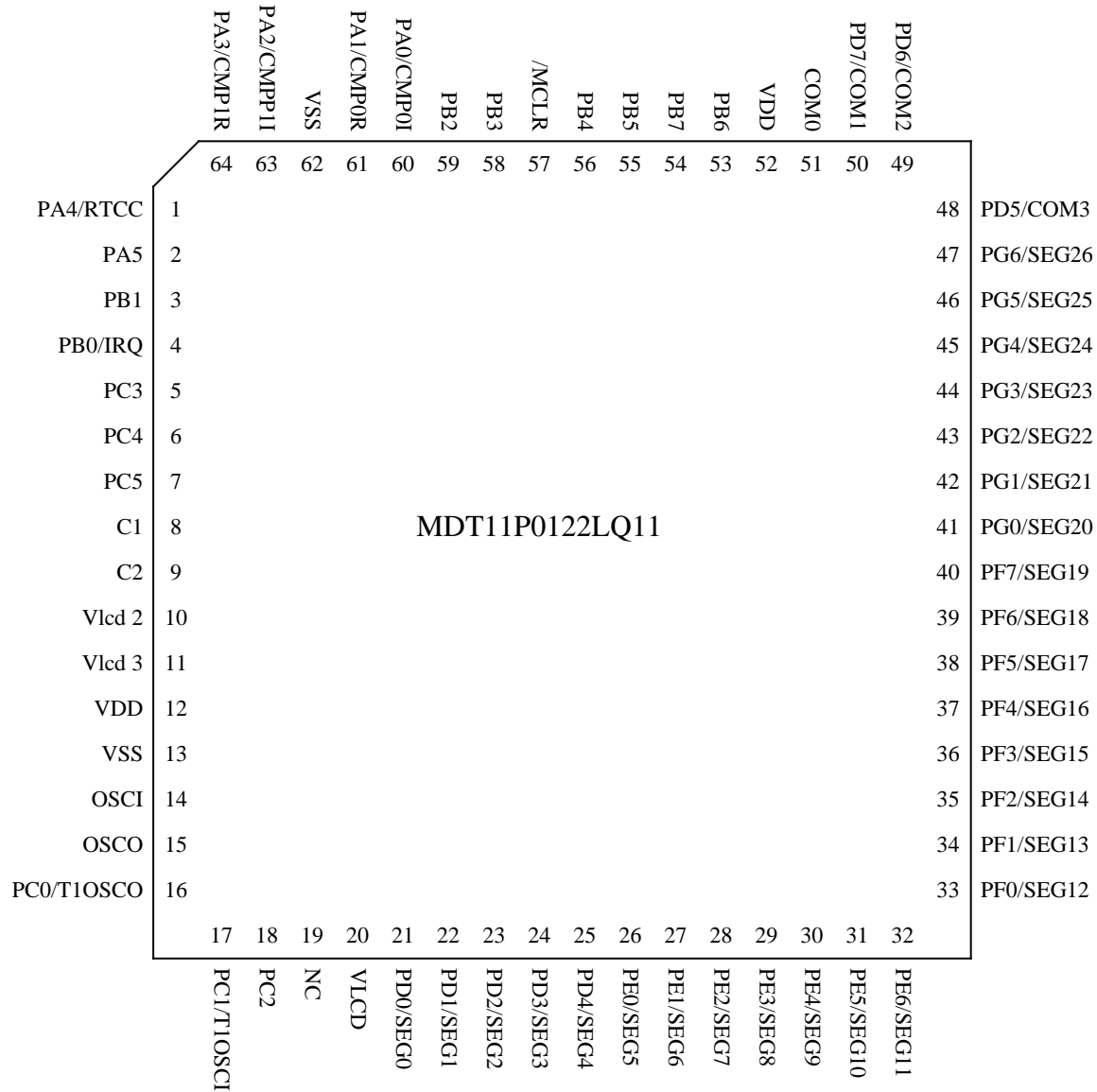
- ◆ RISC CPU
- ◆ Fully static design
- ◆ 37 single word instructions
- ◆ 4K x 14 program memory.
- ◆ 176 bytes RAM for data
- ◆ 25 bi-directional I/O
- ◆ Eight level hardware stacks
- ◆ Watchdog timer with on-chip RC oscillator.
- ◆ Interrupt capability
- ◆ Timer0 : 8-bit timer with 8-bit prescaler
- ◆ Timer1 : 16-bit timer
- ◆ 16-bit Timer1 compare register.
- ◆ Sleep mode for power saving.
- ◆ PB with port change wake-up interrupt.
- ◆ LCD : 29 Segments,4 commons.(27 x 4 at LQFP Package)
1/2,1/3,1/4 multiplex at 1/3,1/2 bias.

- ◆ 2 channel comparator

3. Applications

4. IC Diagram

(1)Pin Diagram



Device	LCD dot	Package	Remark
MDT11P0122LQ11	4 X 27	64 PIN LQFP	
MDT11P0122	4 X 29	COB	

(3)pad Coordinates

PAD-No	PAD Name	X	Y	PAD-No	PAD Name	X	Y
1	PA2	68.00	2278.00	34	PE6	1468.00	77.00
2	PA3	68.00	2178.00	35	PF0	1468.00	177.00
3	PA4	68.00	2078.00	36	PF1	1468.00	277.00
4	PA5	68.00	1978.00	37	PF2	1468.00	377.00
5	PB1	68.00	1878.00	38	PF3	1468.00	477.00
6	PB0	68.00	1778.00	39	PF4	1468.00	577.00
7	PC3	68.00	1678.00	40	PF5	1468.00	677.00
8	PC4	68.00	1578.00	41	PF6	1468.00	777.00
9	PC5	68.00	1478.00	42	PF7	1468.00	877.00
10	C1	68.00	1378.00	43	PG7	1468.00	977.00
11	C2	68.00	1278.00	44	PG0	1468.00	1077.00
12	VLCD2	68.00	1178.00	45	PG1	1468.00	1177.00
13	VLCD3	68.00	1078.00	46	PG2	1468.00	1277.00
14	VDD	68.00	978.00	47	PG3	1468.00	1377.00
15	VSS	68.00	878.00	48	PG4	1468.00	1477.00
16	OSC1	68.00	778.00	49	PG5	1468.00	1577.00
17	OSC2	68.00	678.00	50	PG6	1468.00	1677.00
18	PC0	68.00	578.00	51	PD5	1468.00	1777.00
19	PC1	68.00	478.00	52	PD6	1468.00	1877.00
20	PC2	68.00	378.00	53	PD7	1468.00	1977.00
21	VLCD	68.00	278.00	54	COM0	1468.00	2077.00
22	PD0	73.00	68.00	55	VDD	1357.80	2318.00
23	PD1	173.00	68.00	56	PB6	1257.80	2318.00
24	PD2	273.00	68.00	57	PB7	1157.80	2318.00
25	PD3	373.00	68.00	58	PB5	1057.80	2318.00
26	PD4	473.00	68.00	59	PB4	957.80	2318.00
27	PE7	573.00	68.00	60	MCLRB	831.80	2318.00
28	PE0	673.00	68.00	61	PB3	724.90	2318.00
29	PE1	773.00	68.00	62	PB2	624.90	2318.00
30	PE2	873.00	68.00	63	PA0	524.90	2318.00
31	PE3	973.00	68.00	64	PA1	424.90	2318.00
32	PE4	1073.00	68.00	65	VSS	324.90	2318.00
33	PE5	1173.00	68.00				

5. Pin function description

Pin name	Type	Buffer type	Description
OSC1	I		Oscillator input
OSC2	O		Oscillator out
/MCLR	I	ST	Reset input
PA0/CMP0I	I/O	TTL	Bi-directional I/O port A. Port A can be software programmed for internal 50K ohm pull-up PA0 ~PA3 can use TTL level I/O or Comaparator input. Output_Lo sink current only 14mA Can be clock input to Timer0.
PA1/CMP0R	I/O	TTL	
PA2/CMP1I	I/O	TTL	
PA3/CMP1R	I/O	TTL	
PA4/RTCC	I/O	ST	
PA5	I/O	TTL	
PB0/IRQ	I/O	ST/TTL	Bi-directional I/O port B. Port B can be software programmed for internal 50K ohm pull-up on all pins. PB0-PB7 can generate interrupt on pin state change. PB0/IRQ can be the external interrupt pin.
PB1	I/O	TTL	
PB2	I/O	TTL	
PB3	I/O	TTL	
PB4	I/O	TTL	
PB5	I/O	TTL	
PB6	I/O	TTL	
PB7	I/O	TTL	
PC0	I/O	ST	Bi-directional I/O port C. Port C can be software programmed for internal 100K pull-up on all pins. PC0 can be Timer1 oscillator output or Timer1 clock input. PC1 can be Timer1 oscillator input. PC2 can be Timer1 compare output.
PC1	I/O	ST	
PC2	I/O	ST	
PC3	I/O	ST	
PC4	I/O	ST	
PC5	I/O	ST	
PD0/SEG00	I/O/L	ST	Bi-directional I/O/LCD Driver port. PD0~PD4 are open drain I/O or LCD Segment driver
PD1/SEG01	I/O/L	ST	
PD2/SEG02	I/O/L	ST	
PD3/SEG03	I/O/L	ST	
PD4/SEG04	I/O/L	ST	

Pin name	Type	Buffer type	Description
PD5/COM3	I/L	ST	PD5~PD7 are digital input or LCD Common driver
PD6/COM2	I/L	ST	
PD7/COM1	I/L	ST	
PE0/SEG05	I/L	ST	Digital input or LCD Segment Driver port
PE1/SEG06	I/L	ST	
PE2/SEG07	I/L	ST	
PE3/SEG08	I/L	ST	
PE4/SEG09	I/L	ST	
PE5/SEG10	I/L	ST	
PE6/SEG11	I/L	ST	
PE7/SEG27	I/L	ST	
PF0/SEG12	I/L	ST	Digital input or LCD Segment Driver port
PF1/SEG13	I/L	ST	
PF2/SEG14	I/L	ST	
PF3/SEG15	I/L	ST	
PF4/SEG16	I/L	ST	
PF5/SEG17	I/L	ST	
PF6/SEG18	I/L	ST	
PF7/SEG19	I/L	ST	
PG0/SEG20	I/L	ST	Digital input or LCD Segment Driver port
PG1/SEG21	I/L	ST	
PG2/SEG22	I/L	ST	
PG3/SEG23	I/L	ST	
PG4/SEG24	I/L	ST	
PG5/SEG25	I/L	ST	
PG6/SEG26	I/L	ST	
PG7/SEG28	I/L	ST	
COM0	L	-	LCD Common 0
C1	-	-	LCD voltage charge pump pin 1
C2	-	-	LCD voltage charge pump pin 2
VLCD	-	-	LCD voltage input pin
VLCD2	-	-	LCD voltage pin(1/2VDD)
VLCD3	-	-	LCD voltage pin (3/2VDD)
VDD	-	-	Power input
Vss	-	-	Ground pin

**note : I:input O:output L:lcd

6. Memory Mapping

6.1 Program memory :

0000h	Reset Vector	
0001h		
0002h		
0003h		
0004h	Peripheral interrupt Vector	
0005h	Program memory (Page 0)	
07FFh		
0800h		Program memory (Page 1)
0FFFh		

6.2 Register file map

	BANK 0	BANK 1			BANK 2	BANK 3	
00h	I. ADDR	I. ADDR	80h	100h	I. ADDR	I. ADDR	180h
01h	RTCC	TMR	81h	101h	RTCC	TMR	181h
02h	PCL	PCL	82h	102h	PCL	PCL	182h
03h	STATUS	STATUS	83h	103h	STATUS	STATUS	183h
04h	MSR	MSR	84h	104h	MSR	MSR	184h
05h	Port A	COIO A	85h	105h			185h
06h	Port B	COIO B	86h	106h	Port B	COIO B	186h
07h	Port C	COIO C	87h	107h	Port F	COIO F	187h
08h	Port D	COIO D	88h	108h	Port G	COIO G	188h
09h	Port E	COIO E	89h	109h			189h
0Ah	PCHLAT	PCHLAT	8Ah	10Ah	PCHLAT	PCHLAT	18Ah
0Bh	INTS	INTS	8Bh	10Bh	INTS	INTS	18Bh
0Ch	PIFB1	PIEB1	8Ch	10Ch			18Ch
0Dh			8Dh	10Dh	LCDPFS		18Dh
0Eh	TMR1L	PSTA	8Eh	10Eh	LCDFS		18Eh
0Fh	TMR1H		8Fh	10Fh	LCDCTL		18Fh
10h	T1STA	CMPPH	90h	110h	LCD00		190h
11h			91h	111h	LCD01		191h
12h			92h	112h	LCD02		192h
13h			93h	113h	LCD03		193h
14h			94h	114h	LCD04		194h
15h	CCP1L		95h	115h	LCD05		195h
16h	CCP1H		96h	116h	LCD06		196h
17h	CCPCTL		97h	117h	LCD07		197h
18h			98h	118h	LCD08		198h
19h			99h	119h	LCD09		199h
1Ah			9Ah	11Ah	LCD10		19Ah
1Bh			9Bh	11Bh	LCD11		19Bh
1Ch			9Ch	11Ch	LCD12		19Ch
1Dh			9Dh	11Dh	LCD13		19Dh
1Eh			9Eh	11Eh	LCD14		19Eh
1Fh			9Fh	11Fh	LCD15		19Fh
20h	General Purpose Register	General Purpose Register	A0h	120h			1A0h
70h		Access	F0h	17Fh	Access	Access	1F0h
7Fh		70h~7Fh	FFh	17Fh	70h~7Fh	70h~7Fh	1FFh

 Unimplemented memory location.

• **BANK 1**

R00 IAR(Indirect addressing register)

R01 RTCC (Real Time Counter/Counter Register)
Timer0 register

R02 PCL (Program Counter Low Byte)
Low order 8 bits of the Program Counter (PC)

R03 STATUS (Status register)

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power loss Flag bit
4	TO	WDT TIME OUT bit
5	RBS0	Register page select bit 0 0 : 00/H --- 7F/H
6	RBS1	0 1 : 80/H --- FF/H 1 0 : 100/H --- 17F/H 1 1 : 180/H --- 1FF/H
7	RBS2	Register page select bit 0 : 00/H--- FF/H 1 : 100/H---1FF/H

R04H : MSR (Memory Select Register)
Indirect data memory address pointer.

R05H : Port A

PortA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	-	-	Always available					

PA0~PA5 : portA I/O register.

PA6~PA7 : always read as 0.

R06H : Port B

PortB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	Always available							

PB0~PB7 : Have pin change interrupt

R07H : Port C

PortC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	-	-	Always available					

PC0~PC5 : portA I/O register.

PC6~PC7 : always read as 0.

R08H : Port D

PortD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	Always available							

R09H : Port E

PortE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	Always available							

R0AH : PCHLAT(Program counter high byte.)

BIT 7~0	-	-	-	PCH4	PCH3	PCH2	PCH1	PCH0
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Bit0~4 : Hiht byte of PC.

Bit5~7 : always read as 0

R0BH : INTS(Interrupt control register.)

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag.
1	INTF	PB0/IRQ external interrupt flag bit.
2	TIF	Timer0 overflow interrupt flag bit.
3	RBIE	0 : disable PB change interrupt 1 : enable PB change interrupt
4	INTS	0 : disable INT interrupt 1 : enable INT interrupt
5	TIS	0 : disable TMR0 interrupt 1 : enable TMR0 interrupt
6	PEIE	0 : disable all peripheral interrupt 1 : enable all peripheral interrupt
7	GIS	0 : disable global interrupt 1 : enable global interrupt

R0CH : PIFB1(Peripheral interrupt flag register.)

BIT 7~0	LCDIF	-	-	-	-	-	-	TMR1IF
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Bit 0 : Timer1 overflow interrupt flag bit

Bit 7 : LCD interrupt flag bit

Bit1~6 : always read as 0

R0EH : TMR1L(Timer1 data register low byte.)

ROFH : TMR1H(Timer1 data register high byte.)

R10H : T1STA(Timer1 control register)

Bit	Symbol	Function
0	TMR1ON	0 : Stop TMR1 1 : Enable TMR1
1	TMR1CLK	0 : Internal clock (Fosc/4) 1 : External clock from pin PC0
2	$\overline{\text{T1SYNC}}$	TMR1CLK = 1 0 : Synchronize external clock 1 : Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	0 : TMR1 Oscillator is shut off 1 : TMR1 Oscillator is enable
4~5	T1CKPS1 ~ T1CKPS0	1 1 = 1 : 8 Prescale value 1 0 = 1 : 4 Prescale value 0 1 = 1 : 2 Prescale value 0 0 = 1 : 1 Prescale value
6~7	-	Unimplemented

R15H : CCP1L(Timer1 compare LSB)

R16H : CCP1H(Timer1 compare MSB)

R17H : CCPCTL

Bit	Symbol	Function
0	CCPM0	0 : COMPARE off 1 : COMPARE on
1~7	-	Unimplemented.

R20H~R7FH : General purpose register

• **BANK 1**

R81H : TMR(Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
0~2	PS0~2	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 0 1	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit 0 : RTCC 1 : Watchdog Timer		
4	TCE	RTCC signal edge : 0 : Increment on low-to-high transition on RTCC pin 1 : Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 : Internal instruction cycle clock 1 : Transition on RTCC pin		
6	IES	Interrupt edge select 0 : Interrupt on falling edge on PB0 1 : Interrupt on rising edge on PB0		
7	/PBPH	PORTB pull-hi 0 : PORTB pull-hi are enable 1 : PORTB pull-hi are disable		

R85H : CPIO A (Control Port I/O Mode Register)

- 0 : I/O pin in output mode;
- 1 : I/O pin in input mode.

R86H : CPIO B (Control Port I/O Mode Register)

- 0 : I/O pin in output mode;
- 1 : I/O pin in input mode.

R87H : CPIO C (Control Port I/O Mode Register)

- 0 : I/O pin in output mode;
- 1 : I/O pin in input mode.

R88H : CPIO D (Control Port I/O Mode Register)

- 0 : I/O pin in output mode;
- 1 : I/O pin in input mode.

R89H : CPIO E (Control Port I/O Mode Register)

- 0 : I/O pin in output mode;
- 1 : I/O pin in input mode.

R8CH : PIEB1

Bit	Symbol	Function
0	TMR1IE	TMR1 interrupt enable bit 0 : disable TMR1 interrupt 1 : enable TMR1 interrupt
1~6	-	Unimplemented.
7	LCDIE	LCD interrupt enable bit 0 : disable LCD interrupt 1 : enable LCD interrupt

R8EH : PSTA

Bit	Symbol	Function
0	-	Unimplemented.
1	PORB	0:Power on Reset occurred 1:No Power on Reset occurred
2~7	-	Unimplemented.

R90H:CMPPH

Bit	Symbol	Function
0	CMPS0	0:PA0,PA1 as TTL input 1:PA0,PA1 as Comparaotr input
1	CMPS1	0:PA2,PA3 as TTL input 1:PA2,PA3 as Comparaotr input
2~3	CMPRS0~1	1 1 = PA1,PA3 select extrenal vrefence voltage 1 0 = PA1,PA3 select 3/4 VDD as vrefence voltage 0 1 = PA1,PA3 select 1/2 VDD as vrefence voltage 0 0 = PA1,PA3 select 1/4 VDD as vrefence voltage
4	PAHR	0:Port A pull up enable 1:Port A pull up disable
5	PCHR	0:Port C pull up enable 1:Port C pull up disable
6~7	-	-

• **BANK2**

R107H : PortF

PortF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Always read available								

108H : PortG

PortG	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
Always read available								

R10DH : LCDPFS(Lcd pin function select)

Bit	Symbol	Function
0	DL00	0 : PD0~PD4 as digital input 1 : PD0~PD4 as LCD driver
1	DL05	0 : PE0~PE3 as digital input 1 : PE0~PE3 as LCD driver
2	DL09	0 : PE4~PE6 as digital input 1 : PE4~PE6 as LCD driver
3	DL12	0 : PF0~PF3 as digital input 1 : PF0~PF3 as LCD driver
4	DL16	0 : PF4~PF7 as digital input 1 : PF4~PF7 as LCD driver
5	DL20	0 : PG0~PG6 as digital input 1 : PG0~PG6 as LCD driver
6	DL27	0 : PG7,PE7 as digital input 1 : PG7,PE7 as LCD driver
7	DL29	0 : PD5~PD7 as digital input 1 : PD5,PD7 as LCD driver

R10EH : LCDFS(LCD frame frequency select)

BIT 7~0	-	-	-	-	FS3	FS2	FS1	FS0
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Common select	Frame frequency
1/2	$\text{Clock}/[128 * (\text{FS3}:\text{FS0}+1)]$
1/3	$\text{Clock}/[96 * (\text{FS3}:\text{FS0}+1)]$
1/4	$\text{Clock}/[128 * (\text{FS3}:\text{FS0}+1)]$

R10FH : LCDCTL(LCD control)

Bit	Symbol	Function
0~1	LCDS0~1	LCD Common select bits 0 0 : -- 0 1 : 1/2 (use COM 0,1) 1 0 : 1/3 (use COM 0,1,2) 1 1 : 1/4 (use COM 0,1,2,3)
2~3	CLKS0~1	Clock select 0 0 : sysclk/256 0 1 : Timer1 clk (must enable T1 osc) 1 X : internal RC
4	CRS	Cap mode and Resistor mode select 0 : Resistor mode 1 : Cap mode
5	BIASS	BIAS Select 0 : Use 1/2 bias mode 1 : Use 1/3 bias mode
6	SLPE	LCD enabled in Sleep mode 0 : LCD enable in sleep mode 1 : LCD disable in sleep mode
7	LCDE	LCD enable bit 0 : LCD disable 1 : LCD enable

R110H~R11FH : LCD00~LCD15(LCD data register 00~15)

Address	Symbol	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R110H	LCD00	SEG07 COM0	SEG06 COM0	SEG05 COM0	SEG04 COM0	SEG03 COM0	SEG02 COM0	SEG01 COM0	SEG00 COM0
R111H	LCD01	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG09 COM0	SEG08 COM0
R112H	LCD02	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0
R113H	LCD03	*SEG31 COM0	*SEG30 COM0	*SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
R114H	LCD04	SEG07 COM1	SEG06 COM1	SEG05 COM1	SEG04 COM1	SEG03 COM1	SEG02 COM1	SEG01 COM1	SEG00 COM1
R115H	LCD05	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG09 COM1	SEG08 COM1
R116H	LCD06	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1
R117H	LCD07	*SEG31 COM1	*SEG30 COM1	*SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
R118H	LCD08	SEG07 COM2	SEG06 COM2	SEG05 COM2	SEG04 COM2	SEG03 COM2	SEG02 COM2	SEG01 COM2	SEG00 COM2
R119H	LCD09	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG09 COM2	SEG08 COM2
R11AH	LCD10	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2
R11BH	LCD11	*SEG31 COM2	*SEG30 COM2	*SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
R11CH	LCD12	SEG07 COM3	SEG06 COM3	SEG05 COM3	SEG04 COM3	SEG03 COM3	SEG02 COM3	SEG01 COM3	SEG00 COM3
R11DH	LCD13	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG09 COM3	SEG08 COM3
R11EH	LCD14	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3
R11FH	LCD15	*SEG31 COM3	*SEG30 COM3	*SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3

* These bits don't display, but can used as general ram.

- BANK3**

R187H : CPIO F

R188H : CPIO G

7.Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--00 0000	--00 0000	--uu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	--xx xxxx	--uu uuuu	--uu uuuu
PORT D	08h	0000 0000	0000 0000	uuuu uuuu
PORT E	09h	0000 0000	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah	---- 0000	---- 0000	---- uuuu
INS	0Bh	0000 000x	0000 000u	uuuu uuuu
PIFB1	0Ch	---- ---x	---- ---u	---- ---u
TMR1L	0Eh	xxxx xxxx	uuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuu uuuu	uuuu uuuu
T1STA	10h	--00 0000	--00 0000	--uu uuuu
CCPR1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPCTL	17h	--1- ---0	--1- ---0	--u- ---u
MTR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	--11 1111	--11 1111	--uu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	--11 1111	--11 1111	--uu uuuu
CPIOD	88h	1111 1111	1111 1111	uuuu uuuu
CPIOE	89h	1111 1111	1111 1111	uuuu uuuu
PIEB1	8Ch	---- ---0	---- ---0	---- ---u
PWRCON	8Eh	---- #-	---- -u-	---- -u-
CMPPH	90h	0011 0000	0011 uuuu	00uu uuuu
PORT F	107h	0000 0000	0000 0000	uuuu uuuu
PORT G	108h	0000 0000	0000 0000	uuuu uuuu

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
LCDPFS	10Dh	1111 1111	1111 1111	uuuu uuuu
LCDFS	10Eh	---- 0000	---- 0000	---- uuuu
LCDCTL	10Fh	0000 0000	0000 0000	uuuu uuuu
Lcd00~15	110h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CPIO F	186h	1111 1111	1111 1111	uuuu uuuu
CPIO G	187h	1111 1111	1111 1111	uuuu uuuu

Note : u=unchanged , x=unknown , - =unimplemented , read as "0"

#=value depends on the condition of the following table

Condition	Status bit 4	Status bit 3	PWRCON bit 1
POWR ON RESET	1	1	0
/MCLR reset (not during SLEEP)	u	u	u
/MCLR reset during SLEEP	1	0	u
WDT reset (not during SLEEP)	0	1	u
WDT reset during SLEEP	0	0	u
Interrupt Wake-up during SLEEP	1	0	u

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMR register	W→TMR	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) (4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R - W→t (R+/W+1→t)	C, HC, Z

Instruction Code	Mnemonic Operands	Function	Operation	Status
011101 trrrrrr	DECR R, t	Decrement register	$R - 1 \rightarrow t$	Z
011110 trrrrrr	DECRSZ R, t	Decrement register, skip if zero	$R - 1 \rightarrow t$	None
010010 trrrrrr	ANDWR R, t	AND W and register	$R \cap W \rightarrow t$	Z
110100 iiiiii	ANDWI i	AND W and immediate	$i \cap W \rightarrow W$	Z
010011 trrrrrr	IORWR R, t	Inclu. OR W and register	$R \cup W \rightarrow t$	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	$i \cup W \rightarrow W$	Z
010100 trrrrrr	XORWR R, t	Exclu. OR W and register	$R \oplus W \rightarrow t$	Z
110110 iiiiii	XORWI i	Exclu. OR W and immediate	$i \oplus W \rightarrow W$	Z
011111 trrrrrr	COMR R, t	Complement register	$\neg R \rightarrow t$	Z
010110 trrrrrr	RRR R, t	Rotate right register	$R(n) \rightarrow R(n-1),$ $C \rightarrow R(7), R(0) \rightarrow C$	C
010101 trrrrrr	RLR R, t	Rotate left register	$R(n) \rightarrow r(n+1),$ $C \rightarrow R(0), R(7) \rightarrow C$	C
010000 1xxxxxxx	CLRW	Clear working register	$0 \rightarrow W$	Z
010001 0rrrrrr	CLRR R	Clear register	$0 \rightarrow R$	Z
0000bb brrrrrr	BCR R, b	Bit clear	$0 \rightarrow R(b)$	None
0010bb brrrrrr	BSR R, b	Bit set	$1 \rightarrow R(b)$	None
0001bb brrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if $R(b)=0$	None
0011bb brrrrrr	BTSS R, b	Bit Test, skip if set	Skip if $R(b)=1$	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	$n \rightarrow PC,$ $PC+1 \rightarrow Stack$	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	$n \rightarrow PC$	None
110001 iiiiii	RTIW i	Return, place immediate to W	$Stack \rightarrow PC, i \rightarrow W$	None
110111 iiiiii	ADDWI	Add immediate to W	$PC+1 \rightarrow PC,$ $W+i \rightarrow W$	C,HC,Z
111000 iiiiii	SUBWI	Subtract W from immediate	$i-W \rightarrow W$	C,HC,Z
010000 00001001	RTFI	Return from interrupt	$Stack \rightarrow PC, 1 \rightarrow GIS$	None
010000 00000100	RET	Return from subroutine	$Stack \rightarrow PC$	None

Note :

W	: Working register	b	: Bit position
WT	: Watchdog timer	t	: Target
TMODE	: TMODE mode register	0	: Working register
CPIO	: Control I/O port register (PA, PB, PC Only)	1	: General register
TF	: Timer overflow flag	R	: General register address
PF	: Power loss flag	C	: Carry flag
		HC	: Half carry

PC	: Program Counter	Z	: Zero flag
OSC	: Oscillator	/	: Complement
Inclu.	: Inclusive 'U'	x	: Don't care
Exclu.	: Exclusive '⊕'	i	: Immediate data (8 bits)
AND	: Logic AND '∩'	n	: Immediate address

9. Electrical Characteristics

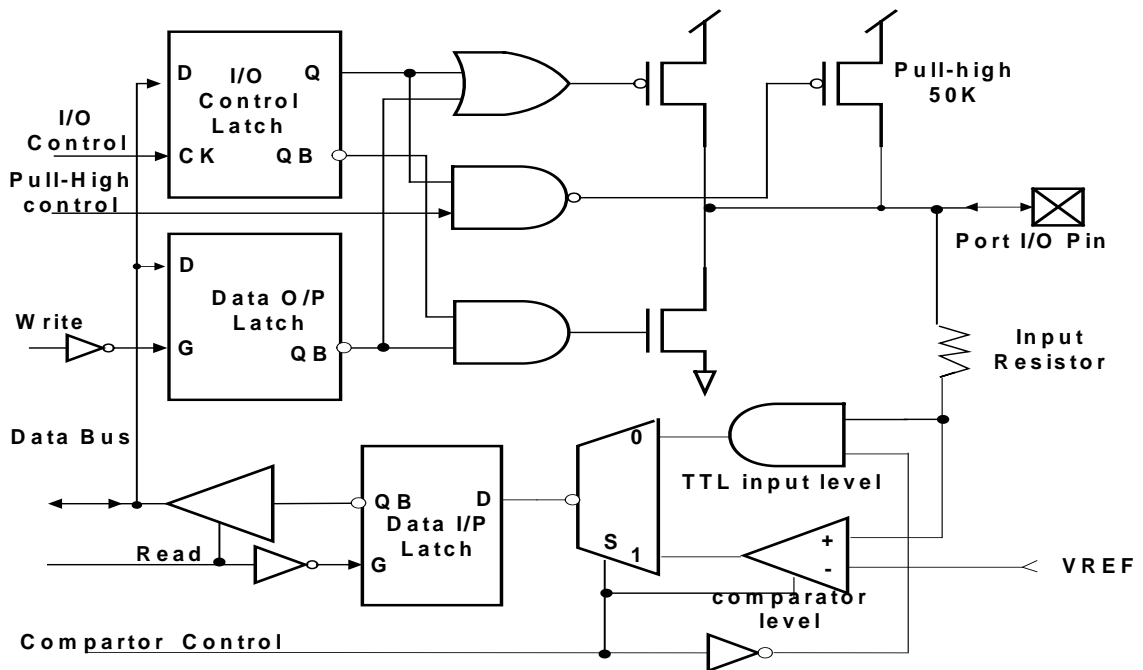
(Operating temperature at 25°C).

Sym	Description	Condition	Min	Typ	Max	Unit
VDD	Operating voltage		2.5		6.3	V
V _{IL}	Input Low Voltage	VDD=5V	-0.6		1.0	V
V _{IH}	Input high Voltage					
	PA, PB	VDD=5V	2.0		VDD	V
	PC, PD, PE, PF, PG RTCC, /MCLR	VDD=5V	3.2		VDD	V
I _{IL}	Input leakage current	VDD=5V			+/-1	μA
V _{OL}	Output Low Voltage	VDD=5V, I _{OL} =20mA		0.4		V
	PA, PB, PC, PD	VDD=5V, I _{OL} =5mA		0.1		V
V _{OH}	Output High Voltage	VDD=5V, I _{OH} = -20mA		3.3		V
	PA, PB, PC	VDD=5V, I _{OH} = -5mA		4.5		V
R _{ph}	PortA pullhigh resister	VDD=5V		50k		Ω
	PortB pullhigh resister	VDD=5V		50K		Ω
	PortC pullhigh resister	VDD=5V		100K		Ω
I _{slp}	Sleep current (WDT disable)	VDD = 2.3 ~ 6.3 V		0.1	1.0	μA
I _{slp}	Sleep current (WDT enable)	VDD = 2.3 V		2		μA
		VDD = 3.0 V		5		μA
		VDD = 4.0 V		10		μA
		VDD = 5.0 V		18		μA
		VDD = 6.3 V		35		μA
I _{slp-L}	Sleep current (LCD on at CAP MODE),no load	Vdd=5.0 V		15		μA
		Vdd=3.0 v		5.5		
	Sleep current (LCD on at RES MODE),no load	Vdd=5.0 V		20		μA
		Vdd=3.0 v		7		
V _{pr}	Power Edge-detector Reset Voltage		1.1		1.3	V

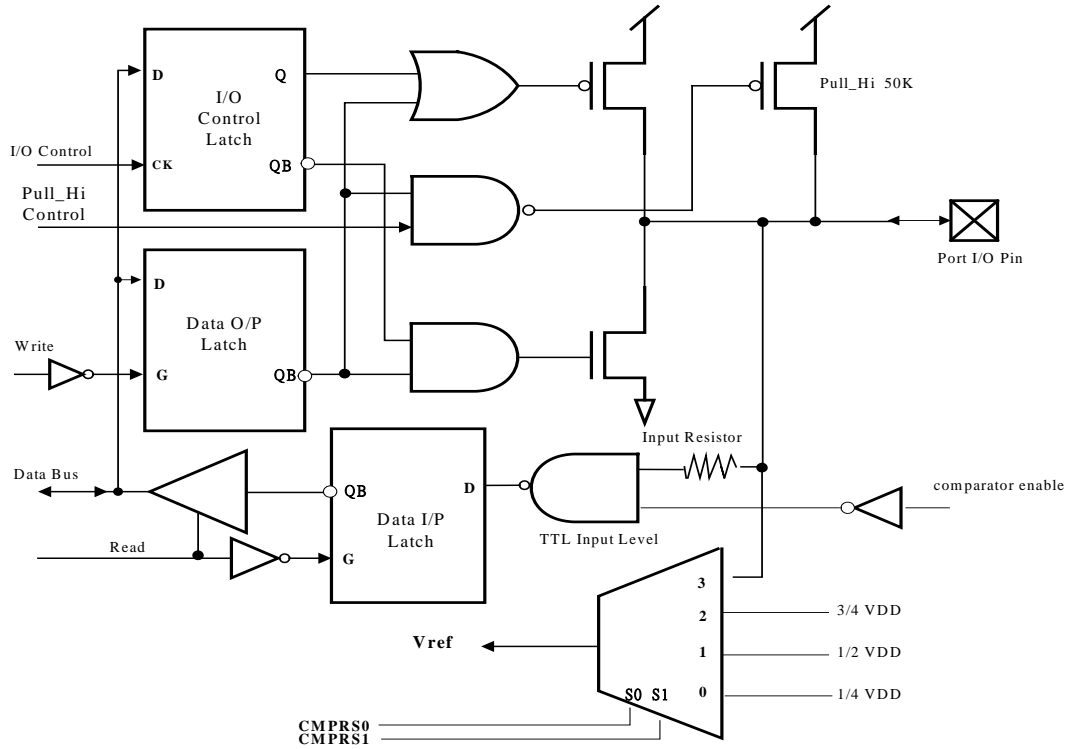
Sym	Description	Condition	Min	Typ	Max	Unit	
Twdt	The basic WDT time-out cycle time	VDD=2.3 V		26.4		mS	
		VDD=3.0 V		23.6		mS	
		VDD=4.0 V		20.1		mS	
		VDD=5.0 V		20.4		mS	
		VDD=6.3 V		16.4		mS	
T _{FLT}	/MCLR filter	VDD=5.0 V		600		nS	
Vref	Input reference voltage	VDD=2.5v ~6.3v			VDD	V	
---	Comparator Response time V-=VDD/4, V+=V- ± 0.2v V-=VDD/2, V+=V- ± 0.2v V-=VDD3/4, V+=V- ± 0.2v V-=VDD-0.8, V+=V± 0.2v	VDD=5.0v, V- = Vref V+ = (PA0~PA3)		8		μS	
				8		μS	
				8		μS	
				8		μS	
Lrc	Internal LCD RC	VDD=5v	15	-	35	kHz	
Ires	Internal LCD resistor current between vlcd pin and VDD	VDD=5v	1/3bias		10		μA
			1/2bias		30		
		VDD=3v	1/3bias		0.1		
			1/2bias		4		

10. Equivalent Circuit

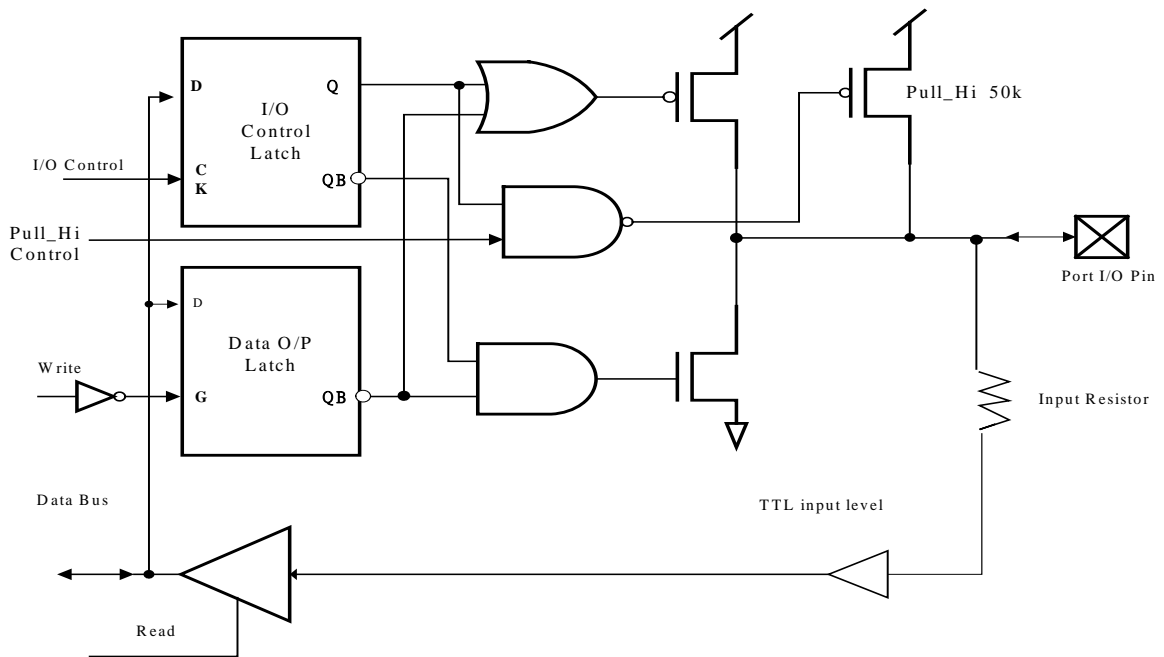
- Port A
PA0, PA2



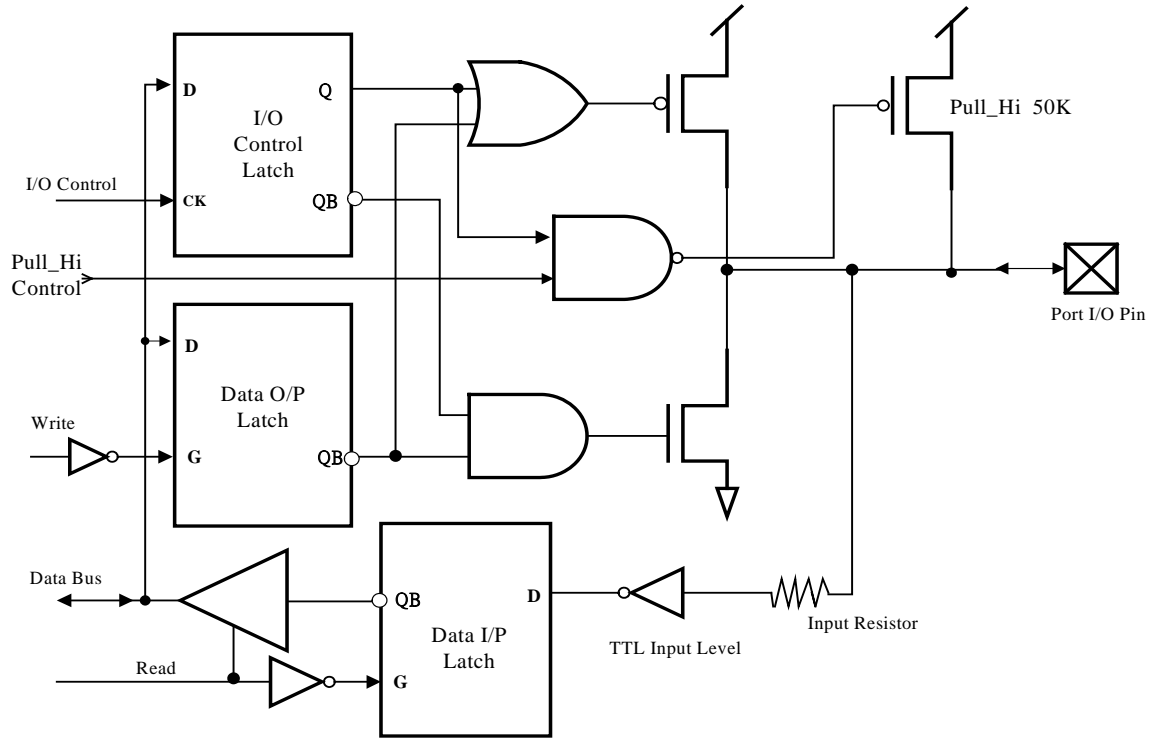
PA1,PA3



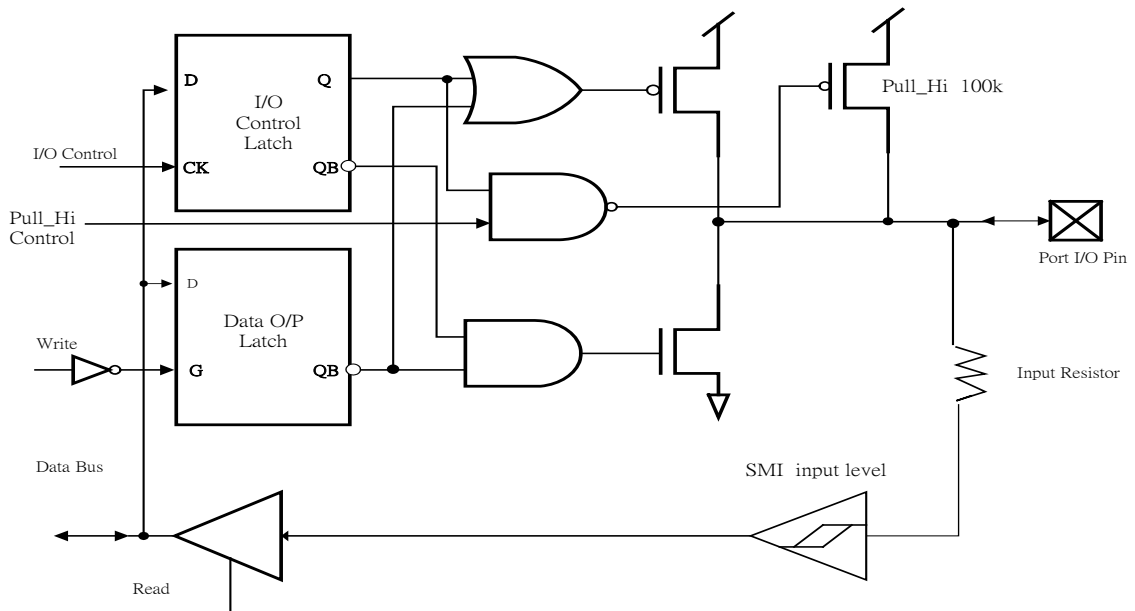
PA4,PA5



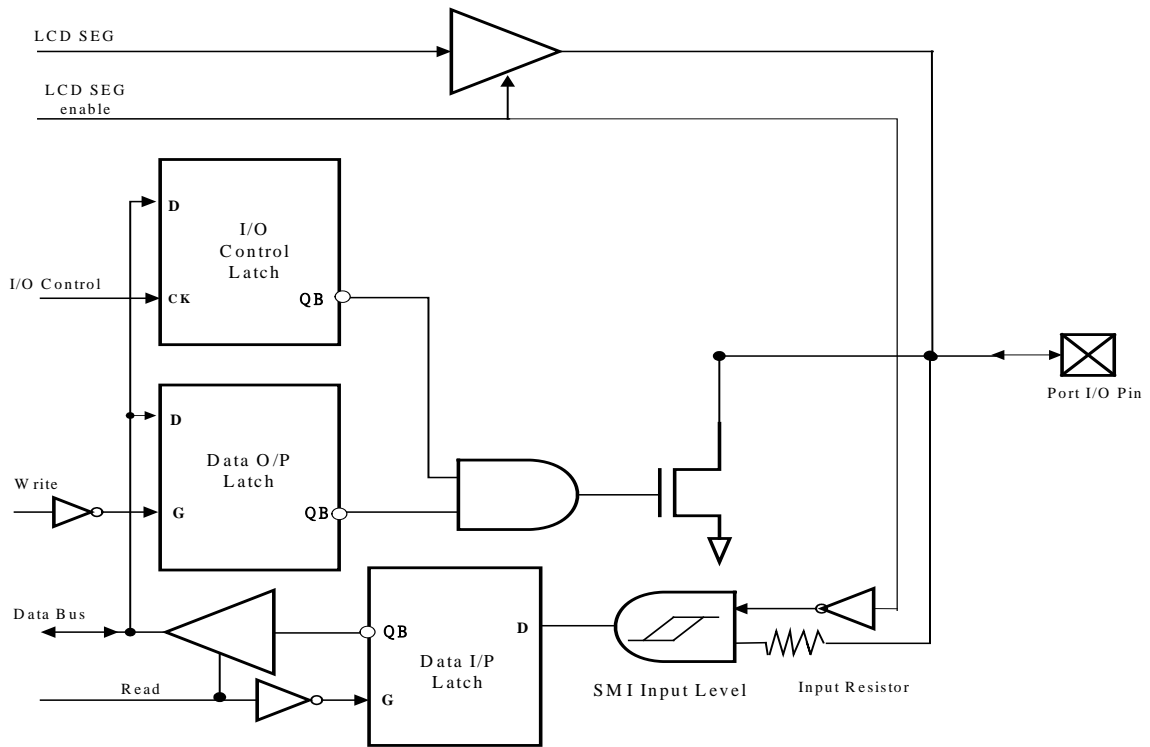
● Port B



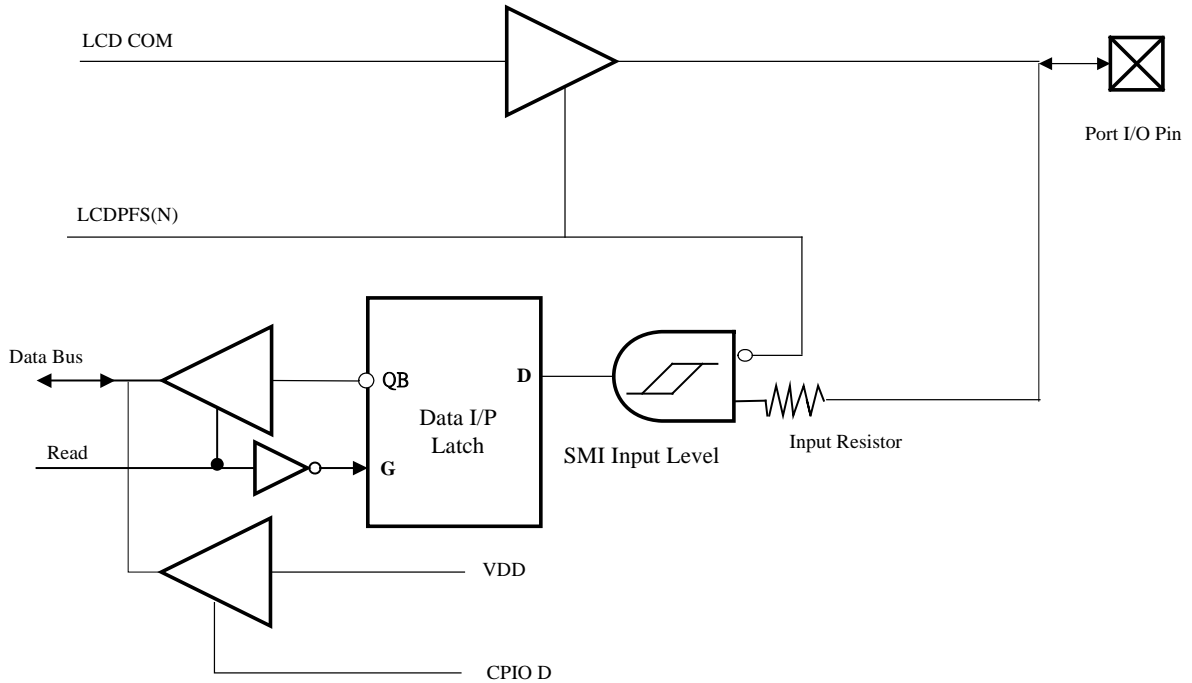
● Port C



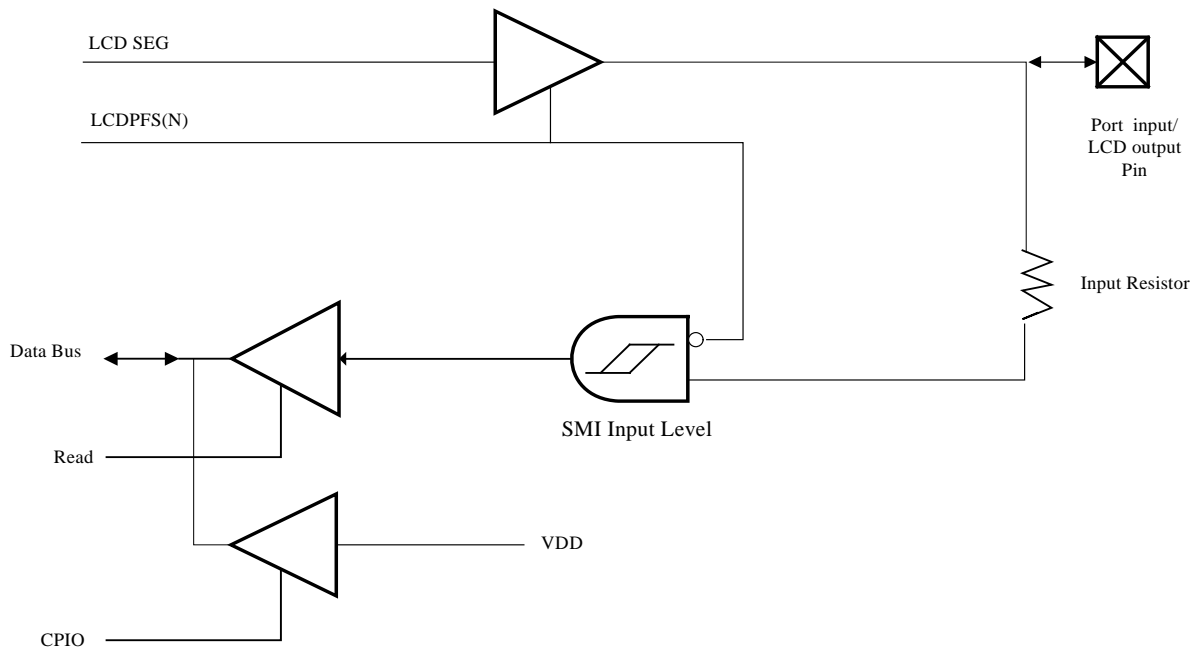
● **Port D**
PD0~PD3



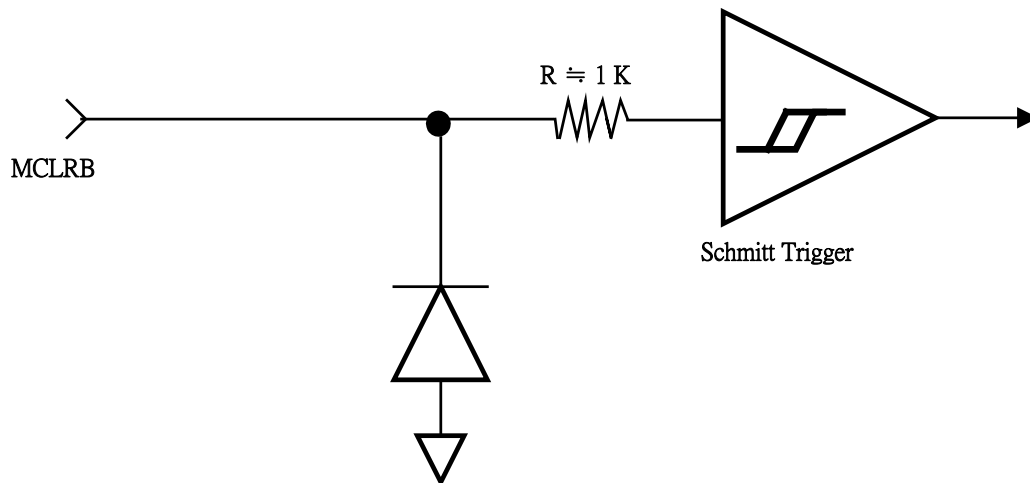
PD5~PD7



● Port E、F、G

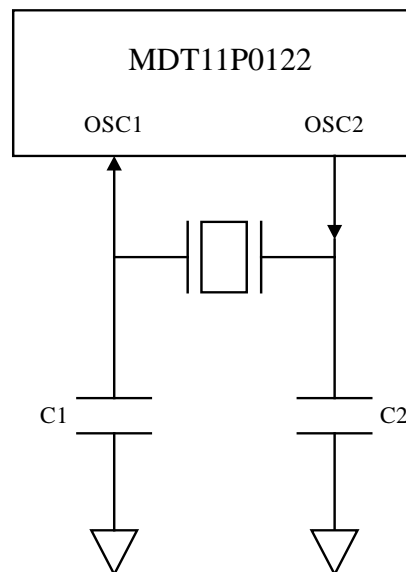


● MCLR PIN



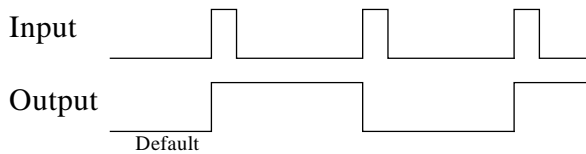
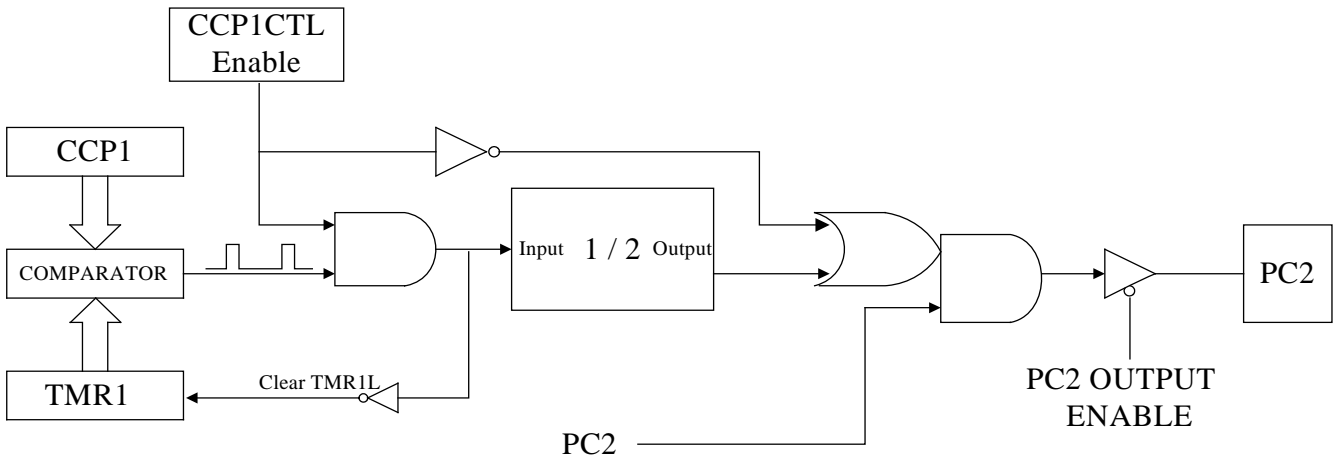
11. External Capacitor Selection For Crystal Oscillator

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF ~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF



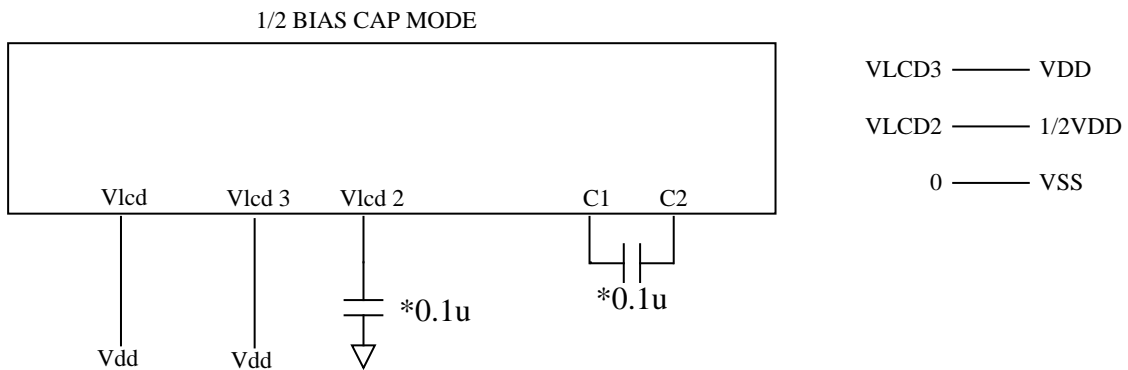
To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor are for reference only, but the higher capacitance also increases the start-up time.

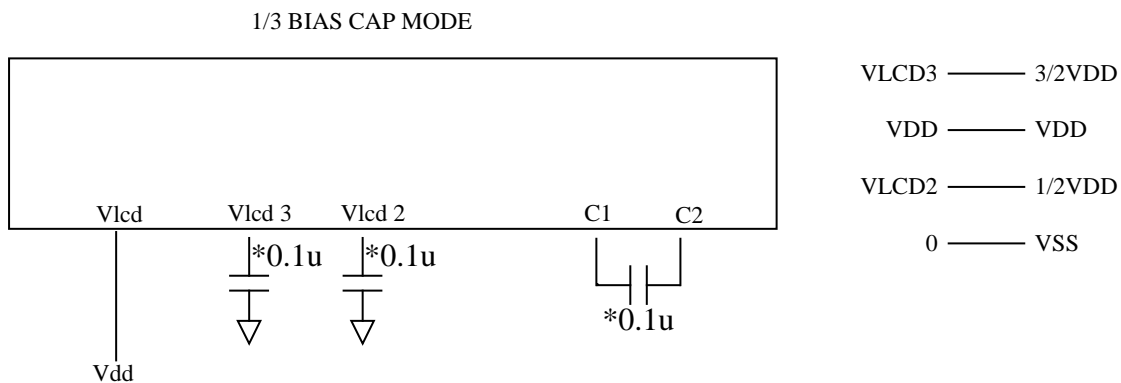
12. Timer1 comapre mode



13. LCD APPLICATION

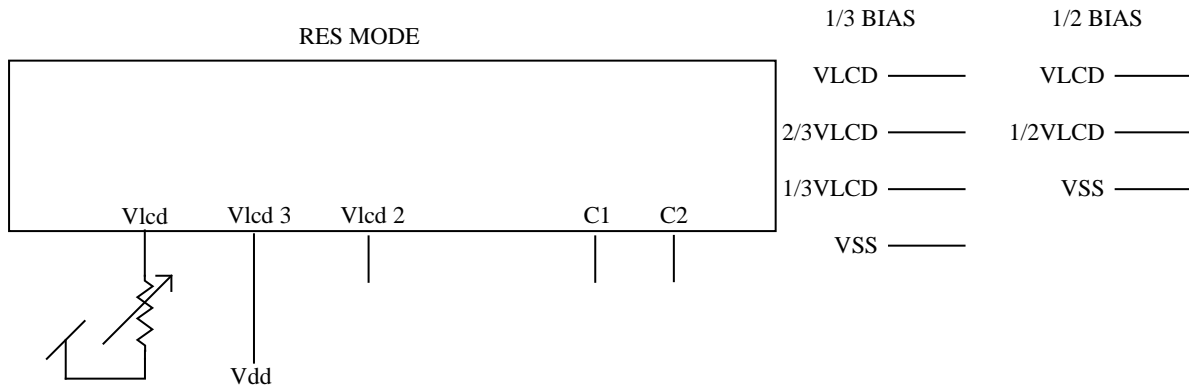
(1) LCD voltage generation at CAP mode





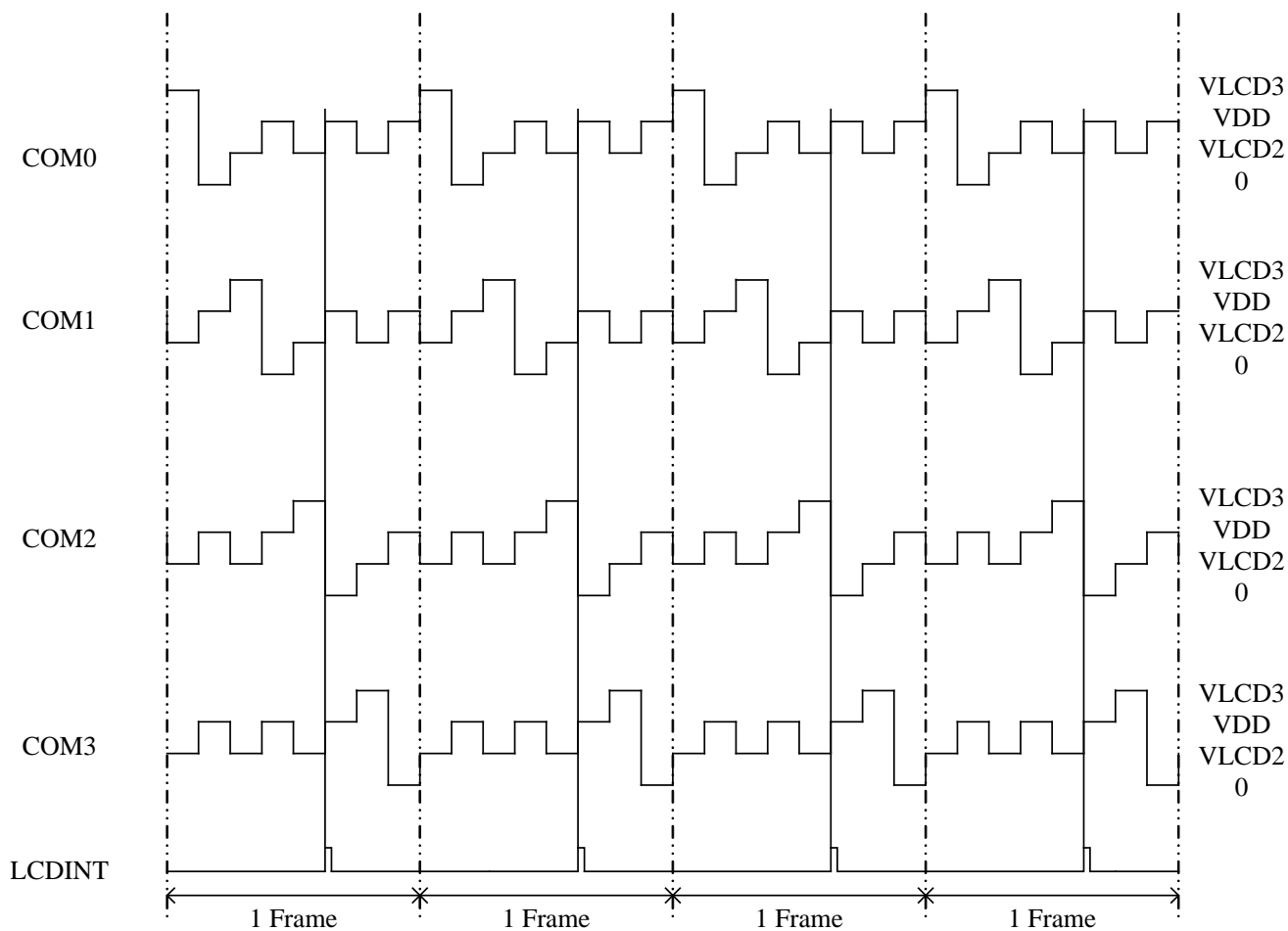
*These value are adjusted to the application by designer

(2) LCD voltage generation at resister mode



* Designer can adjust vlcd resister to change lcd voltage at resister mode.

(3) LCD Interrupt (in 1/3 bias, 1/4 duty)



This interrupt can be used to write next frame data