5A SYNCHRONOUS BUCK SWITCHING REGULATOR

PRODUCTION DATA SHEET

Pb Free Product

DESCRIPTION

The NX9415 is synchronous buck switching converter in multi chip module designed for step down DC to DC converter applications. It is optimized to convert bus voltages from 8V to 22V to as low as 0.8V output voltage. The output current can be up to 5A. An internal regulator converts bus voltage to 5V, which provides voltage supply to internal logic and driver circuit. The NX9415 operates from 200kHz to 2.2MHz and employs loss-less current limiting by sensing the Rdson of synchronous MOSFET followed by hiccup feature.Feedback under voltage protection triggers hiccup.

Other features of the device are: internal schottky diode, thermal shutdown, 5V gate drive, adaptive deadband control, internal digital soft start, 5VREG undervoltage lock out and shutdown capability via the comp pin. NX9415 is available in 4x4 MCM package.

FEATURES

- Single supply voltage from 8V to 22V
- Internal 5V regulator
- Programmable frequency up to 2.2MHz
- Internal Digital Soft Start Function
- Internal boost schottky diode
- Prebias Startup
- Less than 50 nS adaptive deadband
- Current limit triggers hiccup by sensing Rdson of Synchronous MOSFET
- Pb-free and RoHS compliant

APPLICATIONS

- Low Profile On board DC to DC Application
- LCD TV
- Hard Disk Drive
- ADSL Modem

TYPICAL APPLICATION

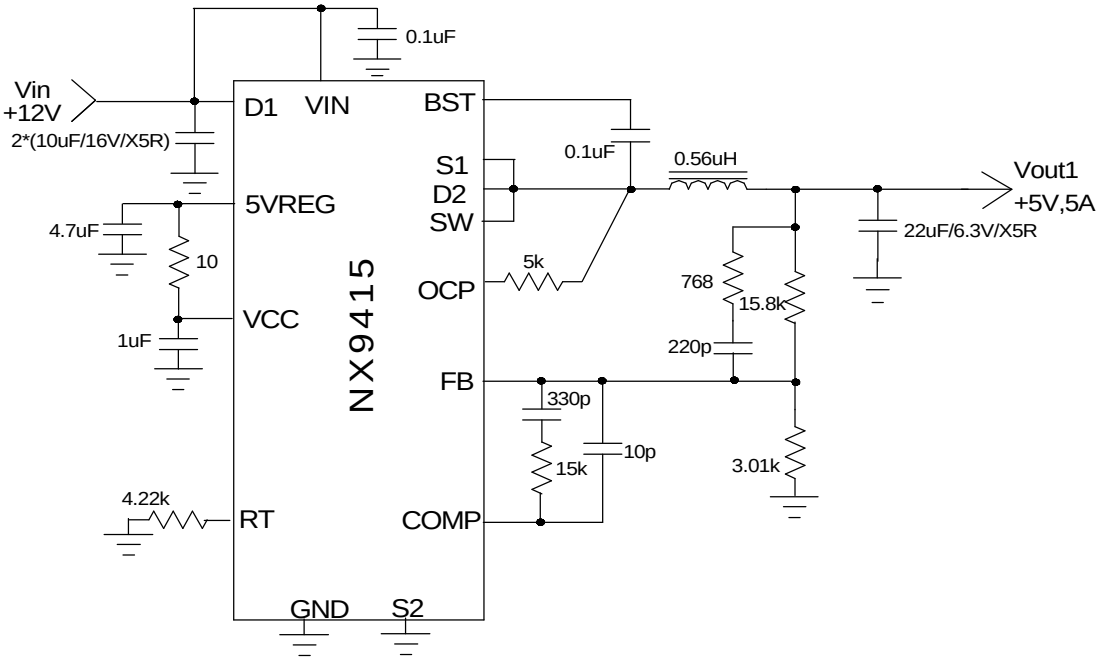

Figure 1 - Typical application of 9415

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX9415CMTR	0 to 70°C	4X4 MCM-24L	200kHz to 2.2MHz	Yes

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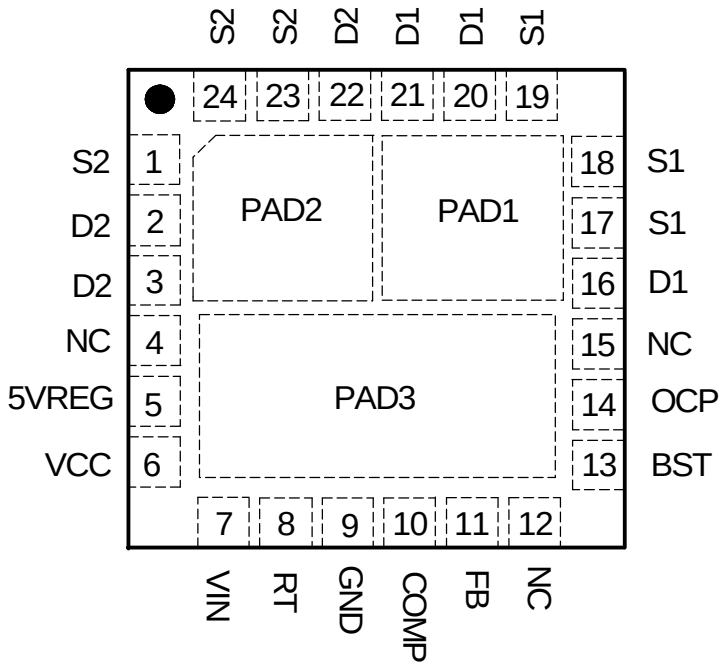
ABSOLUTE MAXIMUM RATINGS

5VREG,VCC to GND & BST to SW voltage ..... -0.3V to 6.5V
VIN to GND Voltage 25V
S1 to GND ..... -2V to 30V
D1 to S1,D2 to S2 ..... 30V
All other pins ..... -0.3V to VCC+0.3V or 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C
ESD Susceptibility 2kV
Power Dissipation ..... Internally Limited by OTP

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

24-LEAD PLASTIC MCM 4 x 4



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ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vin = 12V, and T_A = 0 to 70°C. Followings are bypass capacitors:C_{VIN}=1uF, C_{5VREG}=4.7uF, all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}			0.8		V
Ref Voltage line regulation		V_{in}=9V to 22V		0.4		%
5VREG						
5VREG Voltage range			4.75	5	5.25	V
5VREG Line Regulation		V_{IN}=9V to 22V		10		mV
5VREG Max Current				50		mA
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		9		22	V
Input Voltage Current(Static)		No switching		4.8		mA
Input Voltage Current (Dynamic)		Rt=4.22k		10		mA
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{in} Rising		6.5		V
V_{in}-Hysteresis	V_{in}_Hyst	V_{in} Falling		0.6		V
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		3.9		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V
SS						
Soft Start time	Tss	F_S=2.2MHz		400		uS
Oscillator (Rt)						
Frequency	F_S	Rt=4.22k		2250		kHz
Ramp-Amplitude Voltage	V_{RAMP}			1.5		V
Max Duty Cycle		F_S=2.2MHz		71		%
Min Controlable On Time					150	nS
Error Amplifiers						
Transconductance				2000		umho
Input Bias Current	Ib			10		nA
Comp SD Threshold				0.3		V
FBUVLO						
Feedback UVLO threshold				0.6		V
Over temperature						
Threshold				150		°C
Hysteresis				20		°C
OCP						
OCP current				37		uA
Internal Schottky Diode						
Forward voltage drop		forward current=20mA		350		mV
Ouput Stage						
High Side MOSFET R_{DSON}				31		mohm
Low Side MOSFET R_{DSON}				31		mohm
Output Current				5		A

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
17-19	S1	Source of high side MOSFET and provides return path for the high side driver.
2-3,22,PAD2	D2	Drain of low side MOSFET.
23-24,1	S2	Source of low side MOSFET and needs to be connected to power ground.
21-20,16,PAD1	D1	Drain of high side MOSFET.
5	5VREG	An internal 5V regulator. A high frequency 4.7uF/X5R ceramic capacitor must be connected from this pin to the GND pin as close as possible.
6	VCC	Voltage supply for internal analog circuit and driver
7	VIN	Voltage supply for the internal 5V regulator.
8	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.
9	GND	Ground.
10	COMP	This pin is the output of the error amplifier and is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
11	FB	This pin is the error amplifier inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
13	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1uF must be connected from this pin to SW pin.
14	OCP	This pin is connected to the D2 of the low side MOSFET and is the input of the over current protection(OCP) comparator. An fixed internal current flows to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on.
4,12,15, PAD3	NC	Not used pin. Connecting these pins to ground is recommended.

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BLOCK DIAGRAM

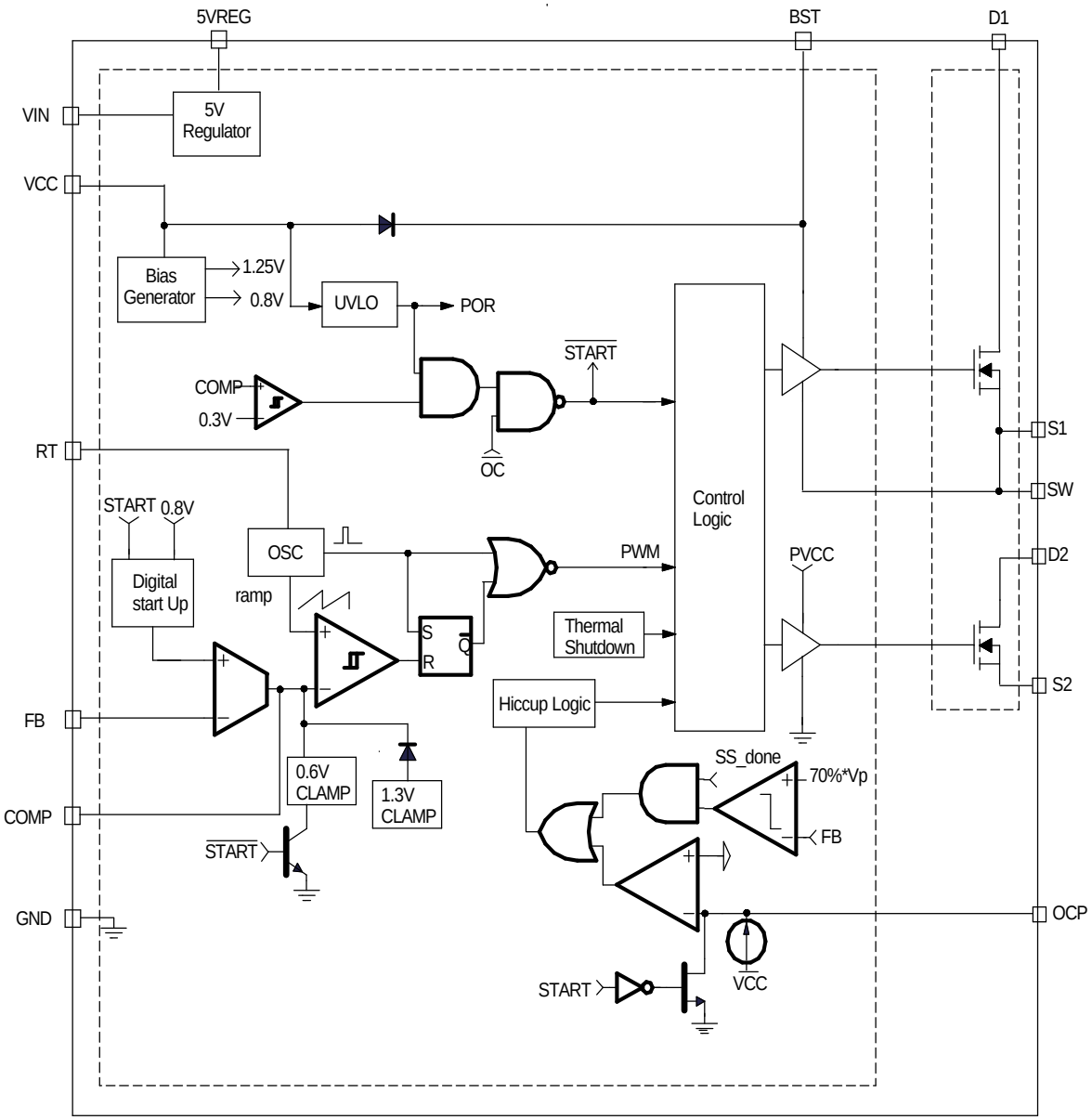

Figure 2 - Simplified block diagram of the NX9415

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TYPICAL APPLICATION

Input Voltage=12V
Output Voltage=5V@5A
Working Frequency=2.2MHz

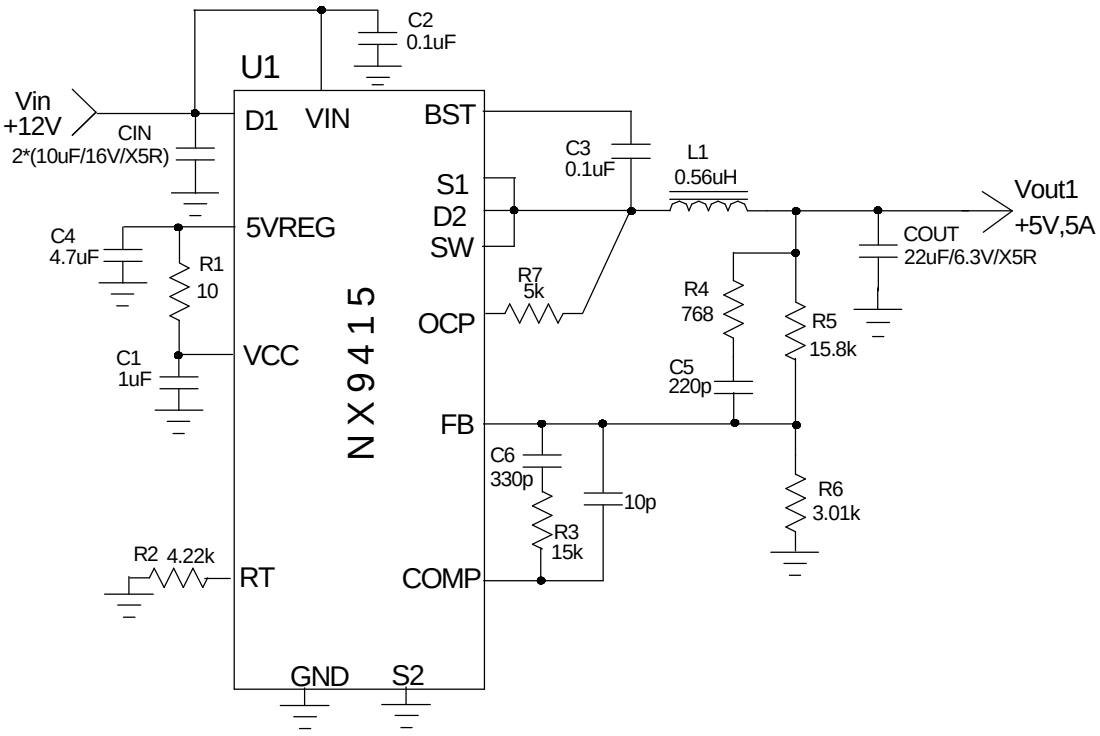

Figure 3- Demo board schematic

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Bill of Materials

Item	Quantity	Reference	Value	Manufacturer
1	1	C1	1u	
2	2	C2,C3	0.1u	
3	1	C4	4.7u/6.3V/X5R	
4	1	C5	220p	
5	1	C6	330p	
6	2	CIN	10u/16V/X5R	
7	1	COUT	22u/6.3V/X5R	
8	1	L1	DO1813P-561HC	Coilcraft
9	1	R1	10	
10	1	R2	4.22k	
11	1	R3	15k	
12	1	R4	768	
13	1	R5	15.8k	
14	1	R6	3.01k	
15	1	R7	5k	
16	1	U1	NX9415CMTR	NEXSEM INC.

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Demoboard waveforms

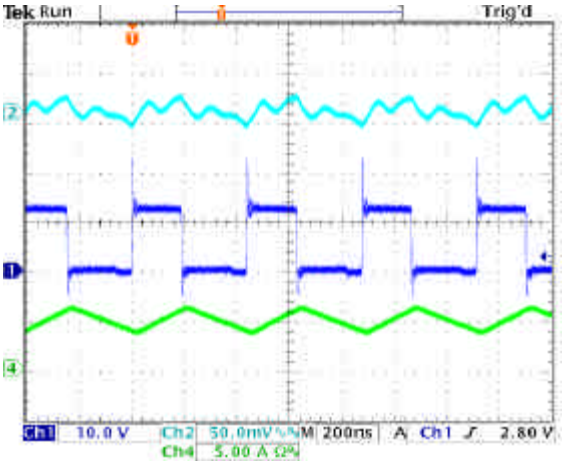

Figure 4 - Output ripple (CH1 SW 10V/DIV, CH2 VOUT AC 50mV/DIV, CH4 OUTPUT CURRENT 5A/DIV)

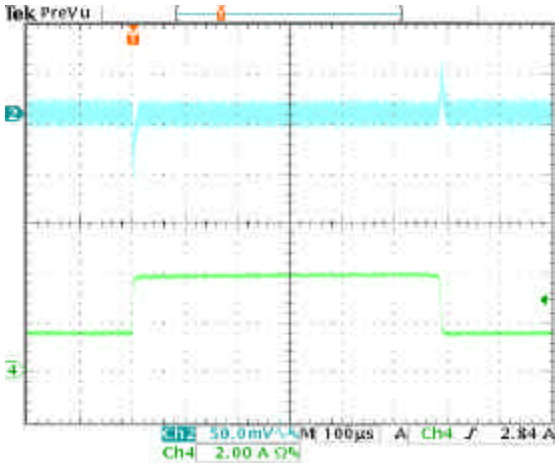

Figure 5 - Output voltage transient response (CH2 VOUT AC 50mV/DIV, CH4 OUTPUT CURRENT 5A/DIV)

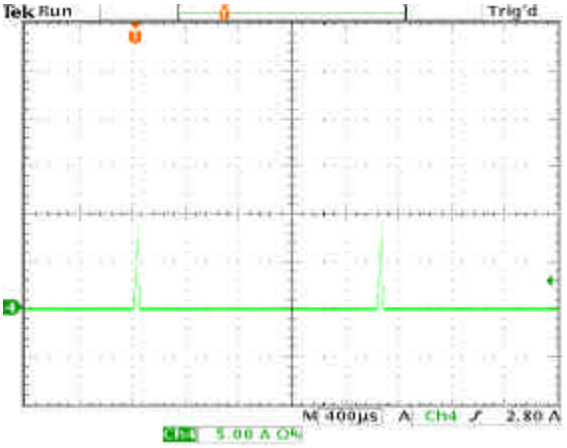

Figure 6 - Over current protection(CH4 OUTPUT CURRENT 5A/DIV)

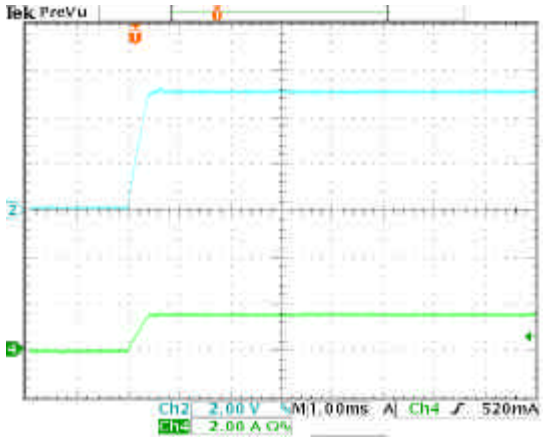

Figure 7 - Startup(CH2 VOUT 2V/DIV, CH4 OUTPUT CURRENT 2A/DIV)

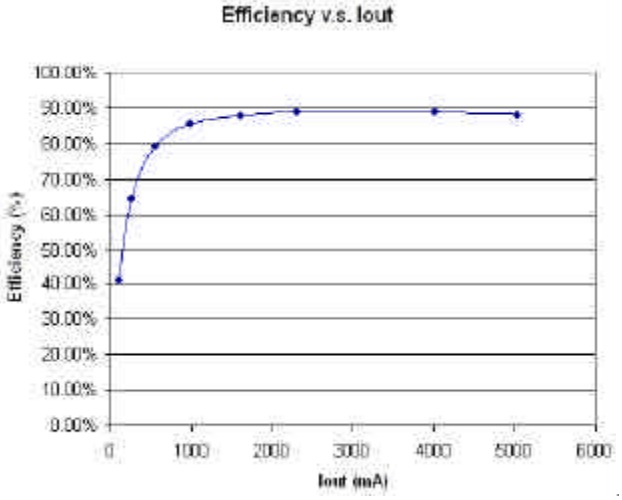

Figure 8 - Output Efficiency @VOUT=5V,VIN=12V

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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{V_{IN} - V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE} = k \times I_{OUTPUT}$$

where k is between 0.2 to 0.4.

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

The amount of voltage ripple during the DC load condition is determined by equation(2).

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \quad ...(2)$$

Where ESR is the output capacitors' equivalent series resistance, C_{OUT} is the value of output capacitors.

Typically when ceramic capacitors are selected as output capacitors, DC ripple spec is easy to be met, but mutiple ceramic capacitors are required at the output to meet transient requirement.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad ...(3)$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R_2 + R_3) \times C_3} \quad ...(4)$$

$$F_{P1} = \frac{1}{2 \times \pi \times R_3 \times C_3} \quad ...(5)$$

$$F_{P2} = \frac{1}{2 \times \pi \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}} \quad ...(6)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m \times Z_f}{1 + g_m \times Z_{in} + Z_{in} / R_1}$$

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For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R_4>>2/gm. And it would be desirable if $R_1||R_2||R_3$>>1/gm can be met at the same time.

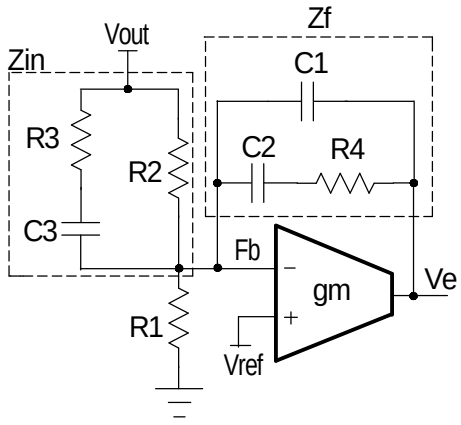

Figure 9 - Type III compensator using transconductance amplifier

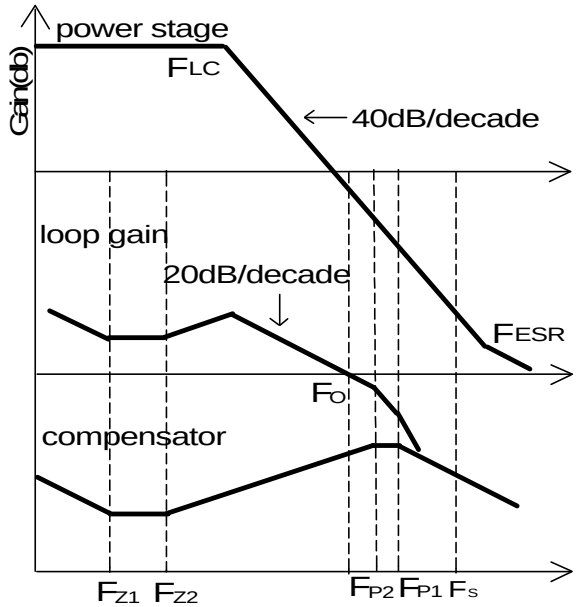

Figure 10 - Bode plot of Type III compensator

B. Type II compensator design

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 12. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$\text{Gain}=g_m \times \frac{R_1}{R_1+R_2} \times R_3 \quad \text{... (7)}$$

$$F_z = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad \text{... (8)}$$

$$F_p \approx \frac{1}{2 \times \pi \times R_3 \times C_2} \quad \text{... (9)}$$

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

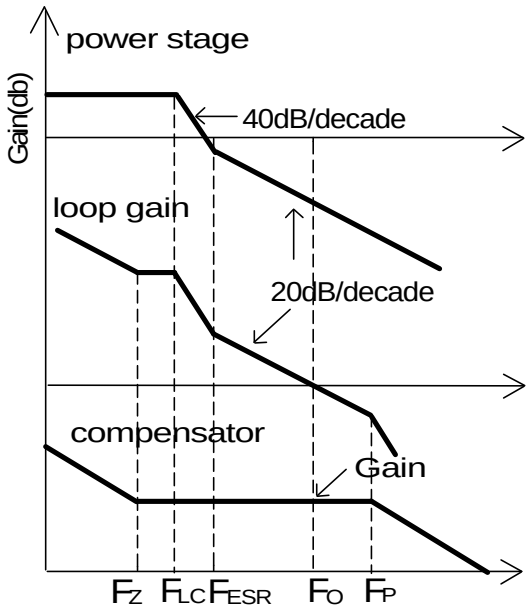

Figure 11 - Bode plot of Type II compensator

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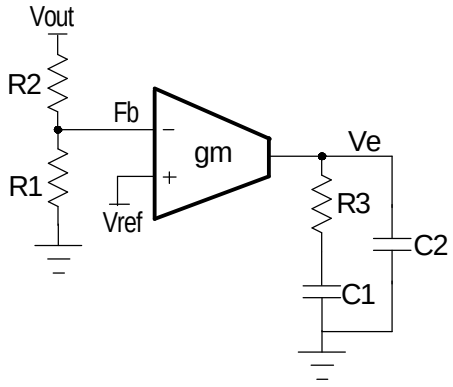


Figure 12 - Type II compensator with transconductance amplifier

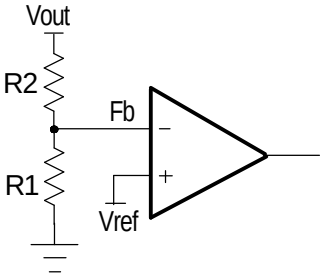
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(10)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

See compensator design for R_1 and R_2 selection.



Voltage divider

Figure 13 - Voltage divider

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. A typical internal current source of 37uA flowing through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs.

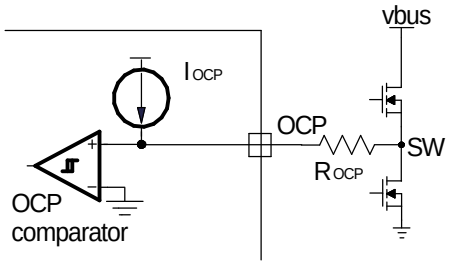


Figure 14 - Over current protection

The over current limit can be set by the following equation

$$I_{SET} = \frac{I_{OCP} \times R_{OCP}}{K \times R_{DSON}}$$

Frequency Selection

The frequency can be set by external Rt resistor. The relationship between frequency and RT pin is shown as follows.

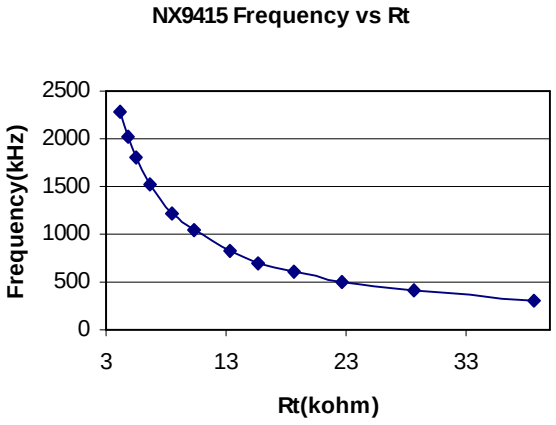


Figure 15 - Frequency versus Rt resistor

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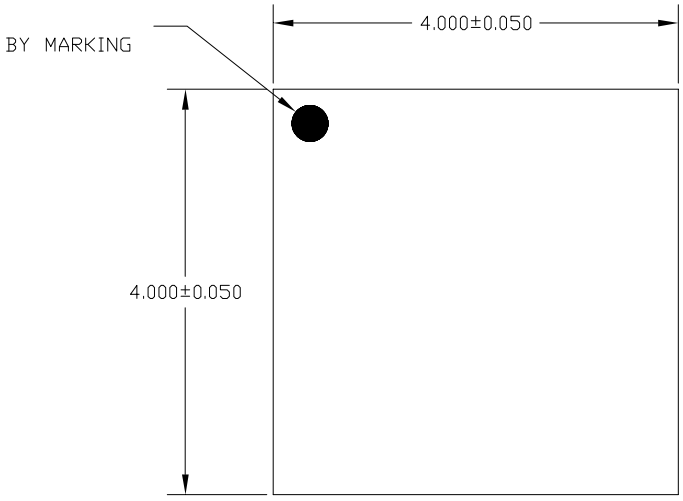
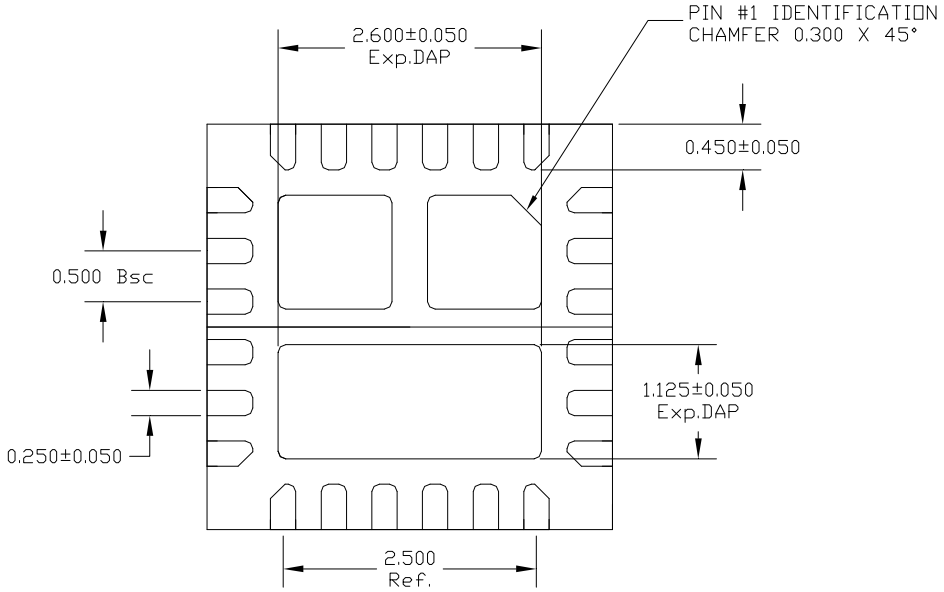
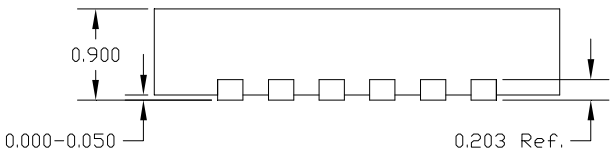
MCM 24 PIN 4 x 4 PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.

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