

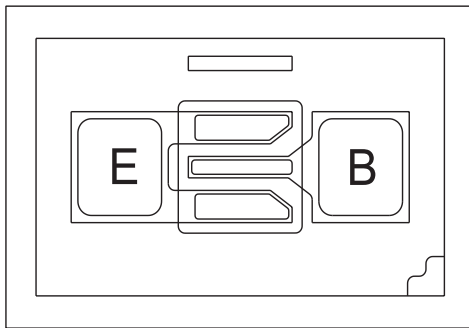
**PROCESS CP207**  
**Small Signal Transistor**  
NPN - Saturated Switch Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	9.0 x 14 MILS
Die Thickness	8.0 MILS
Base Bonding Pad Area	3.1 x 2.9 MILS
Emitter Bonding Pad Area	3.1 x 2.9 MILS
Top Side Metalization	Al - 13,000Å
Back Side Metalization	Au - 6,000Å

**GEOMETRY**



BACKSIDE COLLECTOR

R1

**GROSS DIE PER 4 INCH WAFER**

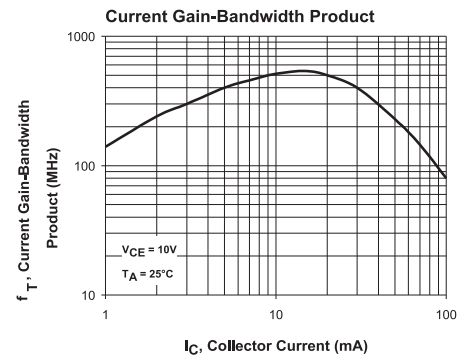
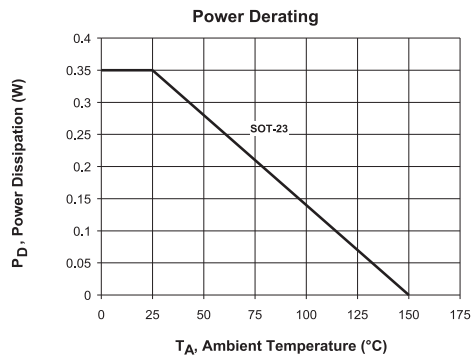
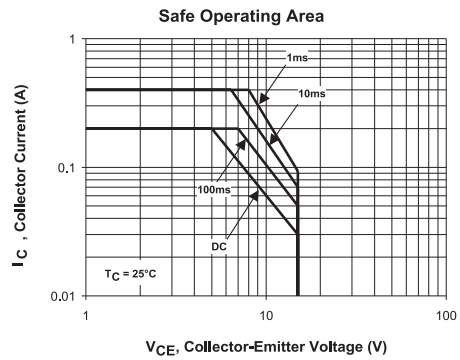
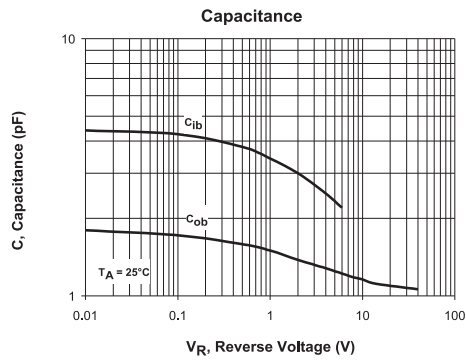
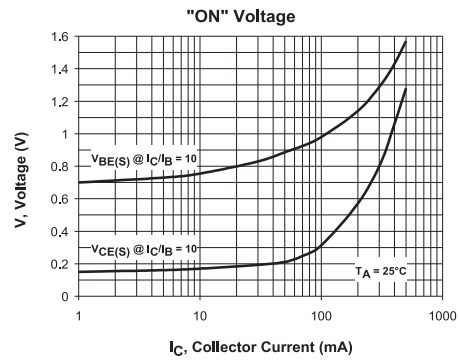
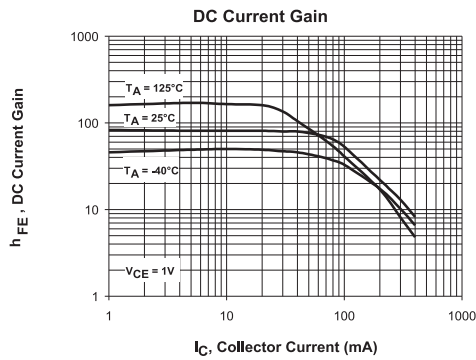
93,430

**PRINCIPAL DEVICE TYPES**

2N2369A  
CMPT2369

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R2 (1-August 2002)



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