High Precision 2-Wire Linear Hall Effect Sensor IC with Pulse Width Modulated Output

Features and Benefits

- Designed for automotive, battery-powered applications
- Customer programmable quiescent duty cycle, sensitivity, and PWM carrier frequency, through VCC pin
- Simultaneous programming of duty cycle, sensitivity, and PWM carrier frequency, for system optimization
- Factory programmed sensitivity temperature coefficient and quiescent duty cycle drift
- Selectable unidirectional or bidirectional quiescent duty cycles
- Pulse width modulated (PWM) output provides increased noise immunity compared to analog output
- Temperature-stable quiescent duty cycle output and sensitivity

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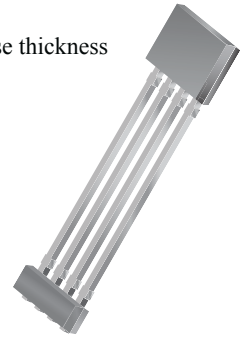
Package: 4-pin SIP (suffix KT)

1 mm case thickness



Not to scale

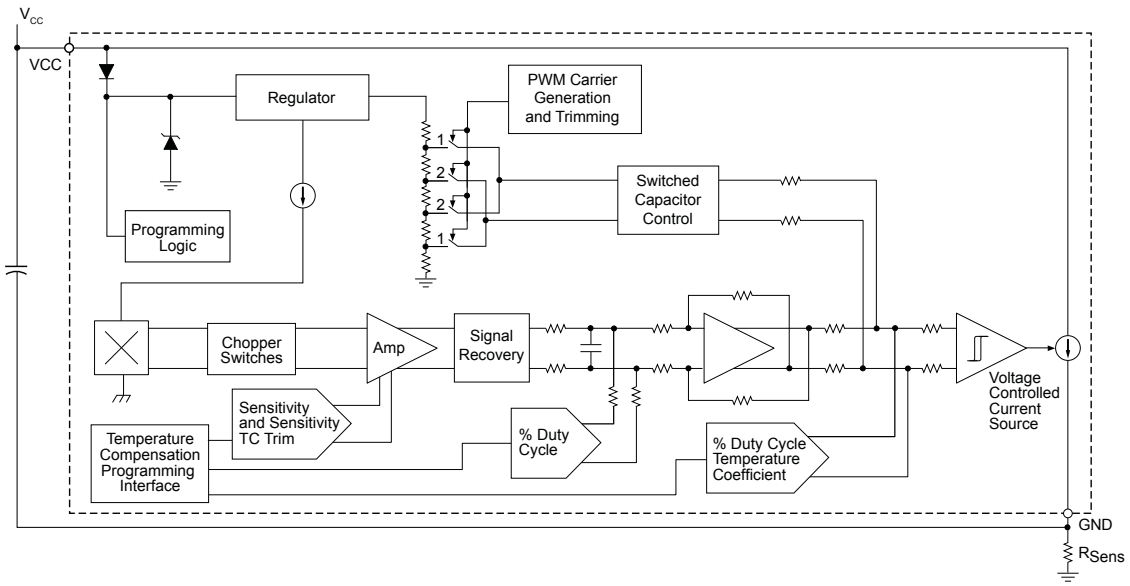
Description

The A1354 device is a high precision, programmable 2-wire Hall effect linear sensor IC with a pulse width modulated (PWM) output. The duty cycle (D) of the PWM output signal is proportional to the applied magnetic field. The A1354 device converts an analog signal from its internal Hall circuit to a digitally encoded PWM output signal. The coupled noise immunity of the digitally encoded PWM output is far superior to the noise immunity of an analog output signal.

The BiCMOS, monolithic circuit inside of the A1354 integrates a Hall element, precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element, a small-signal high-gain amplifier, proprietary dynamic offset cancellation circuits, and PWM conversion circuitry. The dynamic offset cancellation circuits reduce the residual offset voltage of the Hall element. Hall element offset is normally caused by device overmolding, temperature dependencies, and thermal stress. The high frequency offset cancellation (chopping) clock allows a greater sampling rate, which increases the accuracy of the output signal and results in faster signal processing capability.

The A1354 device is provided in a lead (Pb) free 4-pin single inline package (KT suffix), with 100% matte tin leadframe plating.

Functional Block Diagram



Features and Benefits (continued)

- Output duty cycle clamps provide short circuit diagnostic capabilities
- Optional 50% duty cycle calibration test mode at device power-up
- Wide ambient temperature range: –40°C to 125°C
- Resistant to mechanical stress
- Extremely thin package: 1 mm case thickness

Selection Guide

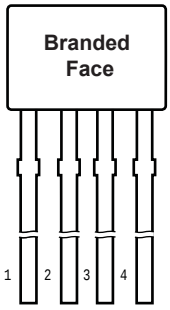
Part Number	Packing*
A1354KKTTN-T	4000 pieces per 13-in. reel

*Contact Allegro® for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–16	V
Forward Supply Current	I_{CC}		50	mA
Reverse Supply Current	I_{RCC}		–50	mA
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 165	ºC

Pin-out Diagram



Terminal List

Number	Name	Function
1	VCC	Input power supply; use bypass capacitor to connect to ground
2	NC	Not connected
3	NC	Not connected
4	GND	Ground

OPERATING CHARACTERISTICS (A) Valid with C_{BYPASS} = 0.01 µF, over full operating temperature range, T_A, and V_{CC}, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage[2]	V_{CC}		4.5	12	16	V
Supply Current	$I_{CC(LOW)}$		–	6	9	mA
	$I_{CC(HIGH)}$		13	–	19	mA
Supply Current Ratio[3]	$I_{CC(rat)}$		2	–	–	–
Power-On Time[4]	t_{PO}	T_A = 25°C, C_L (of test probe)= 10 pF, Sens = 0.1%/G, $f_{PWM} = f_{PWM(slow)}$	–	100	–	ms
		T_A = 25°C, C_L (of test probe)= 10 pF, Sens = 0.1%/G, $f_{PWM} = f_{PWM(fast)}$	–	25	–	ms
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, $I_{CC} = I_{CC}$(max) + 3 mA	28.5	32	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(P-P)}$ magnetic input signal	–	200	–	Hz
Chopping Frequency[5]	f_C	T_A = 25°C	–	200	–	kHz
OUTPUT CHARACTERISTICS						
Response Time[4]	$t_{RESPONSE}$	T_A = 25°C, Impulse magnetic field of 300 G, Sens = 0.1%/G, $f_{PWM} = f_{PWM}$(slow)	–	100	–	ms
		T_A = 25°C, Impulse magnetic field of 300 G, Sens = 0.1%/G, $f_{PWM} = f_{PWM}$(fast)	–	25	–	ms
Clamp Duty Cycles[6]	$D_{CLP(HIGH)}$	T_A = 25°C	90	92.5	95	%
	$D_{CLP(LOW)}$	T_A = 25°C	5	7.5	10	%
Duty Cycle Jitter[4,7]	$Jitter_{PWM}$	T_A = –10°C to 85°C, Sens = 0.12%/G, Measured over 1000 Output PWM clock periods	–	±0.05	–	%
Duty Cycle Resolution	Res_{PWM}	T_A = –10°C to 85°C, Sens = 0.12%/G, Measured over 1000 Output PWM clock periods	–	±0.42	–	G

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Supply voltage, V_{CC}, is defined as the voltage drop between pin 1 and pin 4 of the device. It does not include the voltage drop across R_{SENS}.
[3] I_{CC} ratio is defined as $I_{CC(HIGH)}$ / $I_{CC(LOW)}$ for a given PWM cycle.
[4] See Characteristic Definitions section.
[5] f_C varies up to approximately ±20% over the full operating ambient temperature range, T_A, and process.
[6] Clamp duty cycles are tested with the maximum sensitivity code addressed and an applied magnetic field that is at least 25% greater than the dynamic range.
[7] Jitter is dependent on the sensitivity of the device. Values are based on characterization only and are not guaranteed via production testing.

PROGRAMMING CHARACTERISTICS Valid over full operating voltage range and T_A = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
PRE-PROGRAMMING TARGET[2]						
Pre-Programming Quiescent Duty Cycle Output	$D_{(Q)PRE}$	B = 0 G	–	50	–	%
Pre-Programming Sensitivity	$Sens_{PRE}$		–	0.08	–	%/G
Pre-Programming PWM Output Carrier Frequency	f_{PWMPRE}		–	150	–	Hz
QUIESCENT DUTY CYCLE PROGRAMMING						
Initial Quiescent Duty Cycle Output[3]	$D_{(Q)UNIinit}$	Unipolar device, B = 0 G	–	20	–	%
	$D_{(Q)BIinit}$	Bipolar device, B = 0 G	–	$D_{(Q)PRE}$	–	%
Guaranteed Quiescent Duty Cycle Programming Range[4]	$D_{(Q)UNI}$	Unipolar device, B = 0 G	10	–	30	%
	$D_{(Q)BI}$	Bipolar device, B = 0 G	40	–	60	%
Quiescent Duty Cycle Output[5] Programming Bits		Coarse (range programming)	–	1	–	bit
		Fine (value adjustment)	–	9	–	bit
Average Quiescent Duty Cycle Output Step Size[6,7]	$Step_{D(Q)}$		0.055	0.075	0.095	%
Quiescent Duty Cycle Output Programming Resolution[8]	$Err_{PGD(Q)}$		–	$Step_{D(Q)}$ × ±0.5	–	%
SENSITIVITY PROGRAMMING						
Initial Sensitivity	$Sens_{init}$		–	$Sens_{PRE}$	–	%/G
Guaranteed Sensitivity Programming Range[9]	Sens		0.1	–	0.2	%/G
Sensitivity Programming Bits			–	8	–	bit
Average Sensitivity Step Size[6,7]	$Step_{SENS}$		600	800	900	µ%/G
Sensitivity Programming Resolution[8]	Err_{PGSENS}		–	$Step_{SENS}$ × ±0.5	–	µ%/G
CARRIER FREQUENCY PROGRAMMING						
Initial Carrier Frequency	$f_{PWM(slow)init}$		–	19	–	Hz
	$f_{PWM(fast)init}$		–	f_{PWMPRE}	–	Hz
Guaranteed Carrier Frequency Programming Range[9]	$f_{PWM(slow)}$		12	–	15.5	Hz
	$f_{PWM(fast)}$		95	–	115	Hz
Coarse Carrier Frequency Programming Bits[10]		Coarse (range programming)	–	1	–	bit
		Fine (value adjustment)	–	4	–	bit
Average Carrier Frequency Step Size[6,7]	$Step_{fPWM(slow)}$		0.5	0.8	1.1	Hz
	$Step_{fPWM(fast)}$		4.5	6.4	8.3	Hz
Carrier Frequency Programming Resolution[8]	Err_{PGfPWM}		–	$Step_{fPWM}$ × ±0.5	–	Hz

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PROGRAMMING CHARACTERISTICS (continued) Valid over full operating temperature range, T_A, and V_{CC}, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[1]
CALIBRATION TEST MODE PROGRAMMING						
Calibration Test Mode Selection Bit			–	1	–	bit
LOCK BIT PROGRAMMING						
Overall Programming Lock Bit			–	1	–	bit

[1]1 G (gauss) = 0.1 mT (millitesla).
[2]Raw device characteristic values before any programming.
[3]$D_{(Q)UNIinit}$ may be below the clamp duty cycle $D_{CLP(LOW)}$. $D_{(Q)}$ will not appear to respond to programming pulses until $D_{(Q)} > D_{CLP(LOW)}$.
[4]$D_{(Q)}$(max) is the value guaranteed with all programming fuses blown (maximum programming code set). The $D_{(Q)}$ range is the total range from $D_{(Q)init}$ up to and including $D_{(Q)}$(max). See Characteristic Definitions section.
[5]Bit for selecting between $D_{(Q)BI}$ and $D_{(Q)UNI}$ programming ranges.
[6]Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[7]Non-ideal behavior in the programming D-to-A converter (DAC) can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{D(Q)}$, $Step_{SENS}$, or $Step_{fPWM}$.
[8]Overall programming value accuracy. See Characteristic Definitions section.
[9]f_{PWM}(max) is the value available with all programming fuses blown (maximum programming code set). f_{PWM} range is the total range from $f_{PWMinit}$ up to and including f_{PWM}(max). See Characteristic Definitions section.
[10]Bit for selecting between $f_{PWM(fast)}$ and $f_{PWM(slow)}$ programming ranges.

OPERATING CHARACTERISTICS (B) Valid with C_{BYPASS} = 0.01 µF, over full operating temperature range, T_A, and V_{CC}, unless otherwise noted

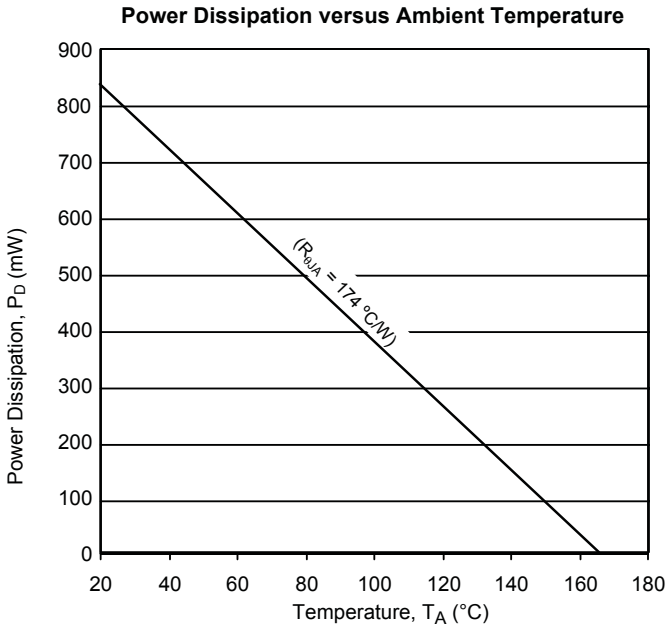
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FACTORY PROGRAMMED SENSITIVITY TEMPERATURE COEFFICIENT AND SENSITIVITY DRIFT						
Sensitivity Temperature Coefficient[1]	TC_{Sens}		–	0.12	–	%/°C
Maximum Sensitivity Drift Through Temperature Range[2,3]	$\Delta Sens_{TC}$	Sens = $Sens_{PRE}$, D = $D_{(Q)PRE}$, calculated at 125°C	–	< ±2	–	%
Sensitivity Drift Due to Package Hysteresis[3,4]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling	–	< ±1.2	–	%
FACTORY PROGRAMMED DUTY CYCLE DRIFT						
Duty Cycle Drift[1,3]	$\Delta D_{(Q)}$	B = 0 G	–	0	–	%
Duty Cycle Drift Error[3]	$Err_{\Delta D(Q)}$	B = 0 G, Sens = $Sens_{PRE}$, D = $D_{(Q)pre}$	–	< ±0.3	–	%
ERROR COMPONENTS						
Linearity Sensitivity Error[3]	Lin_{ERR}		–	< ±1.0	–	%
Symmetry Sensitivity Error[3,5]	Sym_{ERR}		–	< ±1.5	–	%

[1]Programmed at 125°C and calculated relative to 25°C.
[2]Sensitivity drift from expected value at T_A after programming TC_{SENS}. See Characteristic Definitions section.
[3]Specification unit is defined in percent as result of the calculation shown in the Characteristics Definitions section.
[4]See Characteristic Definitions section.
[5]Symmetry error is only valid for bipolar devices.

Thermal Characteristics may require derating at maximum conditions

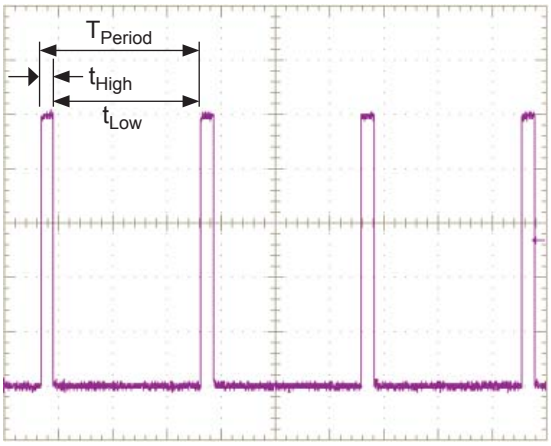
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	174	°C/W

*Additional thermal information available on Allegro website.

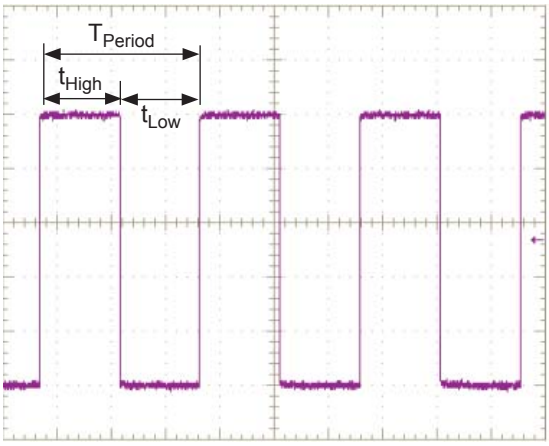


V_{CC} at Various Duty Cycles
4 µs per division

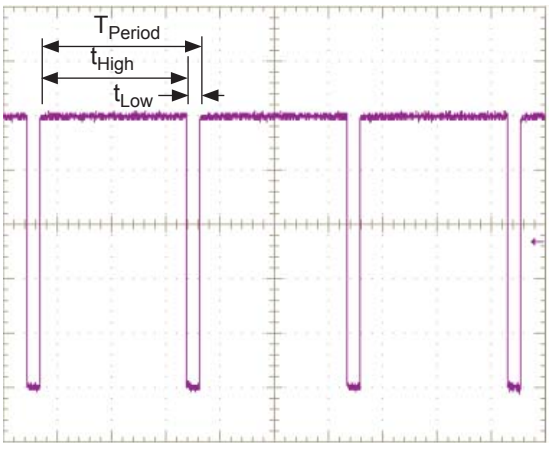
≈10% Duty Cycle (Low Clamp)



≈ 50% Duty Cycle



≈ 90% Duty Cycle (High Clamp)



t_{High} – duration of high voltage

t_{Low} – duration of the low voltage

T_{Period} – one full frequency cycle

Duty Cycle = (t_{High} / T_{Period}) × 100%

Unidirectional Field Detection

Duty Cycle	Field Detection
10%	0 G
10%-90%	0 to +*n* G (south)

Bidirectional Field Detection

Duty Cycle	Field Detection
50%	0 G
50%-90%	0 to +*n* G (south)
50%-10%	0 to –*n* G (north)

Characteristic Definitions

Quiescent Voltage Output and Duty Cycle The operating output voltage, V_{OUT}, is determined by the PWM output voltage duty cycle, D. In turn, D is proportional to a change in air gap between the A1354 Hall element and the magnetic target. The output duty cycle in the quiescent state (no significant magnetic field: B = 0 G), $D_{(Q)}$, remains steady at the specific programmed duty cycle throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before supplying a valid PWM output duty cycle. Power-On Time, t_{PO}, is defined as the time it takes, with no applied magnetic field (quiescent state), for the PWM output voltage duty cycle, $D_{(Q)}$, to settle within ±5% of its steady state value, after the power supply has reached its minimum specified operating voltage, V_{CC}(min).

Response Time The time interval, $t_{RESPONSE}$, between a) when the applied magnetic field reaches 90% of its final value, and b) when the device reaches 90% of its output level corresponding to the applied magnetic field. $t_{RESPONSE}$ depends on the signal delay defined by the device filter bandwidth, BW_i, and a full PWM period, which is required for output update.

Guaranteed Quiescent Duty Cycle Output Range The quiescent duty cycle output, $D_{(Q)}$, can be programmed within the guaranteed quiescent duty cycle range limits: $D_{(Q)}$(min) and $D_{(Q)}$(max). The available guaranteed programming range for $D_{(Q)}$ falls within the distributions of the initial duty cycle, $D_{(Q)init}$, and of the maximum programming code for setting $D_{(Q)}$, as shown in figure 1.

Average Quiescent Duty Cycle Output Step Size The average quiescent duty cycle output step size, $Step_{D(Q)}$, for a single device is determined using the following calculation:

$$Step_{D(Q)} = \frac{D_{(Q)maxcode} - D_{(Q)mincode}}{2^n - 1} \quad , \qquad (1)$$

where:

n is the number of available programming bits in the trim range,
$2^n - 1$ is the value of the maximum programming code in the range, and
$D_{(Q)maxcode}$ is the quiescent output duty cycle at code $2^n - 1$.

Quiescent Duty Cycle Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution is:

$$Err_{PGD(Q)}(typ) = 0.5 \times Step_{D(Q)}(typ) \quad . \qquad (2)$$

Quiescent Output Duty Cycle Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent duty cycle temperature coefficient, $TC_{D(Q)}$, may drift from its nominal value over the range of the operating ambient temperature, T_A. For purposes of specification, the Quiescent Duty Cycle Output Drift Through Temperature Range, $\Delta D_{(Q)}$ (%), is defined as:

$$\Delta D_{(Q)} = D_{(Q)(\Delta TA)} - D_{(Q)(25°C)} \quad . \qquad (3)$$

$\Delta D_{(Q)}$ should be calculated using the actual measured values of $D_{(Q)(\Delta TA)}$ and $D_{(Q)(25°C)}$ rather than ideal programming target values.

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded face of the package, increases the output duty cycle from its quiescent value toward the maximum duty cycle limit. The amount of the output duty cycle increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output duty cycle from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (%/G), of the device, and it is defined for bipolar devices as:

$$Sens = \frac{D_{(BPOS)} - D_{(BNEG)}}{BPOS - BNEG} \quad , \qquad (4)$$

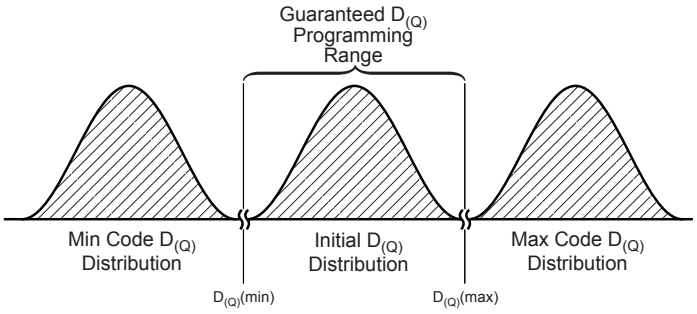


Figure 1. Quiescent output duty cycle versus time

and for unipolar devices as:

$$\text{Sens} = \frac{D_{(\text{BPOS})} - D_{(\text{Q})}}{\text{BPOS}} \quad , \tag{5}$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Guaranteed Sensitivity Range The magnetic sensitivity, Sens, can be programmed around its nominal value within the sensitivity range limits: Sens(min) and Sens(max). Refer to the Guaranteed Quiescent Duty Cycle Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Sensitivity Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Sensitivity Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Guaranteed Carrier Frequency Range The PWM output signal carrier frequency, f_{PWM}, can be programmed around its nominal value in fast mode or slow mode.

Average Carrier Frequency Step Size Refer to the Average Quiescent Duty Cycle Output Step Size section for a conceptual explanation.

Carrier Frequency Programming Resolution Refer to the Quiescent Duty Cycle Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient Device Sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 125°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{\text{Sens}} = \left(\frac{\text{Sens}_{T2} - \text{Sens}_{T1}}{\text{Sens}_{T1}} \times 100\%\right)\left(\frac{1}{T2 - T1}\right) \quad , \tag{6}$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 125°C. The expected value of Sens over the full ambient temperature range, $\text{Sens}_{EXPECTED(TA)}$, is defined as:

$$\text{Sens}_{\text{EXPECTED(TA)}} = \frac{\text{Sens}_{T1} \times [100\% + TC_{\text{SENS}} (T_A - T1)]}{100\ \%} \tag{7}$$

$\text{Sens}_{EXPECTED(TA)}$ should be calculated using the actual measured values of Sens_{T1} and TC_{SENS} rather than ideal programming target values.

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. For purposes of specification, the sensitivity drift through temperature range, ΔSens_{TC}, is defined as:

$$\Delta\text{Sens}_{TC} = \frac{\text{Sens}_{TA} - \text{Sens}_{\text{EXPECTED(TA)}}}{\text{Sens}_{\text{EXPECTED(TA)}}} \times 100\% \ . \tag{8}$$

Sensitivity Drift Due to Package Hysteresis Package stress and stress relaxation can cause the device sensitivity at T_A = 25°C to change during and after temperature cycling.

For purposes of specification, the sensitivity drift due to package hysteresis, ΔSens_{PKG}, is defined as:

$$\Delta\text{Sens}_{PKG} = \frac{\text{Sens}_{(25°C)2} - \text{Sens}_{(25°C)1}}{\text{Sens}_{(25°C)1}} \times 100\% \quad , \tag{9}$$

where $\text{Sens}_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $\text{Sens}_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, after temperature cycling T_A up to 125°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The A1354 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{D_{(+B)} - D_{(Q)}}{2\,(D_{(+B½)} - D_{(Q)})}\right) \times 100\% \ ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{D_{(-B)} - D_{(Q)}}{2\,(D_{(-B½)} - D_{(Q)})}\right) \times 100\% \ , \qquad (10)$$

where:

$$Sens_{Bx} = \frac{|D_{(Bx)} - D_{(Q)}|}{B_x} \ . \qquad (11)$$

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \ . \qquad (12)$$

Note that unipolar devices only have positive linearity error (LIN_{ERRPOS}).

Symmetry Sensitivity Error The magnetic sensitivity of an A1354 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{D_{(+B)} - D_{(Q)}}{D_{(Q)} - D_{(-B)}}\right) \times 100\% \ , \qquad (13)$$

where $Sens_{Bx}$ is as defined in equation 11, and BPOS and BNEG are positive and negative magnetic fields such that |BPOS| = |BNEG|. Note that the symmetry error specification is only valid for bipolar devices.

Jitter The duty cycle of the PWM output may vary slightly over time despite the presence of a constant applied magnetic field and a constant carrier frequency for the PWM signal. This phenomenon is known as jitter, $Jitter_{PWM}$ (%), and is defined as:

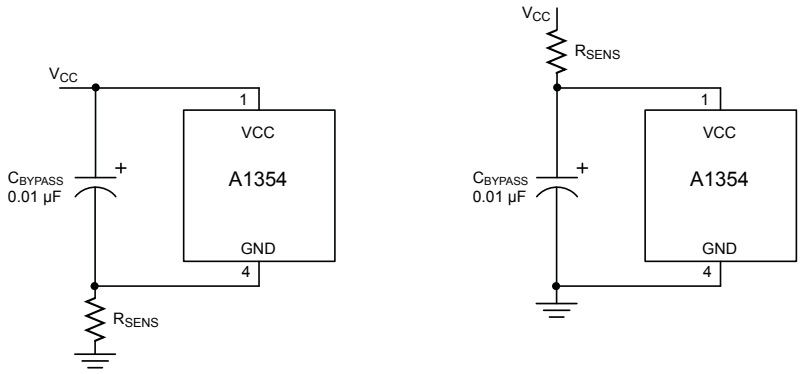
$$Jitter_{PWM} = \pm \frac{D_{Bmax} - D_{Bmin}}{2} \ , \qquad (14)$$

where D_{Bmax} and D_{Bmin} are the maximum and minimum duty cycles measured the over 1000 PWM clock periods with a constant applied magnetic field.

Resolution The ability to derive the value of the applied magnetic field from the device output is affected by jitter. The resolution of the magnetic field, RES_{PWM} (G), is defined as:

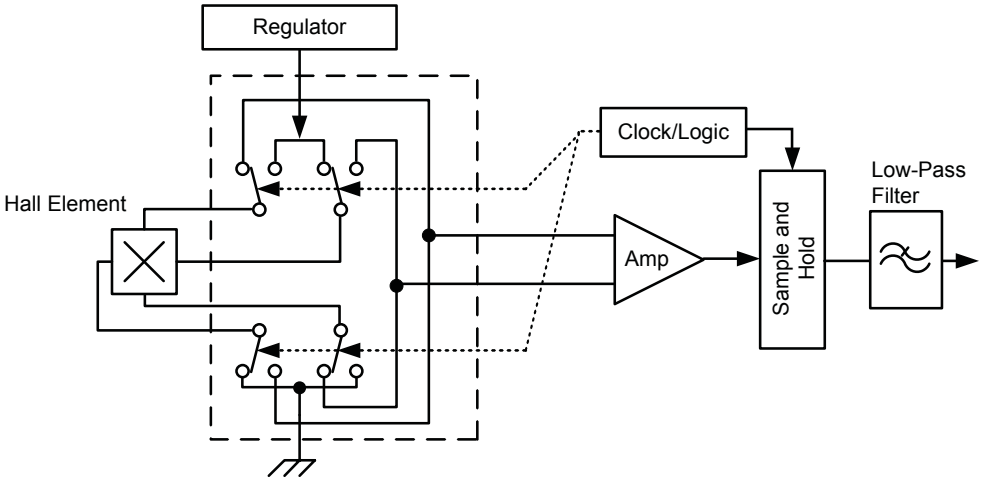
$$RES_{PWM} = \frac{Jitter_{PWM}}{Sens} \ . \qquad (15)$$

Typical Application Drawings



Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Programming Guidelines

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VCC pin of the device. Unique combinations of different voltage amplitude pulses control the internal programming logic of the device to select a programmable parameter and set its value. There are three voltage levels that must be taken into account when programming using a *high* voltage pulse, VPH (consisting of a $V_{P(LOW)} - V_{P(HIGH)} - V_{P(LOW)}$ sequence), and a *mid* voltage pulse, VPM (consisting of a $V_{P(LOW)} - V_{P(MID)} - V_{P(LOW)}$ sequence). The *low* voltage level, $V_{P(LOW)}$, separates the VPH and VPM programming pulses.

The 1354 features Try mode, Blow mode, and Lock mode:

- In Try mode, the value of multiple programmable parameters may be set and measured simultaneously. The parameter values are stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a single programmable parameter may be set, measured, and permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially. This mode is used for blowing the device-level fuse, which permanently blocks the further programming of all parameters.
- Lock mode prevents all future programming of the device. This is accomplished by blowing a special fuse using blow mode.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro website On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

Definition of Terms

Register The section of the programming logic that controls the choice of programmable modes and parameters.

Bitfield The internal fuses unique to each register, represented as a binary number. Incrementing the bitfields of a particular register causes its programmable parameter to change, based on the internal programming logic.

Key A series of mid voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1, or bitfield 0.

Code The number used to identify the combination of fuses activated in a bitfield, expressed as the decimal equivalent of the binary value. The LSB of a bitfield is denoted as code 1, or bit 0.

Addressing Incrementing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing Applying a high pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse A high pulse of sufficient duration to blow the addressed fuse.

Cycling the Supply Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, Protocol at T_A = 25 °C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	$V_{P(LOW)}$	Measured at the VCC pin.	4.5	5	5.5	V
	$V_{P(MID)}$		13	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the VCC and GND pins during programming to provide the current necessary for fuse blowing. The blowing capacitor should be removed and the load capacitance used for properly programming duty cycle measurements.	300	–	–	mA
Pulse Width	t_{LOW}	Duration of $V_{P(LOW)}$ for separating $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses.	40	–	–	µs
	t_{ACTIVE}	Duration of $V_{P(MID)}$ and $V_{P(HIGH)}$ pulses for register selection or bitfield addressing.	40	–	–	µs
	t_{BLOW}	Duration of $V_{P(HIGH)}$ pulses for fuse blowing.	40	–	–	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	5	–	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ to either $V_{P(MID)}$ or $V_{P(LOW)}$.	5	–	100	µs

Mode and Parameter Register Selection

Each mode and programmable parameter can be accessed through a specific register. To select a register, a sequence of voltage pulses consisting of a VPH pulse, a series of VPM pulses, and a VPH pulse (with no VCC supply interruptions) must be applied serially to the VCC pin. The number of VPM pulses is called the *key*, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in figure 2.

The A1354 has two registers that select among the three programming modes:

Register 1:

Blow and Lock

Register 2:

Try

Also, it has four registers that select among the seven programmable parameters:

Register 1:

Sensitivity, Sens

Coarse quiescent duty cycle, $D_{(Q)}$

Register 2:

Fine quiescent duty cycle output, $D_{(Q)}$

Register 3:

Coarse pulse width modulated carrier frequency

Pulse width modulated carrier frequency, f_{PWM}

Register 5:

Calibration Test Mode

Overall device Lock Bit, LOCK

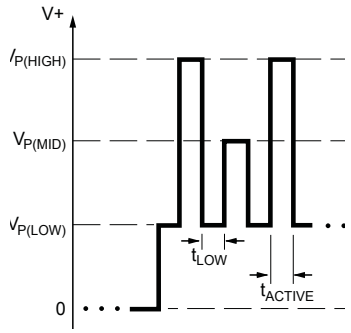


Figure 2. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single VPM pulse.

Bitfield Addressing

After a parameter register has been selected, a VPH pulse transitions the programming logic into the bitfield addressing state. Applying a series of VPM pulses to the VCC pin of the device, as shown in figure 3, increments the bitfield of the selected parameter.

When addressing the bitfield, the number of VPM pulses is represented by a decimal number called the *code*. Addressing activates the corresponding fuse locations in the given bitfield by incrementing the binary value of an internal DAC. The value of the bitfield (and code) increments by one with the falling edge of each VPM pulse, up to the maximum possible code for the register (see the Programming Logic table). As the code increases, the value of the programmable parameter changes. Measurements can be taken after each VPM pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bitfield that have unblown fuses to their initial states.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bitfield. Blowing is accomplished by applying a VPH pulse, called a *blow pulse*, of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bitfield must be blown individually. To accomplish this, the code representing the desired parameter value must be translated to a binary number. For example, as shown in figure 4, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed and blown. An appropriate sequence for blowing code 5 is shown

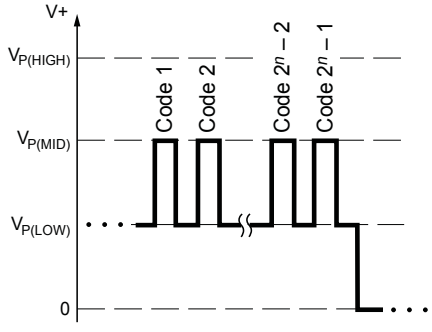


Figure 3. Bitfield addressing pulse train. Addressing the bitfield by incrementing the code causes the programmable parameter value to change. The number of bits available for a given programming code, n, varies among parameters; for example, the bitfield for $D_{(Q)}$ has 6 bits available, which allows 63 separate codes to be used.

in figure 5. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bitfield fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

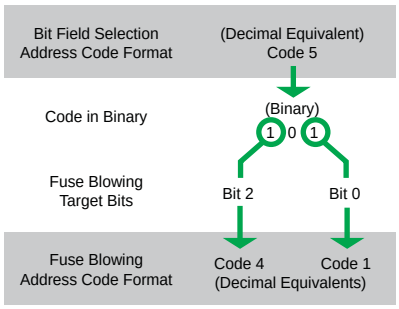


Figure 4. Example of code 5 broken into its binary components, which are code 4 and code 1.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The C_{BLOW} blowing capacitor must be replaced in the final application with a 10 nF bypass capacitor for proper operation.
- The application capacitance, C_{BYPASS}, should be used when measuring the output duty cycle during programming. The blowing capacitor, C_{BLOW}, should be removed during measurement and should only be applied when blowing fuses.
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming sequence is recommended:
  1. Coarse f_{PWM}
  2. Fine f_{PWM}
  3. Coarse $D_{(Q)}$
  4. Sens
  5. Fine $D_{(Q)}$
  6. LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

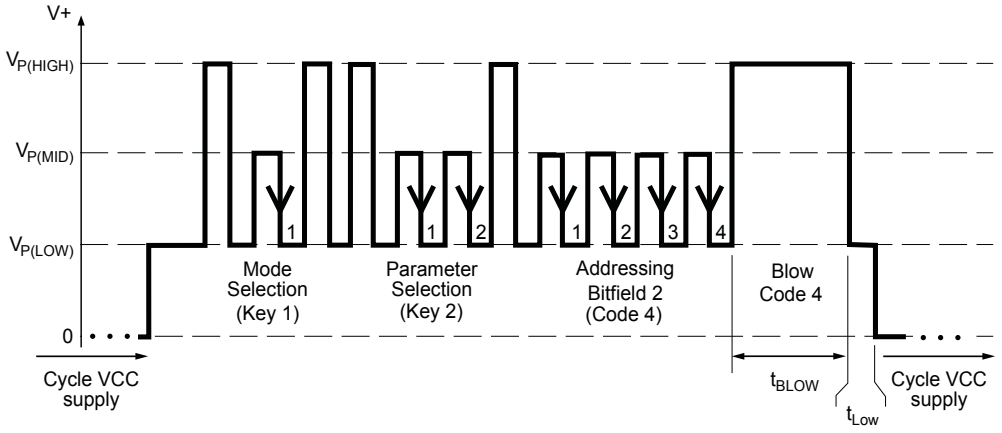


Figure 5. Example of Blow mode programming pulses applied to the VCC pin. In this example, Fine $D_{(Q)}$ (Parameter Key 2) is addressed to code 4 (corresponding to bit 2) and its value is permanently blown.

Programming Modes

Try Mode This mode allows multiple programmable parameters to be tested simultaneously without permanently setting any values. In this mode, each VPH pulse will indefinitely loop the programming logic through the Mode Select, Register Select, and Bitfield Select states, as long as there are no interruptions in the VCC supply.

To enter Try mode, after powering the VCC supply and entering the Initial state, send one VPH pulse to enter Mode Select state, and then two VPM pulses (Mode Selection key 2).

Select the required parameter register and address its bitfield. When addressing the bitfield, each VPM pulse increments the value of the parameter register, up to the maximum possible code (see the Programming Logic table). The addressed parameter value is stored in the device, even after the programming drive voltage is removed from the VCC pin, allowing its value to be measured. To test an additional programmable parameter in conjunction with the original, enter an additional VPH pulse on the VCC pin to re-enter the parameter selection field. Select a different parameter register, and address its bitfield without any supply interruptions. Both parameter values are stored and can be measured after removing the programming drive voltage. Multiple programming combinations can be tested to achieve optimal application accuracy. See figure 6 for an example of the Try mode pulse train.

When testing the device in Try mode, it is recommended to select parameter register 4, the null register, before tests. This recommendation is because the programming voltage levels overlap the V_{CC} operating levels, so varying V_{CC} during tests in Try mode may unintentionally result in device programming.

Registers can be addressed and re-addressed an indefinite number of times, and in any order. After the required code is found for each register, cycle the supply voltage and blow the bitfield fuse using Blow mode. Note that for accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement.

Blow Mode After the required value of the programmable parameter is found using Try mode, the corresponding code should be blown to make the value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Single parameters can still be addressed in Blow mode before fuse blowing (simultaneous addressing of multiple parameters, as in Try mode, is not possible). After powering the VCC supply, select the required parameter register and address its bitfield. When addressing the bitfield, each VPM pulse increments the value of the parameter register, up to the maximum possible code (see Programming Logic table). The addressed parameter value is stored in the device, even after the programming drive voltage is removed from the VCC pin, allowing its value to be measured. Note that for accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement. It is not possible to decrement the value of the register without resetting the parameter bitfield. To reset the bit field, and thus the value of the programmable parameter, cycle the supply voltage.

It is possible to switch between Try and Blow modes where single programmable parameters can be blown in Blow mode while other parameters can still be tested in Try mode.

Lock Mode To lock the device, address the LOCK bit, and apply a blow pulse with C_{BLOW} in place. After locking the device, no future programming of any parameter is possible.

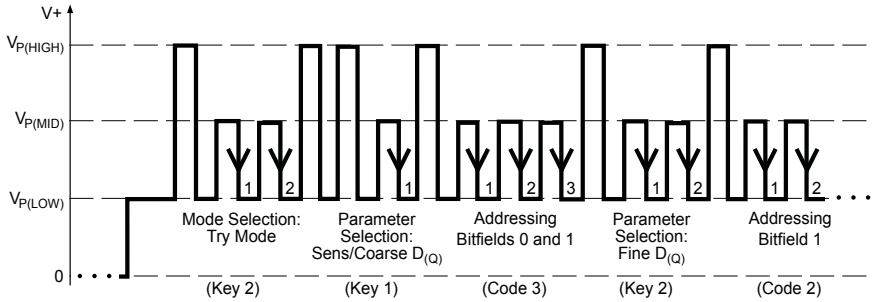
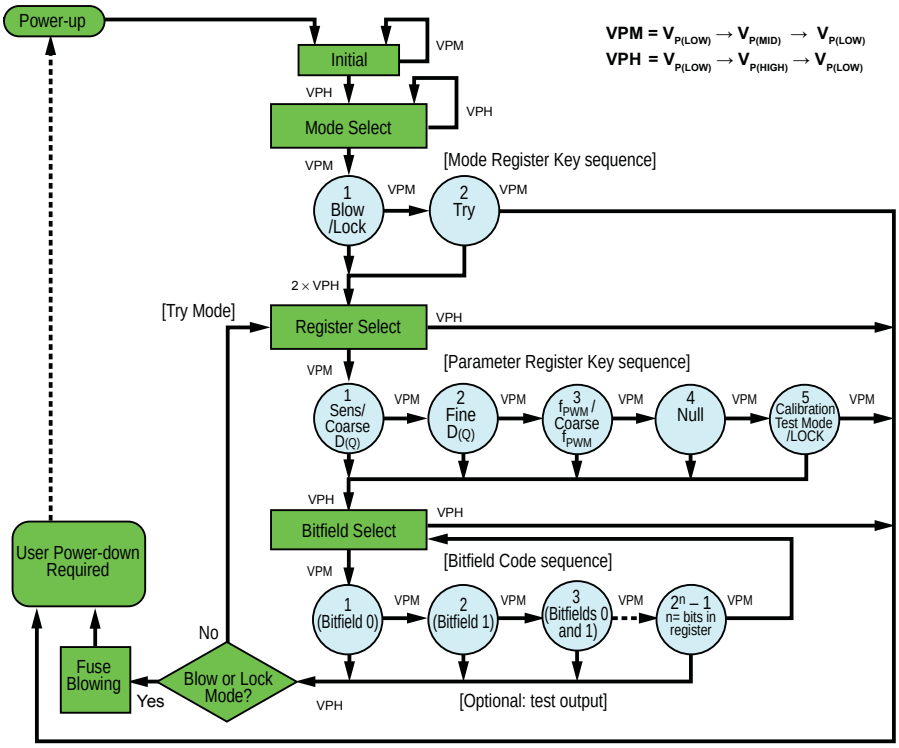


Figure 6. Example of Try mode programming pulses applied to the VCC pin. In this example, Sensitivity (Parameter Key 1) is addressed to code 3, and $D_{(Q)}$ (Parameter Key 2) is addressed to code 2. The values set in the Sensitivity and $D_{(Q)}$ registers are stored in the device until the supply is cycled. Permanent fuse blowing cannot be accomplished in Try mode.

Programming State Machine



Initial State A known state to which the programming logic is reset after system power-up. All the bitfield locations that have intact fuses are reset to logic 0. VPM pulses have no effect. To enter the Mode Select state, apply a single VPH pulse to the VCC pin.

Mode Select State This state allows the selection of the Mode register. To select a Mode register, increment through the keys by applying VPM pulses to the VCC pin. Register keys select among the following programing modes:

- 1 pulse – Blow and Lock
- 2 pulses – Try

To enter the Parameter Select state, apply 2 VPH pulses to the VCC pin.

Parameter Select State This state allows the selection of the Parameter register containing the bitfields to be programmed. Applying VPM pulses to the VCC pin increments through the Parameter registers:

- 1 pulse – Sensitivity / Coarse $D_{(Q)}$
- 2 pulses – Fine $D_{(Q)}$
- 3 pulses – PWM Frequency / Coarse PWM Frequency
- 4 pulses – Null
- 5 pulses – Calibration Test Mode / Device LOCK

To enter the Bitfield Select state, apply 1 VPH pulse to the VCC pin.

Bitfield Select State This state allows the selection of the individual bitfields to be programmed in the selected Parameter register (see the Programming Logic table). Applying VPM pulses to the VCC pin increments the bitfield.

In Try mode, to re-enter the Parameter Selection state, apply 1 VPH pulse on the VCC pin. The previously addressed parameter retains its value as long as V_{CC} is not cycled.

In Blow or Lock mode, to leave the Bitfield Select state requires either cycling V_{CC} or blowing the fuses for the selected code. Note: Merely addressing the bitfield does not permanently set the value of the selected programming parameter; fuses must be blown to do so.

Fuse Blowing State To blow an addressed bitfield, apply a VPH pulse to the VCC pin. Power to the device should then be cycled before additional programming is attempted. Note: Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).

Programming Logic

Register Selection Key	Bitfield Address		Description
	Binary Format (MSB → LSB)	Decimal Equivalent Code	
Mode Register Selection			
Blow / Lock			
1	01	1	Blow or Lock
Try			
2	10	2	Try
Parameter Register Selection			
Sensitivity / Coarse $D_{(Q)}$			
1	000000000	0	Initial value; $D_{(Q)} = D_{(Q)PRE}$, Sens = $Sens_{PRE}$
	011111111	255	Maximum gain value in range
	100000000	256	Enable Coarse $D_{(Q)}$ bit; switch from bidirectional programming to unidirectional programming, $D_{(Q)} = D_{(Q)UNIinit}$
Fine $D_{(Q)}$ (B = 0 gauss)			
2	000000000	0	Initial value
	011111111	255	Maximum $D_{(Q)}$ in range
	100000000	256	Switch from programming increasing $D_{(Q)}$ to programming decreasing $D_{(Q)}$
	111111111	511	Minimum $D_{(Q)}$ in range
PWM Frequency /Coarse PWM Frequency			
3	00000	0	Initial value; $f_{PWM} = f_{PWMPRE}$
	01111	15	Minimum f_{PWM} in $f_{PWM(fast)}$ range
	10000	16	Enable Coarse f_{PWM} bit; switch from $f_{PWM(fast)}$ programming to $f_{PWM(slow)}$ programming, $f_{PWM} = f_{PWM(slow)init}$
	11111	63	Minimum f_{PWM} in $f_{PWM(slow)}$ range
Null			
4	–	–	Recommended to be selected before and during test measurements performed in Try mode
Calibration Test Mode / Lock All			
5	0000000000	0	Initial value
	0000010000	16	Enable 50% duty cycle Calibration Test Mode bit
	1000000000	512	LOCK bit; lock all device registers

Programming Example

This example demonstrates the programming of the device. The recommended sequence for programming is shown in the Additional Guidelines section, but for this example, we start at setting the register for Fine Duty Cycle and then go on to final locking of the device.

To find the correct duty cycle value:

1. Power-on the system.
   This resets all unprogrammed bits in all registers to 0. The device enters the Initial state.
2. Send one VPH pulse to enter the Mode Select state.
3. Send two VPM pulses to select the Try mode.
4. Send two VPH pulses to enter the Register Select state.
5. Send two VPM pulses to select the Fine $D_{(Q)}$ register.
6. Send one VPH pulse to enter the Bitfield Select state.
   The Fine $D_{(Q)}$ register is reset to 000000000.
7. For this example, send one hundred and twenty-eight VPM pulses to set bitfield 7 (010000000, decimal 128).

Now we can measure the device output to see if this is the required value. Assume for this example that the value is slightly too low. So we proceed to change it, as follows:

8. Send one VPM pulse to increment the Fine $D_{(Q)}$ code by 1.
   This yields a total register value of 129 by setting bitfield 0: 010000001.

Assume we measure the device and find this is the correct duty cycle value we require. We are finished trying values for this parameter, and now want to set the value permanently by blowing the corresponding bitfield fuses. Blowing fuses is done one bitfield (one fuse) at a time. We are setting two bitfields, so we have to blow them in two stages:

9. Reset the device by powering it off and on.
   The device returns to the Initial state.
10. Send one VPH pulse to enter the Mode Select state.
11. Send one VPM pulse to select the Blow mode.
12. Send two VPH pulses to enter the Register Select state.
13. Send two VPM pulses to select the Fine $D_{(Q)}$ register.
14. Send one VPH pulse to enter the Bitfield Select state.
    The Fine $D_{(Q)}$ register is reset to 000000000.
15. Send one hundred and twenty-eight VPM pulses to set bitfield 7. (The bitfields can be set in any order.)
16. Send one VPH pulse to exit the Bitfield Select state.
    The bitfield fuse is blown.

One of the two bitfields is programmed. Now we program the other bitfield:

17. Repeat steps 9 to 14 to select the Fine $D_{(Q)}$ register again and enter the Bitfield Select state. This time, however, the register resets to 010000000, because bit 7 has been permanently set.
18. Send one VPM pulse to set bit 0.
19. Send one VPH pulse to exit the Bitfield Select state.
    The bitfield fuse is blown.

Program the remaining parameter by repeating the above steps. After programming all parameters, we can lock the device:

20. Reset the device by powering it off and on. The device returns to the Initial state.
21. Send one VPH pulse to enter the Mode Select state.
22. Send one VPM pulse to select the Lock mode.
23. Send two VPH pulses to enter the Register Select state.
24. Send five VPM pulses to select the LOCK register. The register resets either to 0000000000, or to 0000010000 if Calibration Test mode has been previously enabled.
25. Send one VPH pulse to enter the Bitfield Select state.
26. Send five hundred and twelve VPM pulses to set the LOCK bit, bitfield 9.
27. Send one VPH pulse to exit the Bitfield Select state. The bitfield fuse is blown. Programming of the device is complete. Optionally, test the results, or power-off the device.

Calibration Test Mode

The Calibration Test mode is provided so that the user can compensate for differences in the ground potential between the A1354 and any interface circuitry used to measure the pulse width of the A1354 output. This test mode is optional and must be enabled by blowing its programming bit. After the test mode bit has been blown, the device enters Calibration Test mode every time the device is powered-up.

In customer applications the PWM interface circuitry (body control module: BCM in figure 7) and the A1354 may be powered via different power and ground circuits. As a result, the ground reference for the A1354 may differ from the ground reference of the BCM. In some customer applications this ground difference can be as large as ± 0.5 V.

Differences in the ground reference for the A1354 and the BCM can result in variations in the threshold voltage used to measure the duty cycle of the A1354. If the PWM conversion threshold voltage varies, then the duty cycle will vary because there is a finite rise time, t_r, and fall time, t_f, in the PWM waveform. This problem is shown in figure 8.

The Calibration Test mode allows end users to compensate for any threshold errors that result from a difference in system ground potentials. While the A1354 is in the test period, the

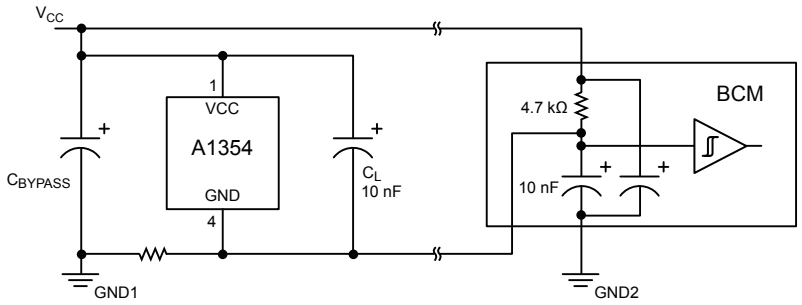


Figure 7: In many applications the A1354 may be powered using a different ground reference than the BCM. This may cause the ground reference for the A1354 (GND 1) to differ from the ground reference of the BCM (GND 2) by as much as to ±0.5 V.

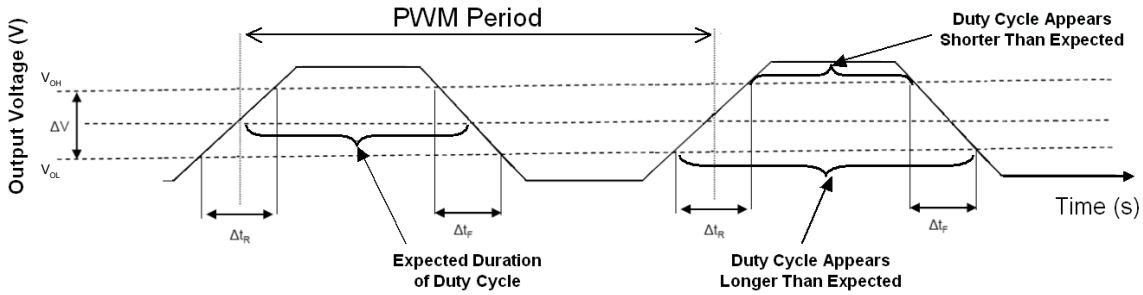


Figure 8. When the threshold voltage is correctly centered between V_{OH} and V_{OL}, the duty cycle accurately coincides with the applied magnetic field. If the threshold voltage is raised, the output duty cycle appears shorter than expected. Conversely, if the threshold voltage is lowered, the output duty cycle is longer than expected.

device output waveform is a fixed 50% duty cycle (the programmed quiescent duty cycle value) regardless of the applied external magnetic field. After powering-up, the A1354 outputs its quiescent duty cycle waveform for 800 ms, regardless of the applied magnetic field (see figure 9). This allows the BCM to compare the measured quiescent duty cycle with an ideal 50% duty cycle.

After the initial 800 ms has elapsed, the duty cycle corresponds to an applied magnetic field as expected. The 800 ms calibration test time corresponds to a PWM frequency of 125 Hz. If the PWM frequency is programmed away from its target of 125 Hz, the duration of the calibration test time will scale inversely with the change in PWM frequency.

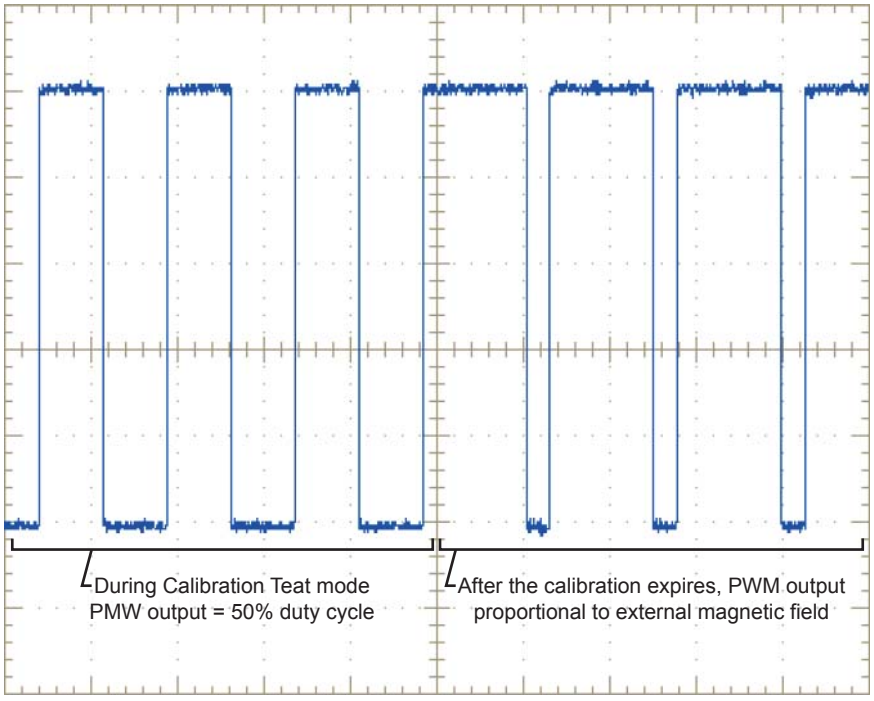
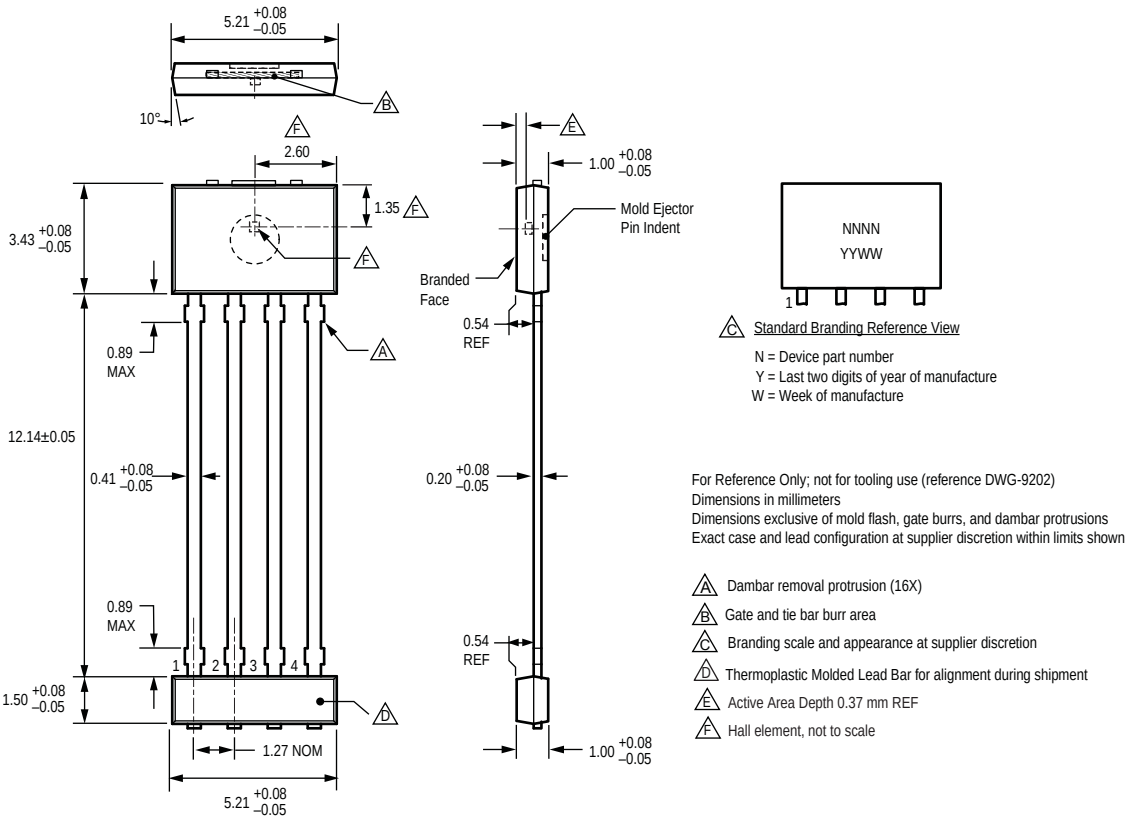


Figure 9. Calibration Test Mode. After powering-on, the A1354 outputs a 50% duty cycle for the first 800 ms, regardless of the applied magnetic field (Calibration Test mode in effect). After the initial 800 ms has elapsed, the output responds to a magnetic field as expected. The example in this figure assumes that a large +B (south polarity) field is applied to the device after the initial 800 ms.

Package KT, 4-Pin SIP



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