Product List

SM59128C25, 25MHz 128KB internal flash MCU
SM59128C40, 40MHz 128KB internal flash MCU

Description

The SM59128 series product is an 8-bit single chip microcontroller embedded with 128KB on-chip flash with In-System Programming (ISP) capability and 1024 bytes RAM. It is a derivative of the 8052 microcontroller family. In addition, SM59128 has IIC interface which is compatible with standard VESA DDC/CI and built in 4-channel SPWM. User can access on-chip expanded RAM by its 'bank mapping direct addressing mode' scheme. With its hardware features and powerful instruction sets, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC or QFP package, or applications which need up to 64K bytes flash memory for program and/or for data.
To program the on-chip flash memory, commercial writers are available by parallel programming method. On the other hand, the on-chip flash memory can be programmed through either parallel or serial interface with its ISP feature.

Ordering Information

yymmv
SM59128ihhkL

yy: year, mm: month
v: version identifier{ , A, B,…}
i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
L: PB Free identifier
{No text is Non-PB Free，"P"is PB Free}

Postfix	Package	Pin / Pad Configuration
P	40L PDIP	Page 2
J	44L PLCC	Page 3
Q	44L QFP	Page 4

Features

- Working Voltage: 4.5V to 5.5 V
- General 8052 family compatible
- 12 clocks per machine cycle
- 128K bytes on-chip flash with In-System Programming (ISP) capability
- IIC (Two wire serial bus) interface compliant with VESA DDC 2B/2Bi/2B+ standard
- On-chip 1024 bytes RAM
- Three 16-bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Temperature range of Industrial level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power-Saving mode: Idle mode and Power-down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address $0000 blank initiate ISP service program
- Configurable ISP service program space with N*512 bytes (N=0 to 8) size
- 4-channel SPWM function
- Flash Memory Endurance : 100K erase and write cycles each byte at TA=25℃
- Flash Memory Data Retention :10 years

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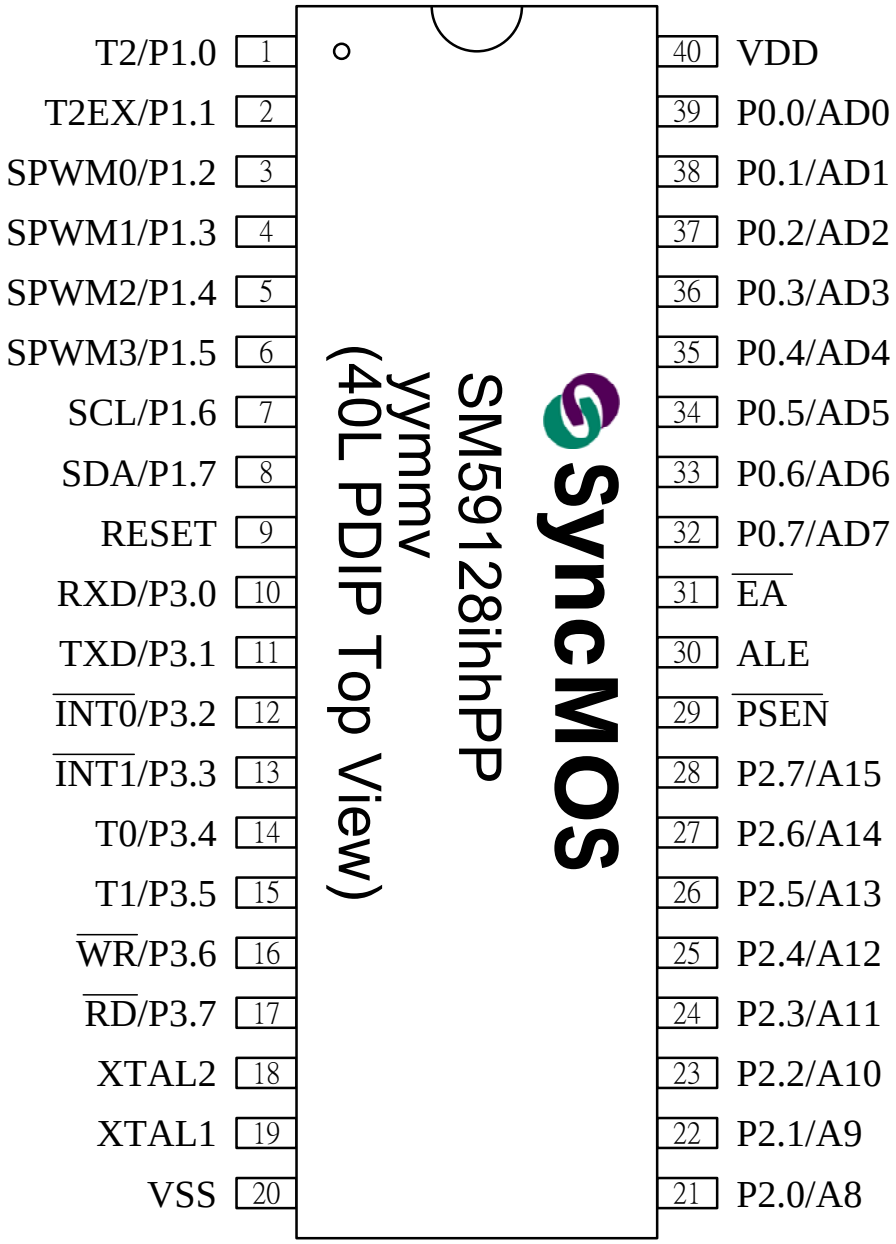
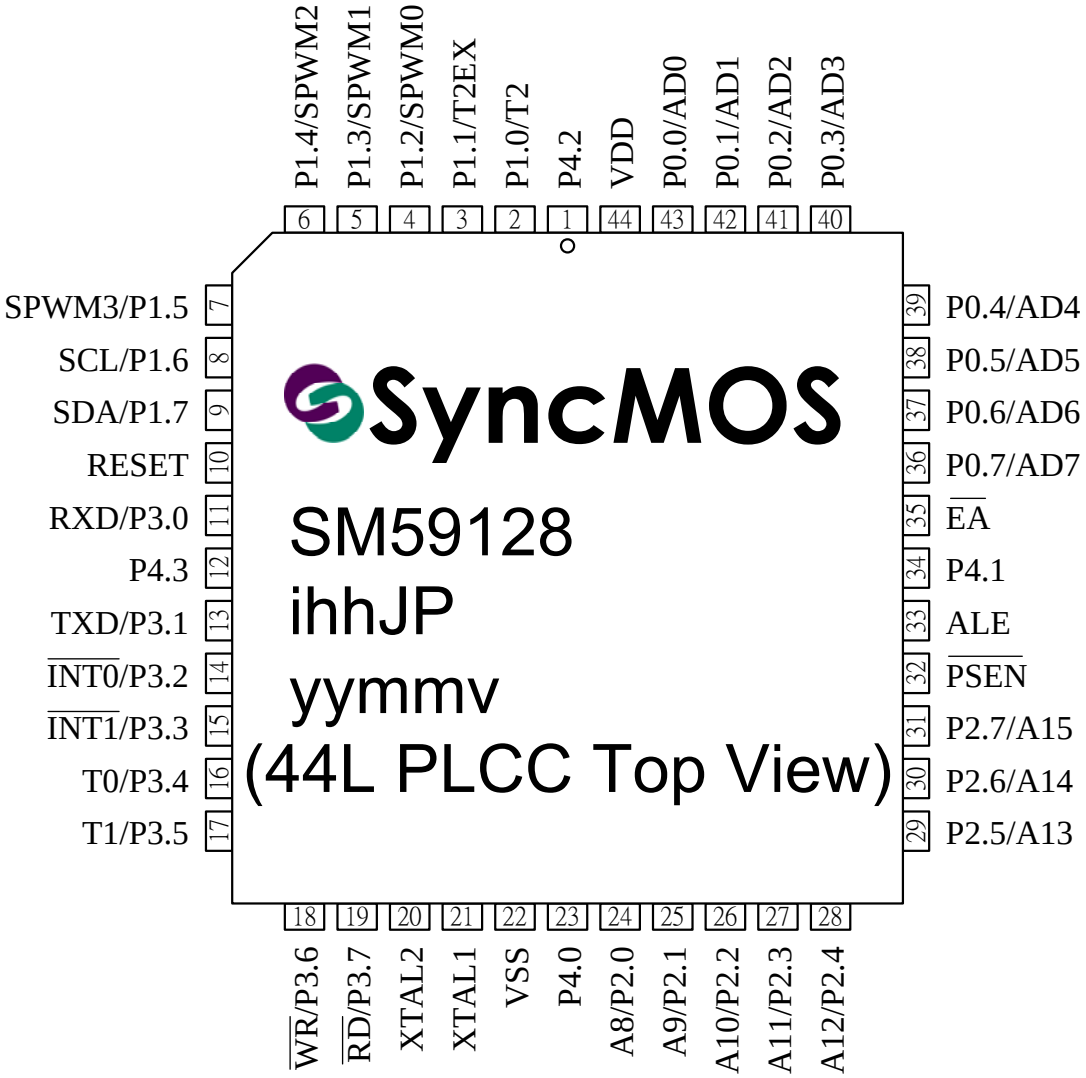
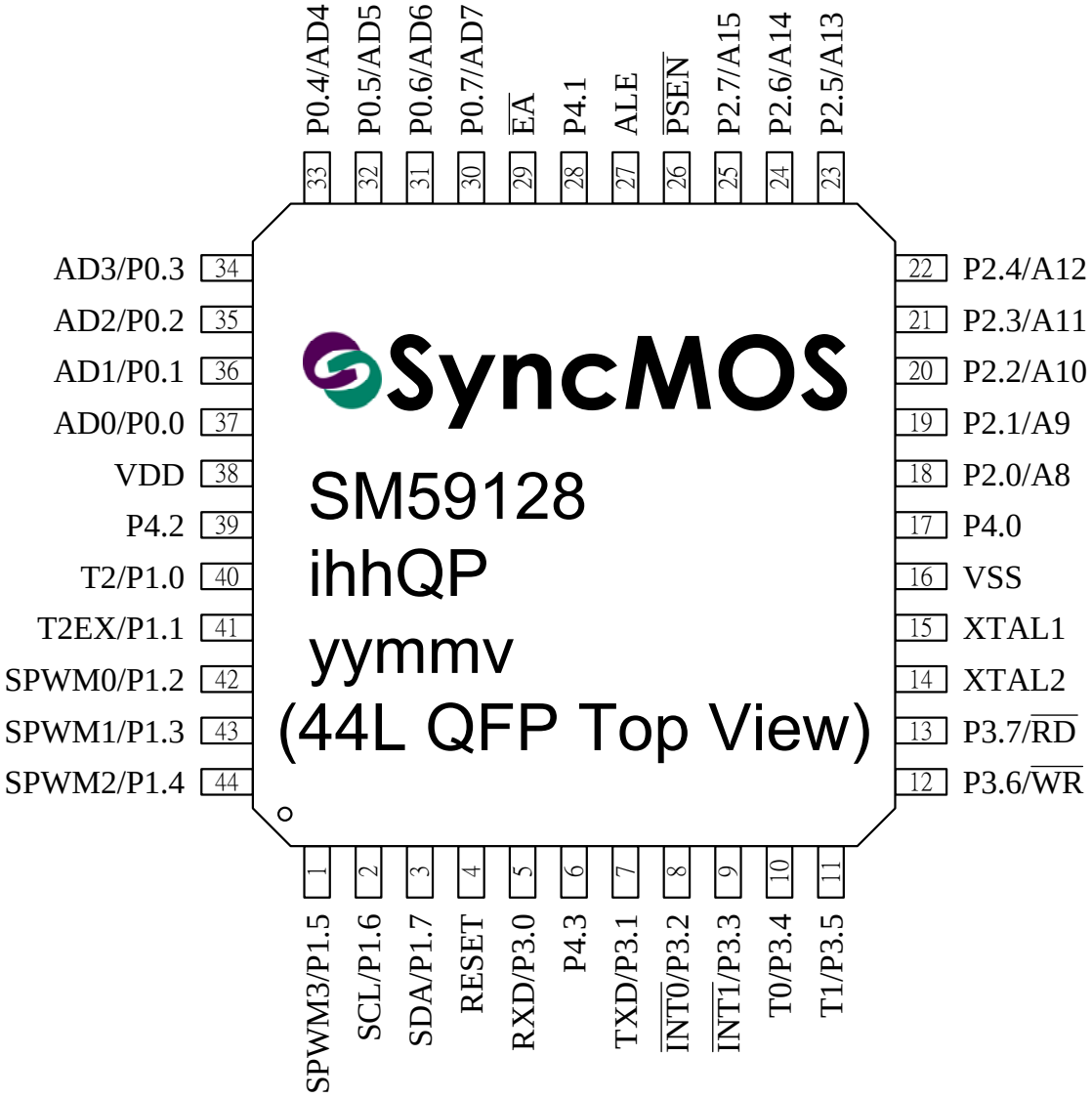
886-3-567-1880
FAX: 886-3-567-1891
886-3-567-1894

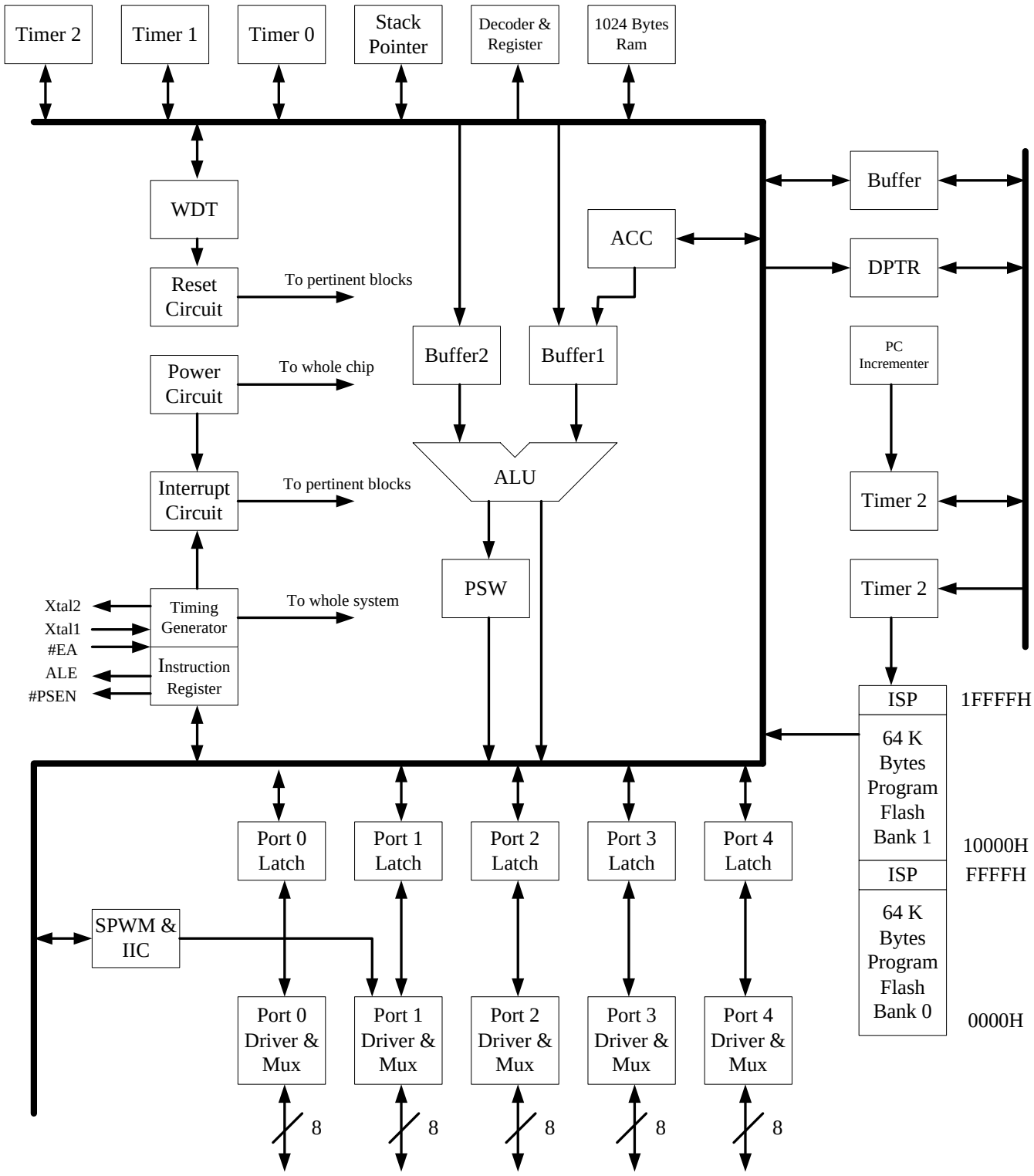
Pin Configuration




P1.4/SPWM2
P1.3/SPWM1
P1.2/SPWM0
P1.1/T2EX
P1.0/T2
P4.2
VDD
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
6
5
4
3
2
1
44
43
42
41
40
SPWM3/P1.5 7
SCL/P1.6 8
SDA/P1.7 9
RESET 10
RXD/P3.0 11
P4.3 12
TXD/P3.1 13
INT0/P3.2 14
INT1/P3.3 15
T0/P3.4 16
T1/P3.5 17
39 P0.4/AD4
38 P0.5/AD5
37 P0.6/AD6
36 P0.7/AD7
35 EA
34 P4.1
33 ALE
32 PSEN
31 P2.7/A15
30 P2.6/A14
29 P2.5/A13
SyncMOS
SM59128
ihhJP
yymmv
(44L PLCC Top View)
18
19
20
21
22
23
24
25
26
27
28
WR/P3.6
RD/P3.7
XTAL2
XTAL1
VSS
P4.0
A8/P2.0
A9/P2.1
A10/P2.2
A11/P2.3
A12/P2.4


P0.4/AD4 33
P0.5/AD5 32
P0.6/AD6 31
P0.7/AD7 30
EA 29
P4.1 28
ALE 27
PSEN 26
P2.7/A15 25
P2.6/A14 24
P2.5/A13 23
AD3/P0.3 34
AD2/P0.2 35
AD1/P0.1 36
AD0/P0.0 37
VDD 38
P4.2 39
T2/P1.0 40
T2EX/P1.1 41
SPWM0/P1.2 42
SPWM1/P1.3 43
SPWM2/P1.4 44
22 P2.4/A12
21 P2.3/A11
20 P2.2/A10
19 P2.1/A9
18 P2.0/A8
17 P4.0
16 VSS
15 XTAL1
14 XTAL2
13 P3.7/RD
12 P3.6/WR
SyncMOS
SM59128
ihhQP
yymmv
(44L QFP Top View)
1 SPWM3/P1.5
2 SCL/P1.6
3 SDA/P1.7
4 RESET
5 RXD/P3.0
6 P4.3
7 TXD/P3.1
8 INT0/P3.2
9 INT1/P3.3
10 T0/P3.4
11 T1/P3.5

Block Diagram



Pin Description

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0/T2		i/o	bit 0 of port 1 & timer 2 clock out
2	41	3	P1.1/T2EX		i/o	bit 1 of port 1 & timer 2 control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3/SPWM0		i/o	bit 3 of port 1 & SPWM channel 0
5	44	6	P1.4/SPWM1		i/o	bit 4 of port 1 & SPWM channel 1
6	1	7	P1.5/SPWM2		i/o	bit 5 of port 1 & SPWM channel 2
7	2	8	P1.6/SCL		i/o	bit 6 of port 1 & IIC Bus Clock
8	3	9	P1.7/SDA		i/o	bit 7 of port 1 & IIC Bus Data
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR		i/o	bit 6 of port 3 & ext. memory write
17	13	19	P3.7/#RD		i/o	bit 7 of port 3 & ext. memory Read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of ext. memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of ext. memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of ext. memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of ext. memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of ext. memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of ext. memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of ext. memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of ext. memory address
29	26	32	#PSEN		o	program storage enable
30	27	33	ALE		o	address latch enable
31	29	35	#EA	L	I	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of ext. memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of ext. memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of ext. memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of ext. memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of ext. memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of ext. memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of ext. memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of port 4

Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only.
Address $80 to $FF is SFR area.
The following table lists the SFR's, which are identical to general 8052, as well as SM59128 Extension SFR's.

Special Function Register (SFR) Memory Map

$F8									$FF
$F0	B				**ISPFAH**	**ISPFAL**	**ISPFD**	**ISPC**	$F7
$E8									$EF
$E0	ACC								$E7
$D8	**P4**								$DF
$D0	PSW								$D7
$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			$CF
$C0	**IICS**	**IICA**	**IICC1**	**IICC2**	**IICTxD**	**IICRxD**			$C7
$B8	IP	**IP1**						**SCONF**	$BF
$B0	P3								$B7
$A8	IE	**IE1**	**IFR**						$AF
$A0	P2			**SPWMC**	**SPWMD0**	**SPWMD1**	**SPWMD2**	**SPWMD3**	$A7
$98	SCON	SBUF		**P1CON**				**WDTC**	$9F
$90	P1							**WDTKEY**	$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH		**RCON**		PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM59128

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	**RCON**	00H	RAMS7	RAMS6	RAMS5	RAMS4	RAMS3	RAMS2	RAMS1	RAMS0
97H	**WDTKEY**	00H	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0
9BH	**P1CON**	**0000**	IICSDAE	IICSCLE	SPWME3	SPWME2	SPWME1	SPWME0		
9FH	**WDTC**	0*0**000	WDTE		CLEAR			PS2	PS1	PS0
A3H	**SPWMC**	******00							SPFS1	SPFS0
A4H	**SPWMD0**	00H	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
A5H	**SPWMD1**	00H	SPWMD14	SPWMD13	SPWMD12	SPWMD11	SPWMD10	BRM12	BRM11	BRM10
A6H	**SPWMD2**	00H	SPWMD24	SPWMD23	SPWMD22	SPWMD21	SPWMD20	BRM22	BRM21	BRM20
A7H	**SPWMD3**	00H	SPWMD34	SPWMD33	SPWMD32	SPWMD31	SPWMD30	BRM32	BRM31	BRM30
BFH	**SCONF**	0***0000	WDR				BANK	ISPE	OME	ALEI
C0H	**IICS**	0000*100	RXIF	TXIF	TFIF	NAKIF		RXAK	MASTER	TXAK
C1H	**IICA**	10100000	IICA7	IICA6	IICA5	IICA4	IICA3	IICA2	IICA1	EXT ADDR
C2H	**IICC1**	0***0001	IICE				Bus Busy	IICFS2	IICFS1	IICFS0
C3H	**IICC2**	00H	Match	SRW			RESTART			MRW
C4H	**IICTxD**	FFH	IICTxD7	IICTxD6	IICTxD5	IICTxD4	IICTxD3	IICTxD2	IICTxD1	IICTxD0

C5H	**IICRxD**	00H	IICRxD7	IICRxD6	IICRxD5	IICRxD4	IICRxD3	IICRxD2	IICRxD1	IICRxD0
A9H	**IE1**	00						EIIC		
AAH	**IFR**	00						IICF		
BAH	**IP1**	00							PIIC	
C8H	**T2CON**	00H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9H	**T2MOD**	******00	*	*	*	*	*	*	T2OE	DCEN
D8H	**P4**	****1111					P4.3	P4.2	P4.1	P4.0
F4H	**ISPFAH**	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	**ISPFAL**	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	**ISPFD**	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	**ISPC**	0*0***00	START		FAU0				F1	F0

Extension Function Description

1. Memory Structure

The SM59128 has the general 8052 hardware core integration of expanded 768 bytes data RAM and 128K bytes flash. The 128K bytes on-chip flash is divided in two 64K bytes program memory space.

1.1 Program Memory

The SM59128 has two 64K bytes on-chip flash memory space as general program memory denoted by bank0 and bank1. Both bank0 and bank1 have up to 4K bytes specific ISP service program memory space. The address range of the 128K bytes is from $0000H to $1FFFFH, the total available ISP service program space is from $F000H to $FFFFH in bank0 and $1F000H to $1FFFFH in bank1. The ISP service program size can be partitioned to N blocks of 512 bytes (N=0 to 8). When N=0 means no ISP service program space is available, total 128K bytes flash memory space is for main program. When N=1 means memory address $FE00H to $FFFFH and $1FE00H to $1FFFFH are reserved for ISP service program. When N=2 means memory address $FC00H to $FFFFH and $1FC00H to $1FFFFH are reserved for ISP service program...etc. User is able to select and program the number of N by writer.

The feature of FLASH memory is shown as following:

READ: byte-wise

WRITE: byte-wise within 30us (previously erased by a chip erase).

ERASE:

Full Erase (64K bytes) within 2 sec.

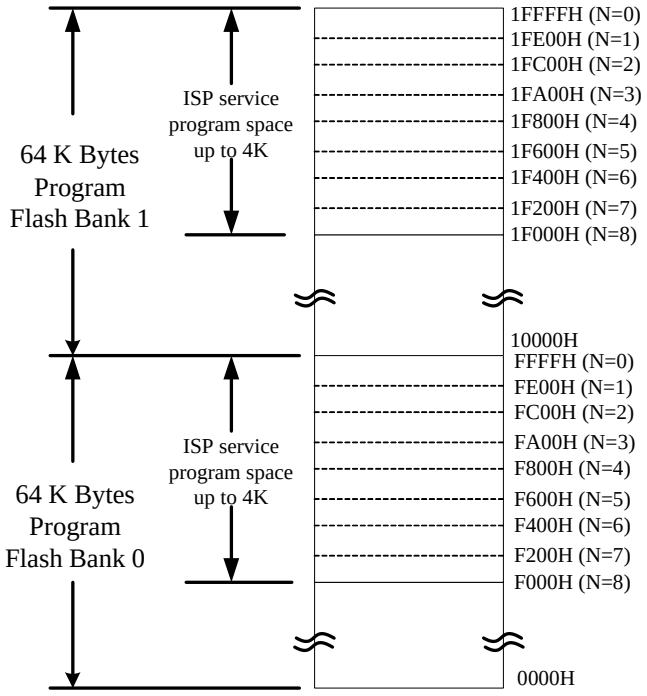
Erased bytes contain FFH

Endurance : 100K erase and write cycles each byte at TA=25℃

Retention : 10 years

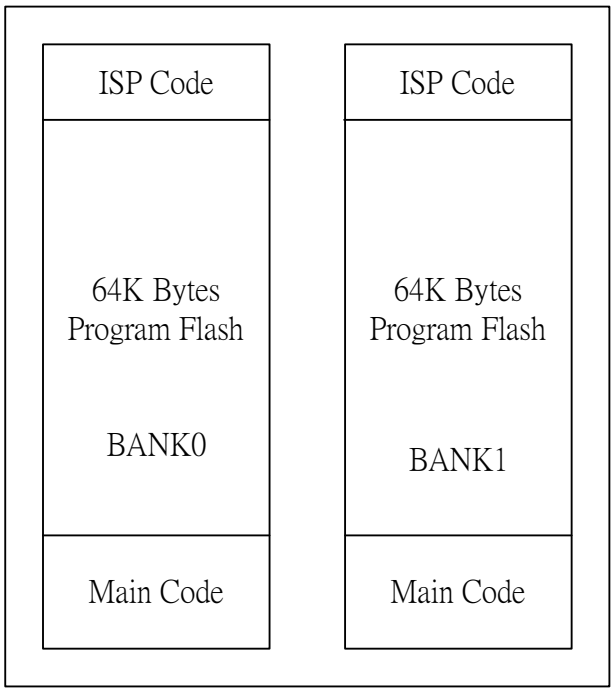
1.1.1 Program Code Security

MOVC instruction executed from external program memory space will not be able to fetch internal codes from on-chip program memory space when the chip is protected.



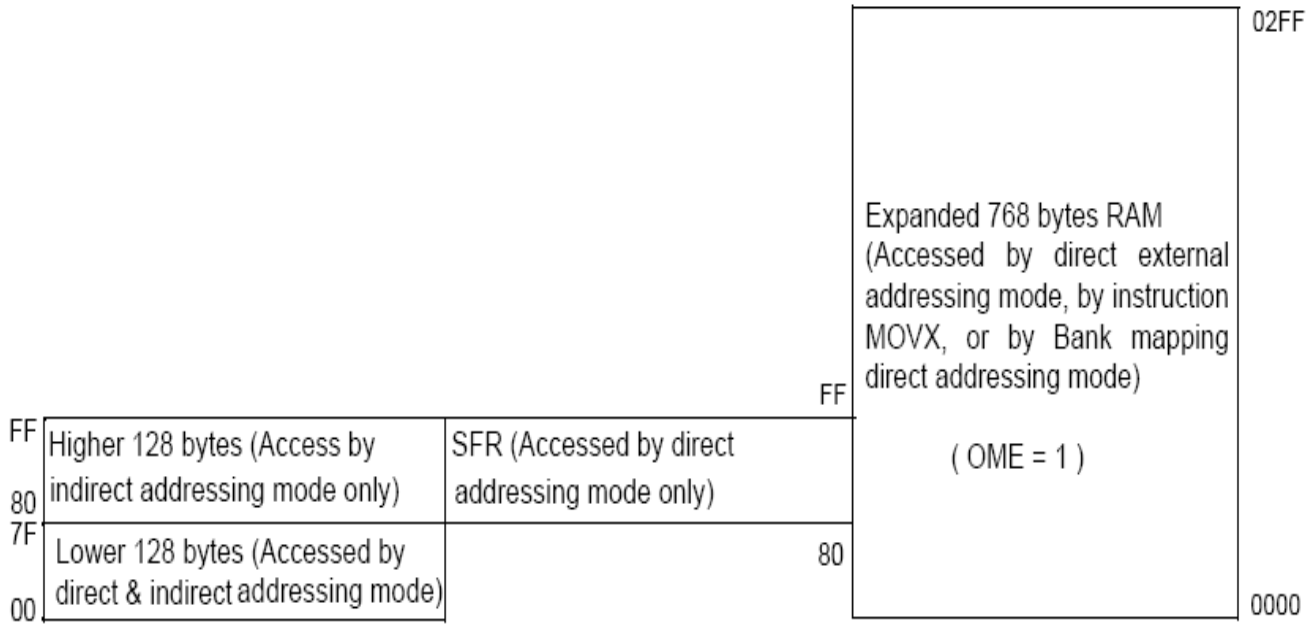
Note: The single flash block address structure of doing the ISP function for the on-chip data flash as well as program flash.

BANK	128K Program Flash
0	BANK0 (64K Flash)
1	BANK1 (64K Flash)



1.2 Data Memory

The SM59128 has 1024 bytes on-chip RAM consists of 256 bytes as same as 8052 internal memory structure and expanded 768 bytes on-chip RAM that can be accessed by external memory addressing method (by instruction MOVX), or by 'Bank mapping direct addressing mode'. User can use MOVX instruction to access internal RAM or external memory by setting OME. The different setting of OME will map to different memory block.



On-chip expanded RAM address structure.

OME	address of MOVX below 768	address of MOVX over 768
0	external memory	external memory
1	internal RAM	external memory

1.2.1 Data Memory - Lower 128 byte ($00 to $7F)

Data Memory $00 to $FF follow 8052.

The address $00 to $7F can be accessed by direct and indirect addressing modes.

Address $00 to $1F is register area.

Address $20 to $2F is memory bit area.

Address $30 to $7F is general memory area.

1.2.2 Data Memory - Higher 128 byte ($80 to $FF)

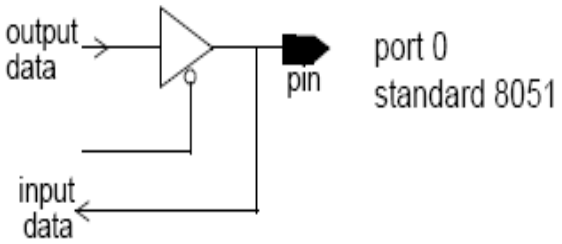
The address $80 to $FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.

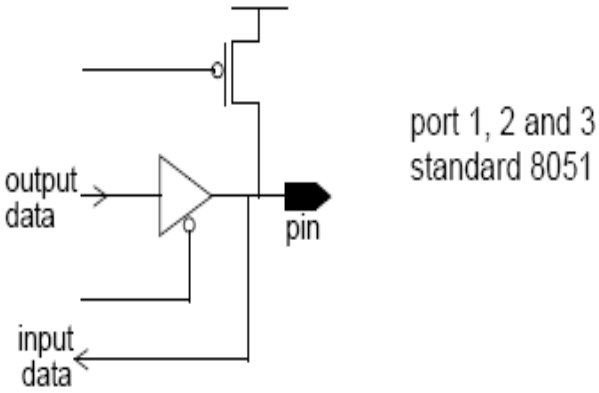
Address $80 to $FF is data area.

1.3 I/O Pin Configuration

The ports 1, 2 and 3 of standard 8051 have internal pull-up resistor, and port 0 has open-drain output. Each I/O pin can be used independently as an input or an output. When an I/O port used as an input pin, the port bit latch must contain a '1' to turn off the output driver FET. Port 1, 2 and 3 pins are pulled high by a weak internal pull-up, and can be pulled low by an external source. The port 0 has open-drain output which means its pull-ups are not active during normal port operation. Writing '1' to the port 0 bit latch will cause bit floating so that it can be used as a high-impedance input.

The port 4 can be used as GPIO has the same function as port 1, 2 and 3.





2. Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and port address is located at 0D8H. The function of port 4 is as same as port 1, port 2 and port 3.

Port4 (P4, $D8)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 out put the setting to pin P4.3, P4.2, P4.1, P4.0, respectively.

3. In-System Programming (ISP) Function

The SM59128 can generate flash control signals by internal hardware circuit. User is able to utilize flash control register, flash address register and flash data register to execute the in-system programming (ISP) function without removing the SM59128 from system board. The SM59128 provides internal flash control signals for users who would like to perform on-line data update by utilizing ISP service program to execute the flash program/chip erase/page erase/protect functions.

3.1 ISP Service Program

The ISP service program is a user-develop firmware program, which resides in the ISP service program space that is reserved by N*512 bytes (N=0 to 8). After user develops the ISP service program, user shall determine the size of the ISP service program space by setting a fittest N value before programming the ISP program code into the SM59128.

The ISP service program is developed by either IC vendor or user his own, and it shall include the features which relate to the flash memory programming function as well as communication protocol between SM59128 and host device. For example, if user utilizes UART interface to receive/transmit data between SM59128 and host device, the ISP service program shall include baud rate, checksum, parity check or any error-checking mechanism to avoid data transmission error.

User shall note the ISP service program can be initiated under active or idle mode, cannot be initiated under power down mode.

3.2 Lock Bit (N)

The Lock Bit, N represents two functions, the first is for service program size configuration and the second is to protect and prevent the ISP service program space from erase.

The address range for the ISP service program is from $F000H to $FFFFH of bank0 and $1F000H to $1FFFFH of bank1. It can be divided to blocks of N*512 bytes (N=0 to 8). When N=0 means no ISP space, all of 128K byte flash memory can be only used as program memory. When N=1 means ISP service program occupies 512 bytes , the rest of 63.5K bytes in both bank0 and bank1 can be used as program memory. The allowed maxima ISP service program space is 4K bytes (N=8). Under such configuration, the usable program memory space is 60K bytes in each bank.

After the lock bit N is determined, SM59128 will reserve the ISP service program space downward from the top of the program address $FFFFH of bank0 and $1FFFFH of bank1. The starting address of the ISP service program locates at $Fx00H and $1Fx00H while x is an even number depending on the lock bit N. Please see page 7 to refer ISP service program space structure.

The setting of lock bit N is different from the setting of flash protect function. **The ISP chip erase function is able to erase all of the 128KB flash memory space except the locked ISP service program space of bank0 (Note: The locked ISP service program space of bank1 will be erased if user executes ISP chip erase function).** If SM59128 is not protected, the content of flash data is readable. If SM59128 is protected, the whole flash program memory space including ISP service program can not be read.

3.3 Program the ISP Service Program

After setting the lock bit N and ISP service program has been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N internally is controlled by a specific program/erase timing which is different from the program/erase timing of flash function. User can erase the locked ISP service program by writer only. **The ISP chip erase function is able to erase all of the 128KB flash memory space except the locked ISP service program space of bank0 (Note: The locked ISP service program space of bank1 will be erased if user executes ISP chip erase function).** User can not update any ISP service program code while SM59128 residents on system board.

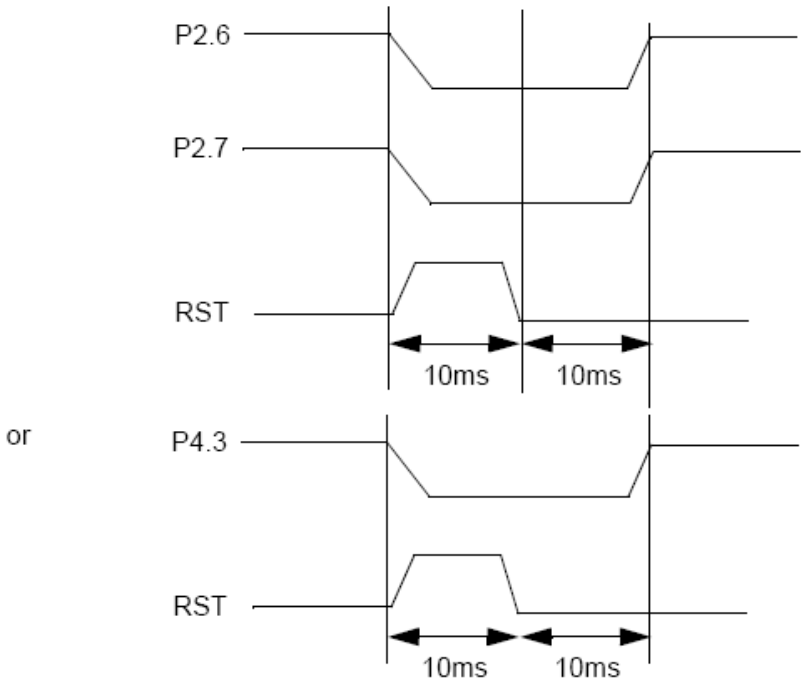
3.4 Initiate ISP Service Program

To initiate the ISP service program means to load the program counter (PC) with starting address of ISP service program and execute. There are three ways to approach:

(1) Blank reset: When Hardware resets and the first address is blank ($0000=#FFH) will automatically load the PC with starting address of ISP service program and execute.

(2) 'JUMP' instruction: Load the starting address of the ISP service program to PC and execute.
(3) Hardware setting: User can force SM59128 to enter/execute ISP service program by setting P2.6, P2.7 as "low" or setting P4.3 as "low" during hardware reset period. User must be careful on setting of P2.6, P2.7 and P4.3 during reset period to prevent SM59128 from accidentally entering ISP service program.

Hardware setting to enter/execute ISP service program:



User can initiate general 8052 UART function to initiate the ISP service program. After ISP service program executed, user needs to reset the SM59128, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

3.5 ISP Registers - System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDTE	Unused	Unused	Unused	BANK	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value:	0	*	*	*	0	0	0	0

The bit 2 (ISPE) of SCONF is the bit for ISP enable. User can enable overall ISP function by setting ISPE bit to '1', setting ISPE to '0' will disable overall ISP function.
The function of ISPE is like a security key. User can disable overall ISP function to prevent user's software program be erased accidentally.

3.6 ISP Registers: ISPFAH, ISPFAL, ISPFD and ISPC registers

The ISPFAH & ISPFAL provide the 16-bit flash memory addressing for ISP function. The flash memory address should not include the ISP service program space address. If the address of ISPFAH & ISPFAL registers overlay the ISP service program space that is under protection, the ISP function of flash program/page erase can not be executed effectively. When performing byte program ISP function, the content of ISPFD register will be programmed to the flash

address, which is pointed by ISPFAH and ISPFAL registers.

ISP Registers- Flash Address-High Register (ISPFAH, $F4)

bit-7 bit-0

	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA15 ~ FA8: flash address (high) for ISP function

ISP Registers - Flash Address-Low Register (ISPFAL, $F5)

bit-7 bit-0

	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA7 ~ FA0: flash address (low) for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory addressing for ISP function. The flash memory address should not include the ISP service program space address. If the address of ISPFAH & ISPFAL registers overlay the ISP service program space that is under protection, the ISP function of flash program/page erase can not be executed effectively.

ISP Registers - Flash Data Register (ISPFD, $F6)

bit-7 bit-0

	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FD7 ~FD0: flash data for ISP function

The ISPFD provides the 8-bit data for ISP function

ISP Registers -Flash Control Register (ISPC, $F7)

bit-7 bit-0

	START	Unused	FAU0	Unused	Unused	Unused	ISPF1	ISPF0
Read / Write:	R/W	-	R/W	-	-	-	R/W	R/W
Reset value:	0	*	0	*	*	*	0	0

ISPF [1:0]: ISP function select bit

ISPF [1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase (512Byte)
11	Chip erase

※The ISP chip erase function is able to erase all of the 128KB flash memory space except the locked ISP service program space of bank0 (Note: The locked ISP service program space of bank1 will be erased if user executes ISP chip erase function).

START: ISP function start bit
= 1: start ISP function which indicated by bit 1, bit 0 (ISPF1, ISPF0)
= 0: no operation
FAU0: 64K program Flash bank select bit (only in ISP mode used)
= 1: selected 64K bank1 flash
= 0: selected 64K bank0 flash
Note: The default START bit is read-only , user's software must write three specific values 55H, AAH and 55H sequentially to the ISPFD register to enable the START bit write attribute. That is:

```
MOV ISPFD, #55H
MOV ISPFD, #0AAH
MOV ISPFD, #55H
```

After START bit is set to 1 then the SM59128 hardware circuit will latch flash address and data bus and hold the program counter until the START bit reset to 0 when ISP function was finished. The program counter (PC) will point to next instruction after START bit reset to 0. User does not need to check START bit status by software method.

Before executing byte program/page erase ISP function, user needs to specify flash address at first. When executing page erase function, SM59128 will erase whole page of flash address indicated by ISPFAH & ISPFAL registers within the page.

Example: flash address: $XYMN
Page erase function will erase address from $XY00 to $X(Y+1)FF (Y: even number), or
Page erase function will erase address from $X(Y-1)00 to $XYFF (Y: odd number)

To perform the ISP chip erase function, SM59128 will erase all the flash program memory and data flash memory except the ISP service program space if lock bit N has been configured. Also, SM59128 will de-protect the flash memory automatically. After chip protect ISP function is executed, all the flash memory will be read as #00H.

Example: ISP service program performs the "byte program" - to program #22H to the address $1005H

```
MOV ISPFD, #55H
MOV ISPFD, #0AAH
MOV ISPFD, #55H
MOV 0BFh, #04H      ; enable SM59128 ISP function
MOV 0F4h, #10H      ; set flash address-high, 10H
MOV 0F5h, #05H      ; set flash address-low, 05H
MOV 0F6h, #22H      ; set flash data to be programmed, data = 22H
MOV 0F7h, #80H      ; start to program #22H to the flash address $1005H
                    ; after byte program finished, START bit of FCR will be reset to 0 automatically
                    ; program counter then point to the next instruction
```

4. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems, which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever un-predicted reset happened

The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway.

There is a 250KHz RC oscillator embedded in chip. Set WDTE = “1” will enable the RC oscillator and the frequency is independent to the system frequency.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM59128 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

4.1 Watch Dog Timer Registers:

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	bit-7							bit-0
	WDTE	Reserve	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS[2:0] : Overflow period select bits

PS [2:0]	Overflow Period (ms)
000	2.048
001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.144

Watch Dog Key Register - (WDTKEY, $97H)

	bit-7							bit-0
	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
Read / Write:	W	W	W	W	W	W	W	W
Reset value:	0	0	0	0	0	0	0	0

By default, the WDTC is read only. User need to write values 1EH, E1H sequentially to the WDTKEY($97H) register to enable the WDTC write attribute, That is

```
MOV WDTKEY, # 1EH
MOV WDTKEY, # 0E1H
```

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY($97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # 0E1H
MOV WDTKEY, # 1EH
```

Watch Dog Timer Register - System Control Register (SCONF, $BF)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	BANK	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset value:	0	*	*	*	0	0	0	0

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to “1” when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened

5. Reduce EMI Function

The SM59128 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

6. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module contains 1 kind of PWM sub module: SPWM (Specific PWM). SPWM has five 8-bit channels.

6.1 SPWM Function Description:

The 8-bit SPWM channel is composed of an 8-bit register, which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value that programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The SPFS[1:0] settings of SPWMC ($A3) register are dividend of Fosc to be SPWM clock, Fosc/2^(SPFS[1:0]+1). The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is [Fosc/2^(SPFS[1:0]+1)]/32.

6.2 SPWM Registers - P1CON, SPWMC, SPWMD[3:0]

SPWM Registers - Port1 Configuration Register (P1CON, $9B)

	bit-7							bit-0
	IICDAE	IICCLE	SPWME3	SPWME2	SPWME1	SPWME0	Unused	Unused
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Reset value:	0	0	0	0	0	0	*	*

IICDAE: When the bit set to one, the corresponding IICDA pin is active as IICDA function. When the bit reset to zero, the corresponding IICDA pin is active as I/O pin. Four bits are cleared upon reset.
IICCLE: When the bit set to one, the corresponding IICCLE pin is active as IICCLE function. When the bit reset to zero, the corresponding IICCLE pin is active as I/O pin. Four bits are cleared upon reset.
SPWME[3:0]: When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Four bits are cleared upon reset.

SPWM Registers -SPWM Control Register (SPWMC, $A3)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	Unused	Unused	SPFS1	SPFS0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

SPFS[1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

SPFS1	SPFS0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Registers -SPWM Data Register (SPWMD[4:0], $AC, $A7 ~$A4)

	bit-7							bit-0
	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [2:0]2	BRM [2:0]1	BRM [2:0]0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

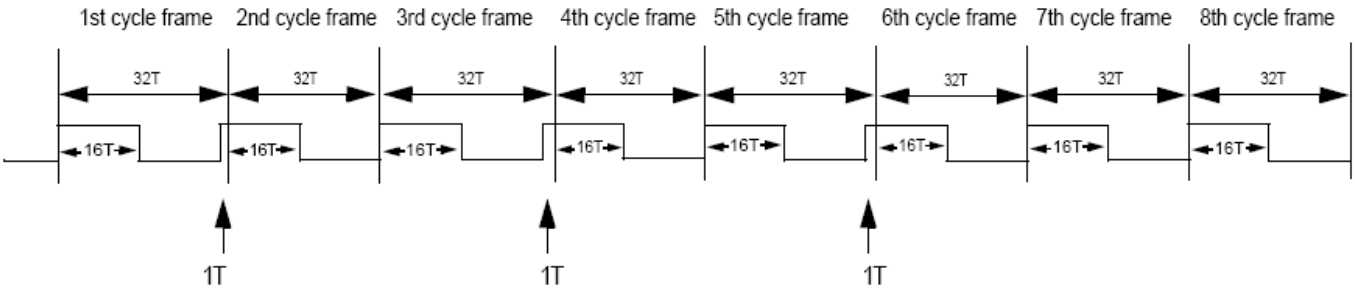
SPWMD[4:0] : content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[2:0] : will insert certain narrow pulses among an 8-SPWM-cycle frame

N = BRM[2:0]	Number of SPWM cycles inserted in an 8-cycle frame
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Example of SPWM timing diagram:

```
MOV  SPWMD0 , #83H          ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM[2:0] = 3
MOV  P1CON , #08H           ; Enable P1.3 as SPWM output pin
```



(narrow pulse inserted by BRM0[2:0] setting, here BRM0[2:0]=3)

SPWM clock = 1 / T = Fosc / 2^(SPFS[1:0]+1)
The SPWM output cycle frame frequency = SPWM clock / 32 = [Fosc/2^(SPFS[1:0]+1)]/32

If user use Fosc=20MHz, SPFS[1:0] of SPWMC=#03H, then
SPWM clock = 20MHz/2^4 = 20MHz/16 = 1.25MHz
SPWM output cycle frame frequency = (20MHz/2^4)/32=39.1KHz

7. IIC Interface (Inter-Integrated Circuit)

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. User can select speed to 6.25K~400Kbps by setting the BR[2..0] control bit in software. The IIC module provide 4 interrupts (Rx, Tx, NonAck, TxFail). It will generate and/or detects START, repeated START and STOP signals automatically in master mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

7.1 IIC Registers

IIC Status Register (IICS, $C0)

	bit-7							bit-0
	RXIF	TXIF	TFIF	NAKIF	-	RXAK	MASTER	TXAK
Read / Write:	Note1	Note1	Note1	Note1		Note2	Note3	Note3
Reset value:	0	0	0	0	Unused	1	0	0

Note1:Read and Writer'0' only

Note2:Read only

Note3:Read and Writer

RXIF: The data Receive Interrupt Flag (RXIF) is set after the IICRDB (IIC Receive Data Buffer) is loaded with a newly receive data. Once the IRDB is loaded with received data, no more received data can be loaded to the IICRDB register again.

TXIF: The data Transmit Interrupt Flag is set when the data of the IICTDB register is downloaded to the shift register or Master Transmit mode the IADR is downloaded to the shift register. It is software's responsibility to fill the IICTDB register with new data when this bit is set. This bit is cleared by writing zero to it, write data to IICTDB or when reset.

TFIF: The Transmit Fail Interrupt Flag is set when the data transmit is fail, which as set MASTER bit when the BB has been set by detecting the start condition on the lines or when the module is transmitting a One to SDA line but detected a Zero from SDA line in master mode, which is also called arbitration loss. This bit is cleared by writing Zero to it or by reset.

NAKIF: The NonAcknowledge Interrupt Flag is only set in the master transmit mode when there is no acknowledge bi detected after one byte data or calling address is transferred. This bit is cleared by writing Zero to it or by reset.

RXAK: If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. If RXAK is high, it indicates no acknowledge signal has been detected at the 9th clock. Then the module will release the SDA line for the master to generate Stop or Repeated Start condition. It is set upon reset.

MASTER: If set the MASTER bit, the module will generate a start condition to the SDA and SCL lines and send out the calling address which is stored in the IADR register. But if the TFIF flag is set when transmit fail occurs on the lines, the module will discard the master mode by clearing the MASTER bit and release both SDA and SCL lines immediately. This bit can also be cleared by writing zero to it or when the NAKIF is set. When the MASTER bit is cleared either by set NAKIF or software the module will generate a stop condition to the lines after the current byte transmission is done, and IGNORE the IICTDB data when next IIC transmit cycle if this data had not been transmit out. Reset clears this bit.

TXAK: The bit (TXAK) control the acknowledge transmit in RECEIVE mode, if it is cleared, a low (Ack) will be generated at the 9th clock after receiving 8 bits data. When TXAK is set, a high (NoAck) will be generated at the 9th clock after receiving 8 bits data. Reset clears this bit.

IIC Address Register (IICA, $C1)

	bit-7							bit-0
Read: Write:	IICA.7	IICA.6	IICA.5	IICA.4	IICA.3	IICA.2	IICA.1	EXTADDR
Reset value:	1	0	1	0	0	0	0	0

IICA[7:1] : These 7 bits can be the chip address in slave mode or the calling address when in master mode. This register is set as $A0 upon reset.

EXTADDR : The EXTAD bit is set to expand the chip address of this module. When it is one, the module will acknowledge the general call address $00 and the address comparison circuit will only compare the 4 MSB bits in the LADR register. When it is zero, the module will only acknowledge to the specific address which is stored in the IADR register. It is zero after reset.

IIC Control Register (IICC1, $C2)

	bit-7							bit-0
Read: Write:	IICE	-	-	-	BB	IICFS2	IICFS1	IICFS0
Reset value:	0	0	0	0	0	0	0	1

IICE: If this IIC module Enable bit (IE1) is set, the IIC module is enable. If the IE1 is clear, the interface is disable and all flags will restore its reset default states. Reset to clear this bit.

BB : The Bus Busy Flag is set after a start condition is detected, and is reset when a stop condition is detected. Reset clears this bit.

IICFS[2:0] :The three Baud Rate select bits will select one of the eight clock rates as the master clock when the module is in master mode. The serial clock frequency is equal to the external clock divided by the certain divider. These bits are cleared upon reset.

IICFS[2:0]	Baud Rate
0:0:0	Unused
0:0:1	400K
0:1:0	200K
0:1:1	100K
1:0:0	50K
1:0:1	25K
1:1:0	12.5K
1:1:1	6.25K

Note: clock source is from external (12M Hz).

IIC Control Register 2 (IICC2, $C3)

	bit-7							bit-0
Read/Write:	MATCH Note1	SRW Note1	-	-	RSTART Note2	-	-	MRW Note3
Reset value:	1	0	0	0	0	0	0	0

Note1: Read and Writer'0' only

Note2: Read only

Note3: Read and Writer

MATCH: The MATCH flag is set when the first received data (following START signal) in the IRDB register which matches with the address or its extended addresses (EXTAD=1) specified in the IADR.

SRW: The Slave Rw bit will indicate the data direction of IIC protocol. It is updated after the calling address is received in the SLAVE mode. When it is one, the master will read the data from IIC module, so the module is in transmit mode. When it is zero, the master will send data to the IIC module, and the module is in receiving mode. The reset clears it.

RESTART: If user sets RESTART bit in master mode (MASTER=1), the module will generate a start condition to the SDA and SCL lines (after current ACK bit) and send out the calling address which is stored in the IICADR register. But if the TFIF flag is set when transmit fail occurs on the lines, the module will discard the master mode by clearing the MASTER bit and release bit SDA and SCL lines immediately. This bit will be cleared automatically after generate a start condition to the SDA and SCL lines. Reset clears this bit.

MRW: This MRW bit will be transmitted out to be the bit 0 of the calling address when the module sets the MAS TER bit to enter the master mode. It will also determine the transfer direction of the following data bytes. When it is one, the module is in master receive mode. When it is zero, the module is in master transmit mode. Reset clears this bit.

IIC Transmit Data Buffer (IICTxD, $C4)

	Bit-7						bit-0
Read: Write:	IICTxD.7	IICTxD.6	IICTxD.5	IICTxD.4	IICTxD.3	IICTxD.2	IICTxD.1	IICTxD.0
Reset value:	0	0	0	0	0	0	0	0

The data written into this register will be automatically downloaded to the shift register when the module detects a calling address is matched and the bit 0 of the received data is one (Slave transmit mode) or when the data in the shift register has been transmitted with received acknowledge bit (RXAK) =0 in transmit mode. So if the program doesn't write the data into the IICTDB register before the matched calling address is detected or the shift register has been transmitted out, the module will pull down the SCL line (after receive acknowledge bit). If write a data to the IICTxD register, then the written data will be downloaded to the shift register immediately and the module will release the SCL line, and the TXIF flag is set to generate another interrupt request for next data. So the S/W may need to write the next data to the IICTxD register and for the auto downloading of data to the shift register after the data in the shift register is transmitted over again with RXAK=0. If the module receiver non-acknowledge (RXAK=1), the module will release the SDA line for master to generate Stop or Repeated Start conditions.

IIC Receive Data Buffer (IICRxD, $C5)

	Bit-7							bit-0
Read:	IICRD.7	IICRD.6	IICRD.5	IICRD.4	IICRD.3	IICRD.2	IICRD.1	IICRD.0
Write:								
Reset value:	0	0	0	0	0	0	0	0

The IIC Receive Data Buffer (IICRxD) contains the last received data when the MATCH flag is one or the calling address from master when the MATCH flag is zero. The IICRxD register will be updated after a data byte is received and the previous received data had been read out, otherwise the DDC module will pull down to SCL line to inhabit the next data transfer. It is a read-only register. The read operation of this register will clear the RXIF flag. After the RXIF flag is cleared, the register can load the received data again and set the RXIF flag the venerate interrupt request for reading the newly received data.

7.2 IIC Interrupt

The IIC module will generate IIC interrupt while hardware circuit detects START signal of IICSDA and IICSCL. The IIC interrupt vector locates at $3B. There are three SFRs for configuring IIC interrupt: IP1, IE1 and IFR. To use IIC interrupt is the same as to use other generic 8052 interrupts. That means using EIIC of IE1 for enable/disable IIC interrupt, using PIIC for assign IIC interrupt priority. Whenever IIC interrupt occurs, IICIF will be set to 1. After IIC interrupt subroutine (vector) been executed, IICIF will be cleared to 0.

Interrupt Priority I Register (IP1, $B9)

	Bit-7							bit-0
Read: Write:	R	R	R	R	R	R	PIIC	R
Reset value:	0	0	0	0	0	0	0	0

Interrupt priority bit PIIC = 1 assigns high interrupt priority
Interrupt priority bit PIIC = 0 assigns low interrupt priority

Interrupt Enable I Register (IE1, $A9)

	Bit-7							bit-0
Read: Write:	R	R	R	R	R	R	EIIC	R
Reset value:	0	0	0	0	0	0	0	0

Interrupt enable bit EIIC = 1 enables the IIC interrupt
Interrupt enable bit EIIC = 0 disables the IIC interrupt

Interrupt Flag Register (IFR, $AA)

	Bit-7							bit-0
Read: Write:	R	R	R	R	R	R	IICIF	R
Reset value:	0	0	0	0	0	0	0	0

Interrupt flag bit IICIF will be set to 1 when IIC interrupt occurs. Interrupt flag bit IICIF will be clear to 0 if IIC interrupt subroutine executed.

7.2 PROGRAM ALGORITHM

When the IIC module detects an arbitration loss in master, it will release both SDA and SCL lines immediately. But if there is no further Stop condition detected, the module will be hanged up.

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

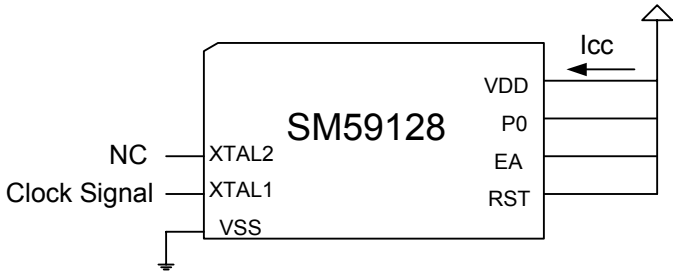
(TA = -40 degree C to 85 degree C, Vcc = 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 ℃
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1:Under steady state (non-transient) conditions, IOL must be externally
Limited as follows : Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 1,2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Note2 : Minimum VCC for Power-down is 2V.

Icc Active Mode Test Circuit



AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT -20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT+20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT-10		3xT+10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT-20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT-35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

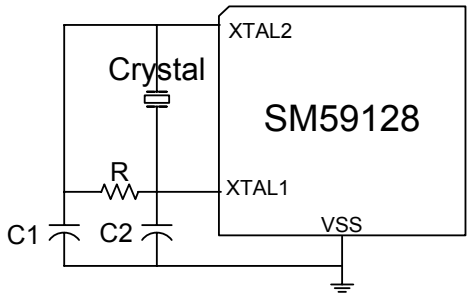
ISP Test Conditions

(40 MHZ, typical operating conditions, valid for SM59128 series)

Symbol	MAX	Remark
Chip erase	3000ms	Vcc = 5V
Page erase	10ms	"
Program	30us	"
Protect	400us	"

Application Reference

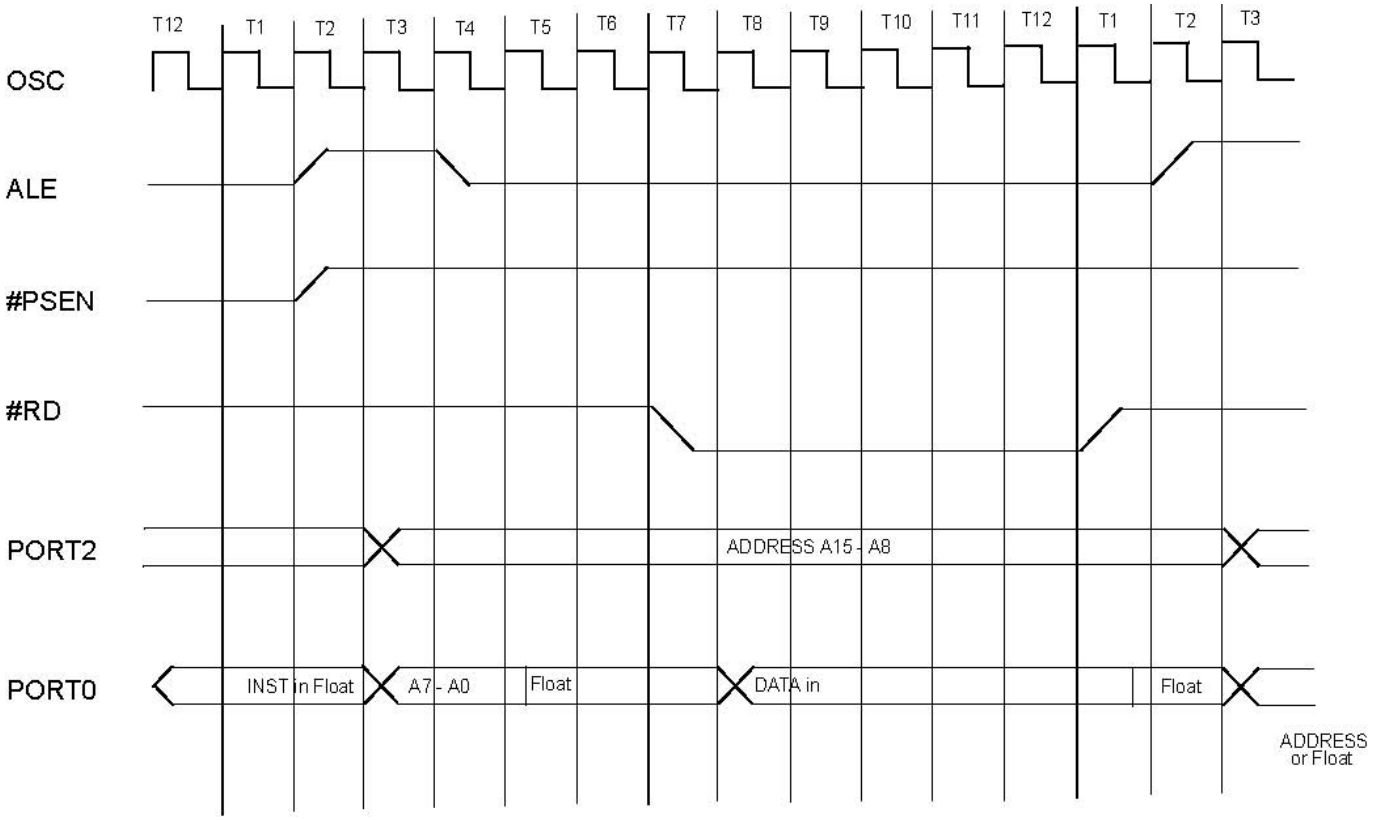
Valid for SM59128				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



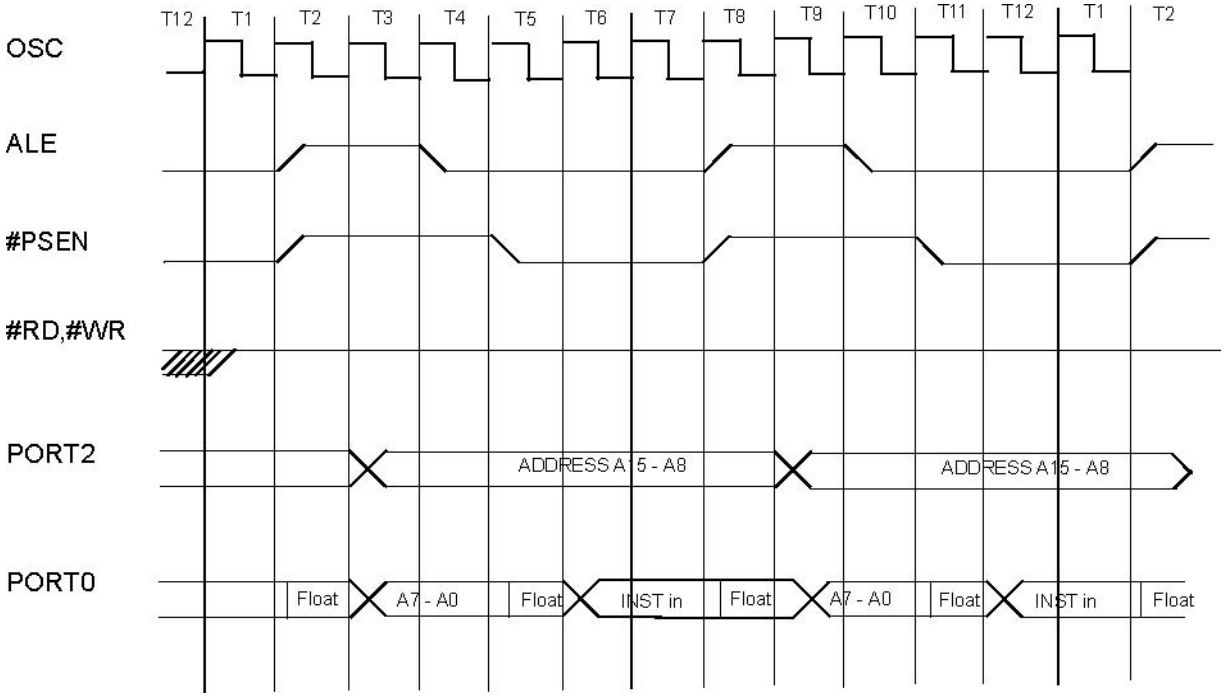
NOTE: Oscillation circuit is varied with different crystal or ceramic resonator in higher oscillation frequency, it depends on crystal, or ceramic resonator of its own characteristics. User should check the crystal or ceramic resonator manufacture for appropriate value of external components.

Please see SM59128 application note for details.

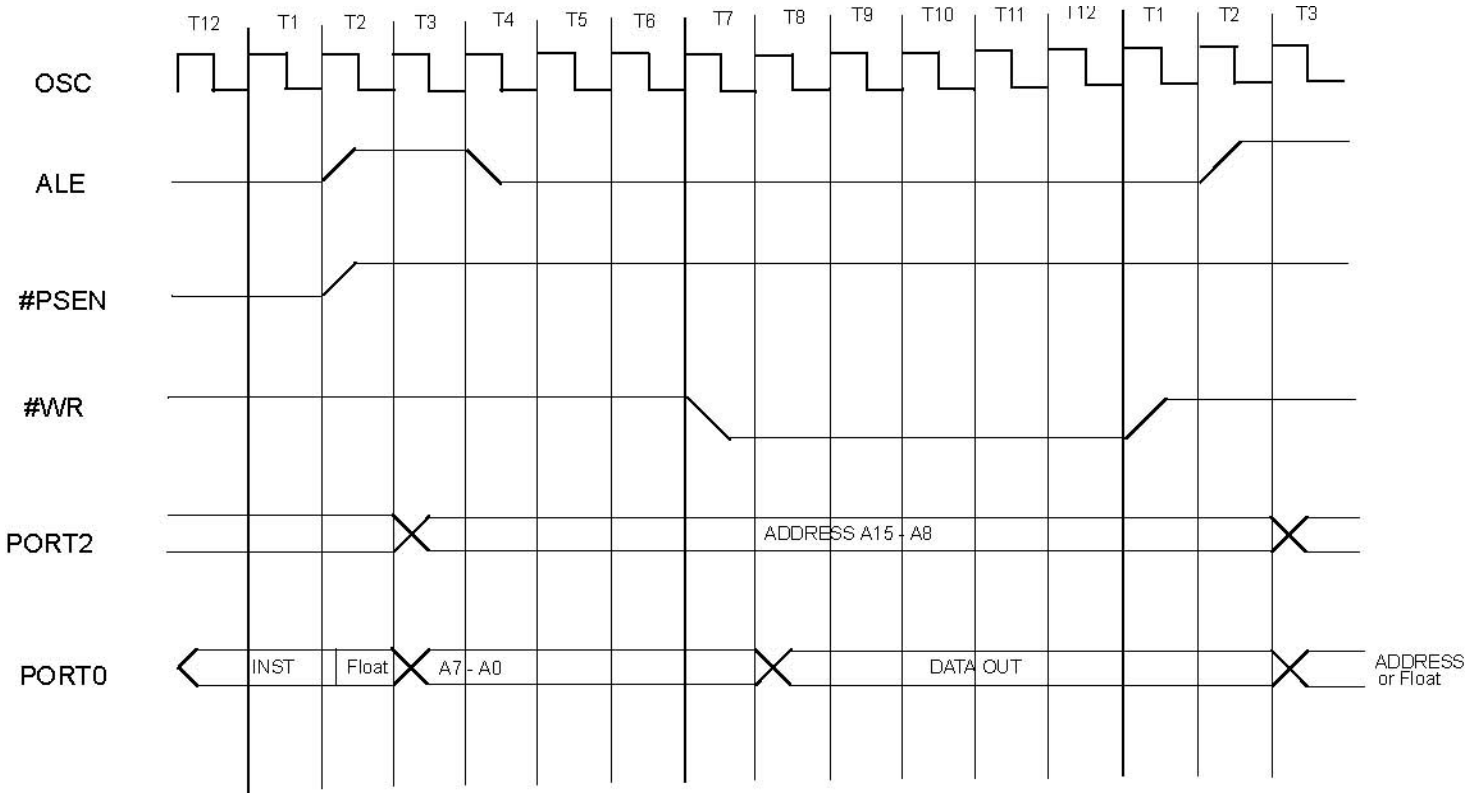
Data Memory Read Cycle Timing



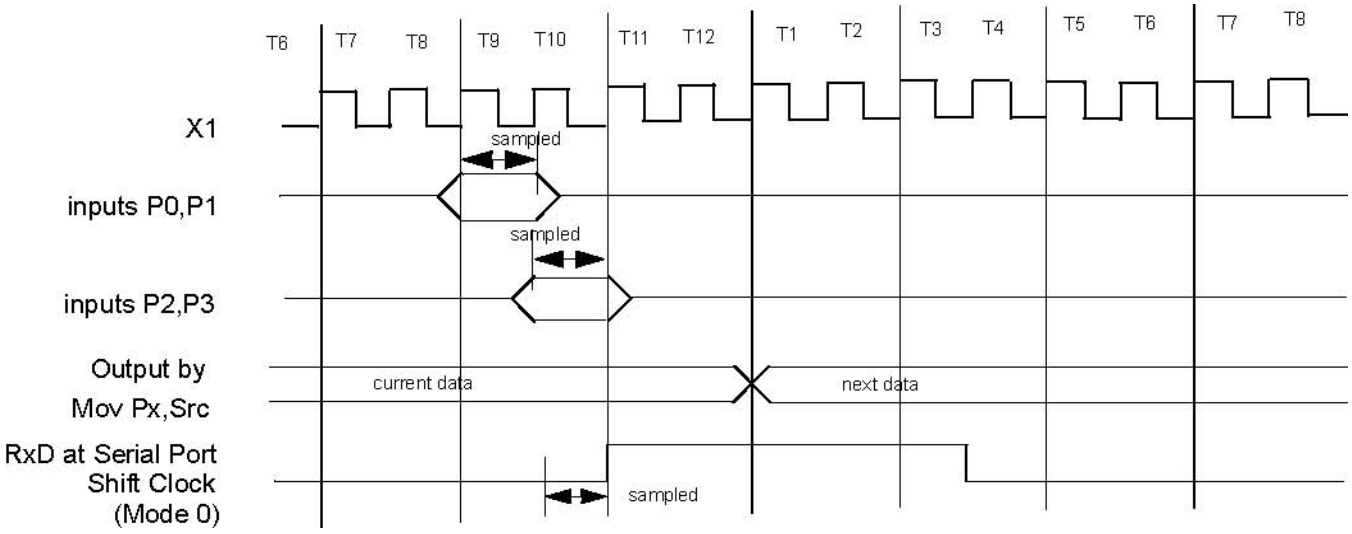
Program Memory Read Cycle Timing



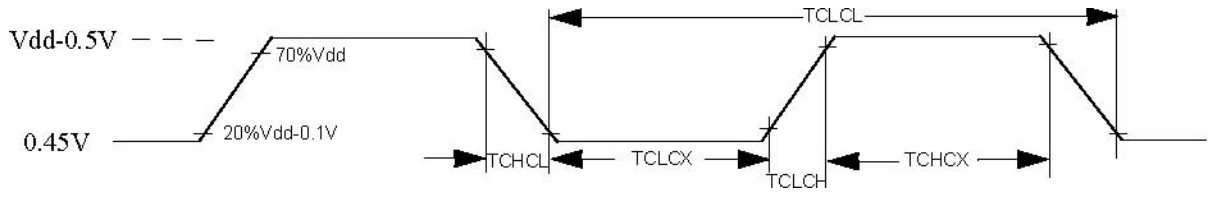
Data Memory Write Cycle Timing



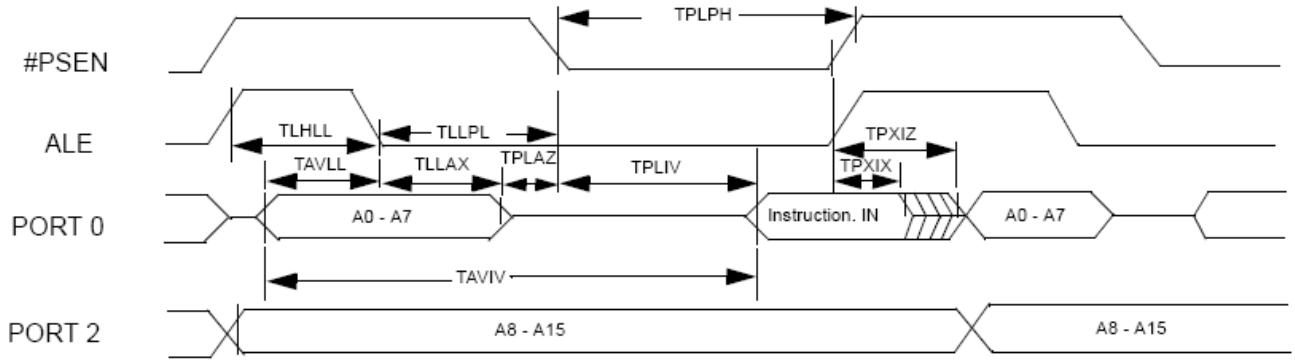
I/O Ports Timing



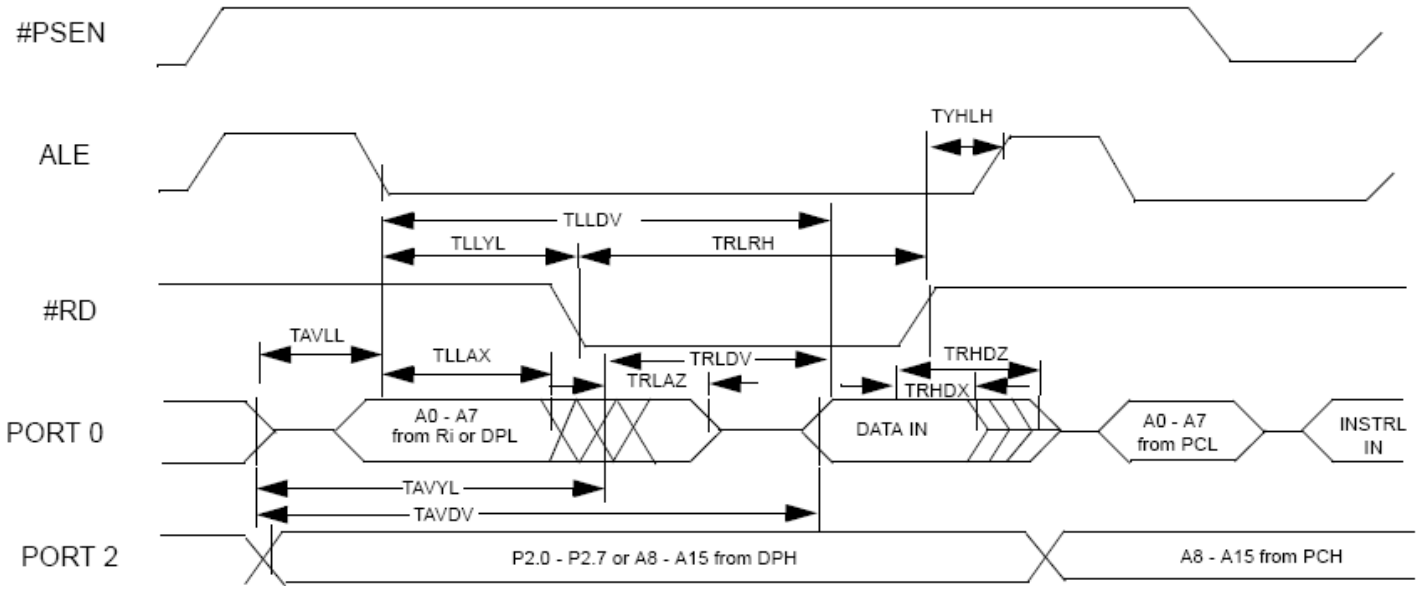
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



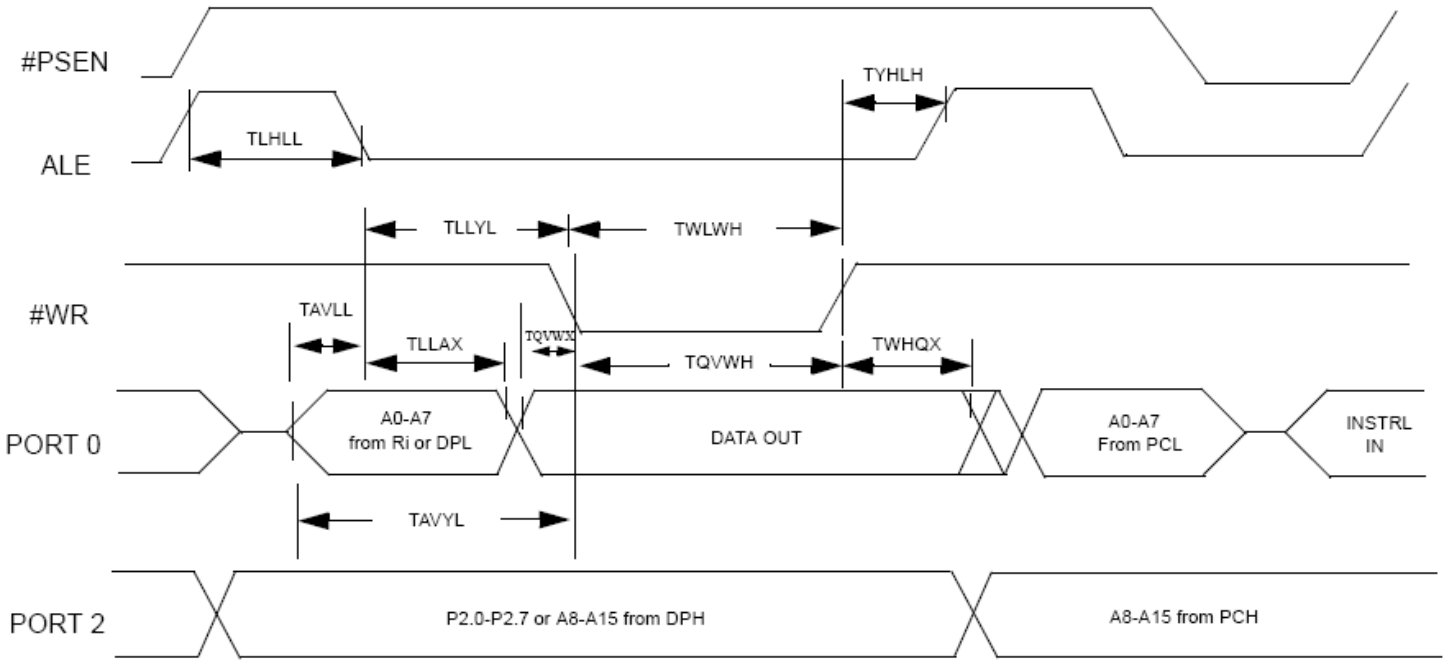
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



MCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	Lab Tool - 48XP/UXP Lab Tool – 848/848XP
Hi-Lo 4F.,No.18,Lane 79,Rueiguang Rd.,Neihu,Taipei,Taiwan R.O.C. Web site: http://www.hilosystems.com.tw	Tel: 02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw	All - 100 series
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei , Taiwan, ROC Web site: http://www.leap.com.tw	Tel: 886-2-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	Leap-48
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TianJin Weilei technology ltd Rm 357,Venturetech Center,12 Keyan West Road Nankai District,Tianjin,P.R.C, 300192 Web site: http://www.weilei.com.cn/	TEL: + 86-22-87891218#801 E-mail: weilong@weilei.com.cn cm@weilei.com.cn	VP-890;VP-980;VP-880;VP-680 VP-480;VP-380;VP-280;VP-190
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